Computer Architecture
Lecture 15: Emerging Memory Technologies
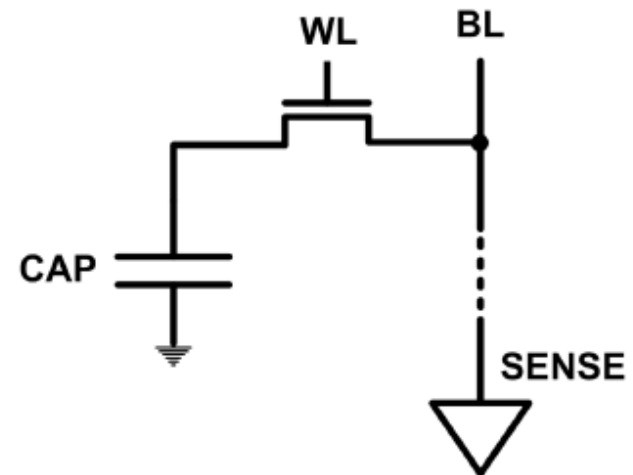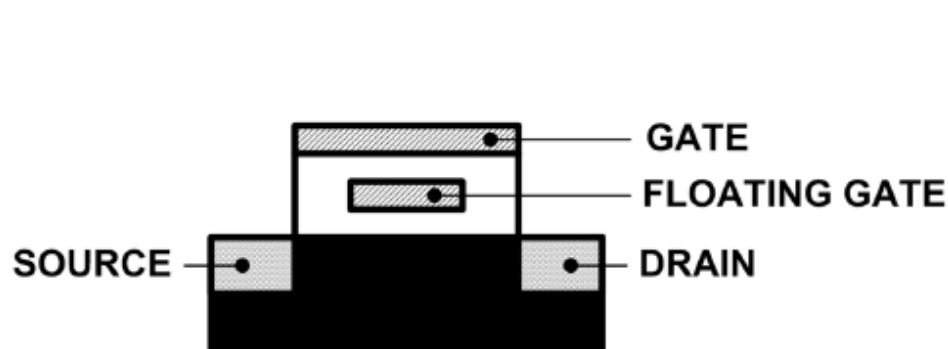
Prof. Onur Mutlu

ETH Zürich

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13 November 2020

Limits of Charge Memory

- Difficult charge placement and control
  - Flash: floating gate charge
  - DRAM: capacitor charge, transistor leakage

- Reliable sensing becomes difficult as charge storage unit size reduces

Solution 1: New Memory Architectures

- Overcome memory shortcomings with
  - Memory-centric system design
  - Novel memory architectures, interfaces, functions
  - Better waste management (efficient utilization)

- Key issues to tackle
  - Enable reliability at low cost → high capacity
  - Reduce energy
  - Reduce latency
  - Improve bandwidth
  - Reduce waste (capacity, bandwidth, latency)
  - Enable computation close to data

Solution 1: New Memory Architectures

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- Hsieh+, "Transparent Offloading and Mapping (TOM): Enabling Programmer-Transparent Near-Data Processing in GPU Systems," ISCA 2016.
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  - Pekhimenko+, "Toggle-Aware Bandwidth Compression for GPUs," HPCA 2016.

Solution 2: Emerging Memory Technologies

- **Some emerging resistive memory technologies seem more scalable than DRAM (and they are non-volatile)**

- Example: Phase Change Memory
    - Data stored by changing phase of material
    - Data read by detecting material's resistance
    - Expected to scale to 9nm (2022 [ITRS 2009])
    - Prototyped at 20nm (Raoux+, IBM JRD 2008)
    - Expected to be denser than DRAM: can store multiple bits/cell
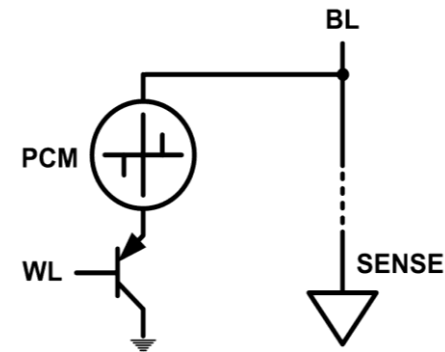
- But, emerging technologies have (many) shortcomings
    - Can they be enabled to replace/augment/surpass DRAM?

Solution 2: Emerging Memory Technologies

- Lee+, "Architecting Phase Change Memory as a Scalable DRAM Alternative," ISCA'09, CACM'10, IEEE Micro'10.
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Charge vs. Resistive Memories

- **Charge Memory (e.g., DRAM, Flash)**
  - Write data by capturing charge Q
  - Read data by detecting voltage V

- **Resistive Memory (e.g., PCM, STT-MRAM, memristors)**
  - Write data by pulsing current dQ/dt
  - Read data by detecting resistance R

Promising Resistive Memory Technologies

- **PCM**
  - Inject current to change material phase
  - Resistance determined by phase

- **STT-MRAM**
  - Inject current to change magnet polarity
  - Resistance determined by polarity

- **Memristors/RRAM/ReRAM**
  - Inject current to change atomic structure
  - Resistance determined by atom distance

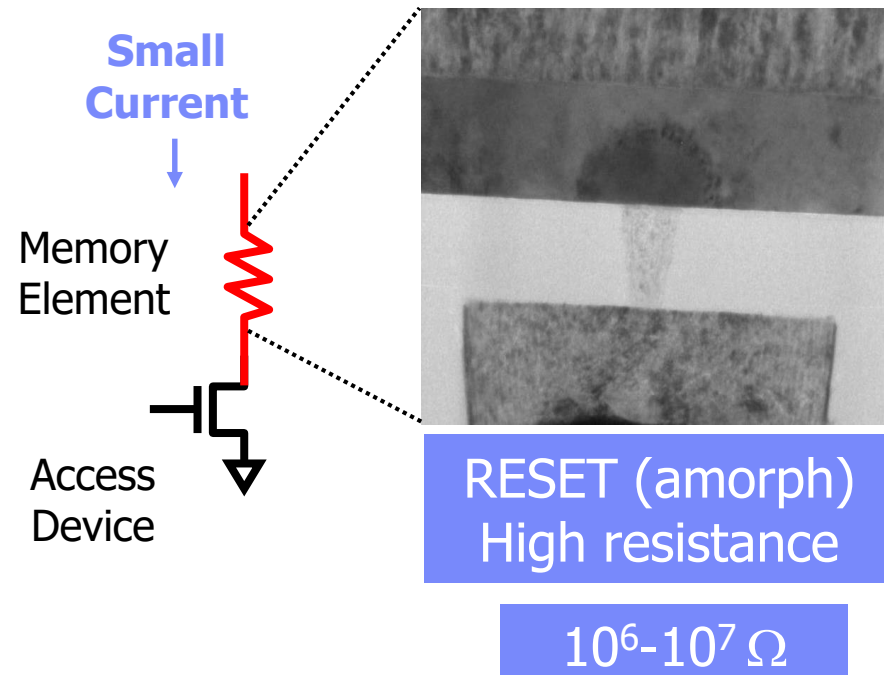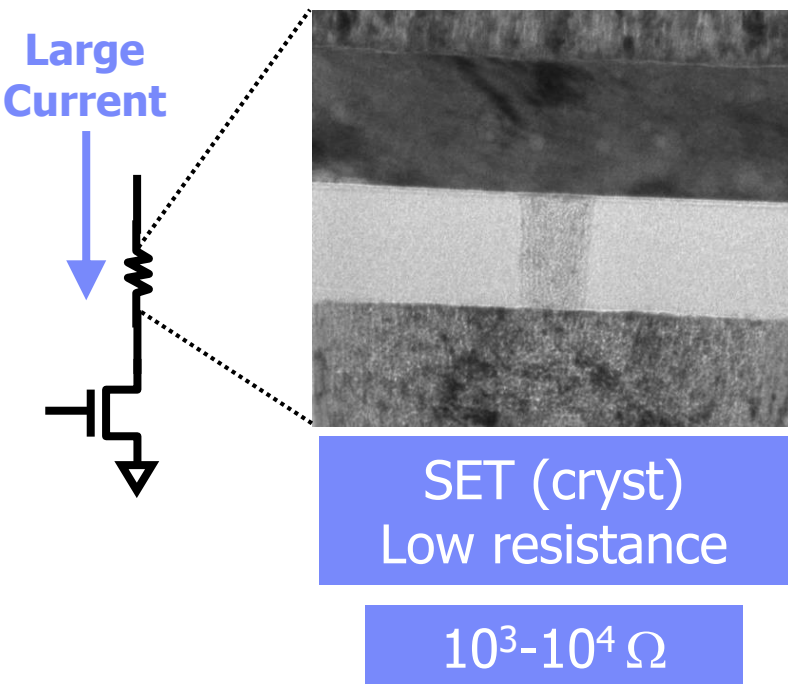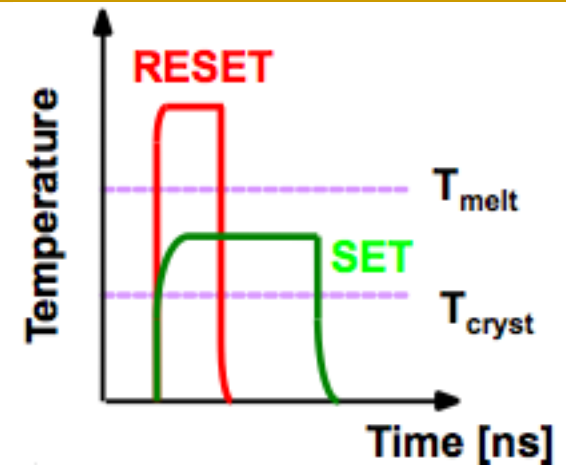# What is Phase Change Memory?

- Phase change material (chalcogenide glass) exists in two states:
  - Amorphous: Low optical reflexivity and high electrical resistivity
  - Crystalline: High optical reflexivity and low electrical resistivity
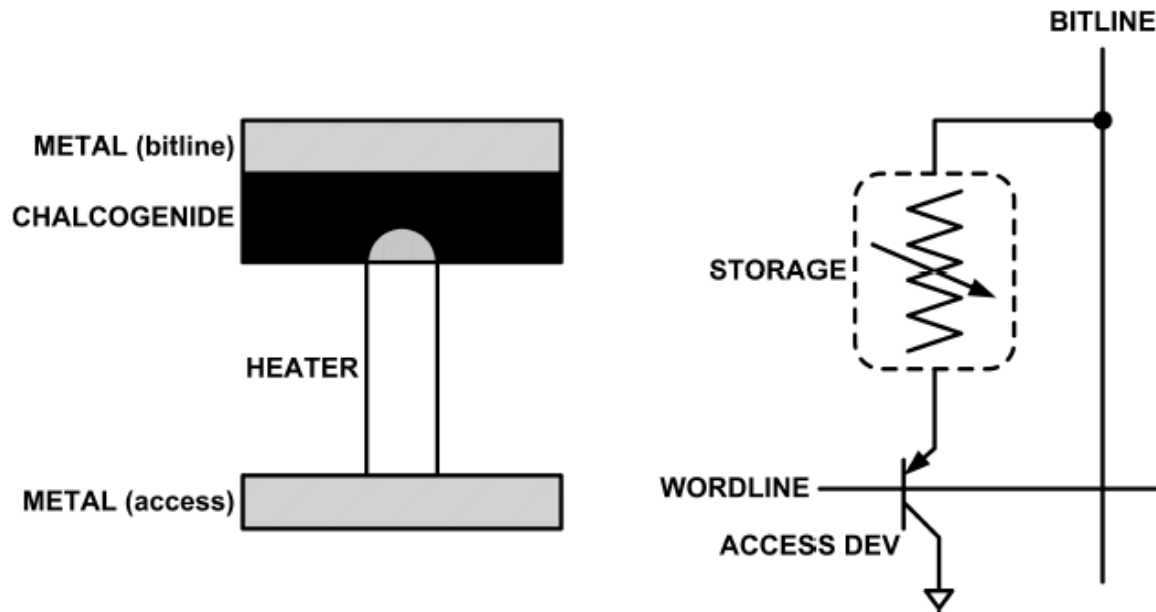
PCM is resistive memory: High resistance (0), Low resistance (1)
PCM cell can be switched between states reliably and quickly

How Does PCM Work?

- Write: change phase via current injection
  - SET: sustained current to heat cell above T_{cryst}
  - RESET: cell heated above T_{melt} and quenched
- Read: detect phase via material resistance
  - amorphous/crystalline

Large Current

Small Current

Memory Element

Access Device

SET (cryst)
Low resistance

10^3-10^4 Ω

RESET (amorph)
High resistance

10^6-10^7 Ω

Photo Courtesy: Bipin Rajendran, IBM   Slide Courtesy: Moinuddin Qureshi, IBM

Opportunity: PCM Advantages

- **Scales better than DRAM, Flash**
  - ❑ Requires current pulses, which scale linearly with feature size
  - ❑ Expected to scale to 9nm (2022 [ITRS])
  - ❑ Prototyped at 20nm (Raoux+, IBM JRD 2008)

- **Can be denser than DRAM**
  - ❑ Can store multiple bits per cell due to large resistance range
  - ❑ Prototypes with 2 bits/cell in ISSCC'08, 4 bits/cell by 2012

- **Non-volatile**
  - ❑ Retain data for >10 years at 85C
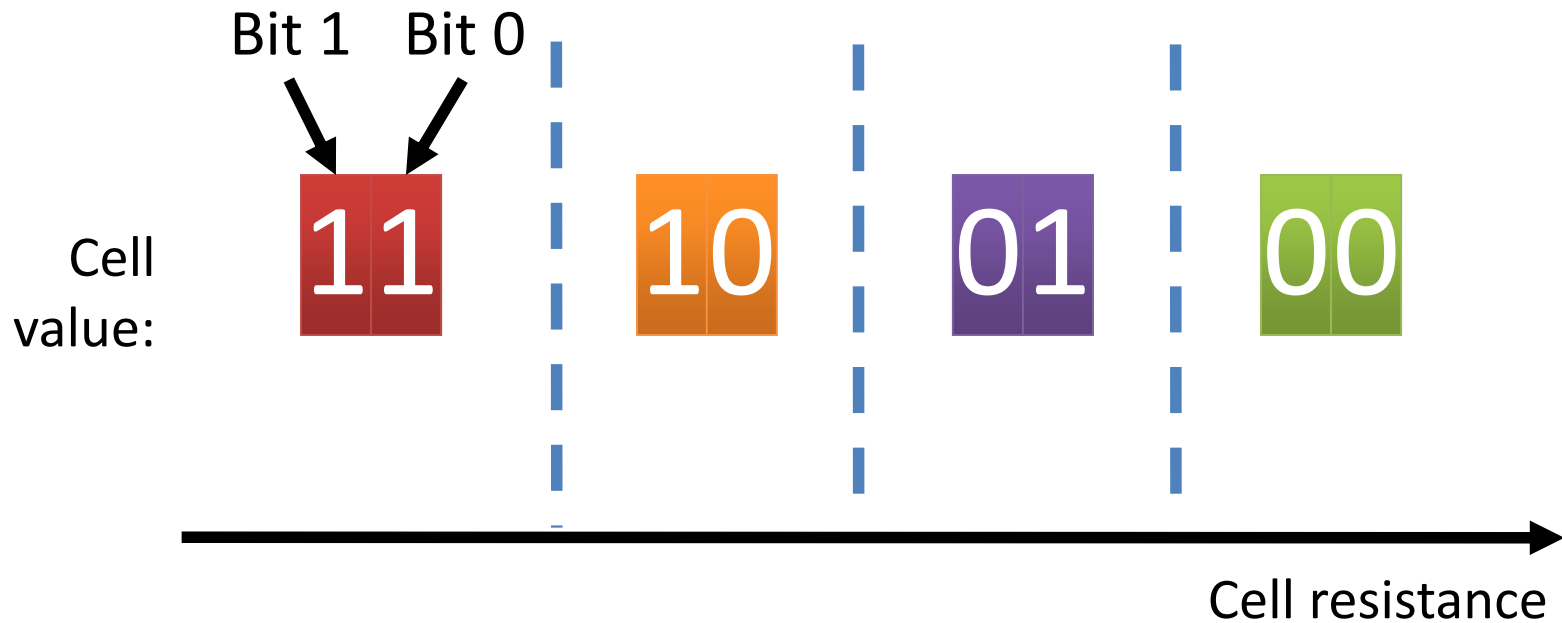
- **No refresh needed, low idle power**

PCM Resistance → Value

Cell value:

1

0
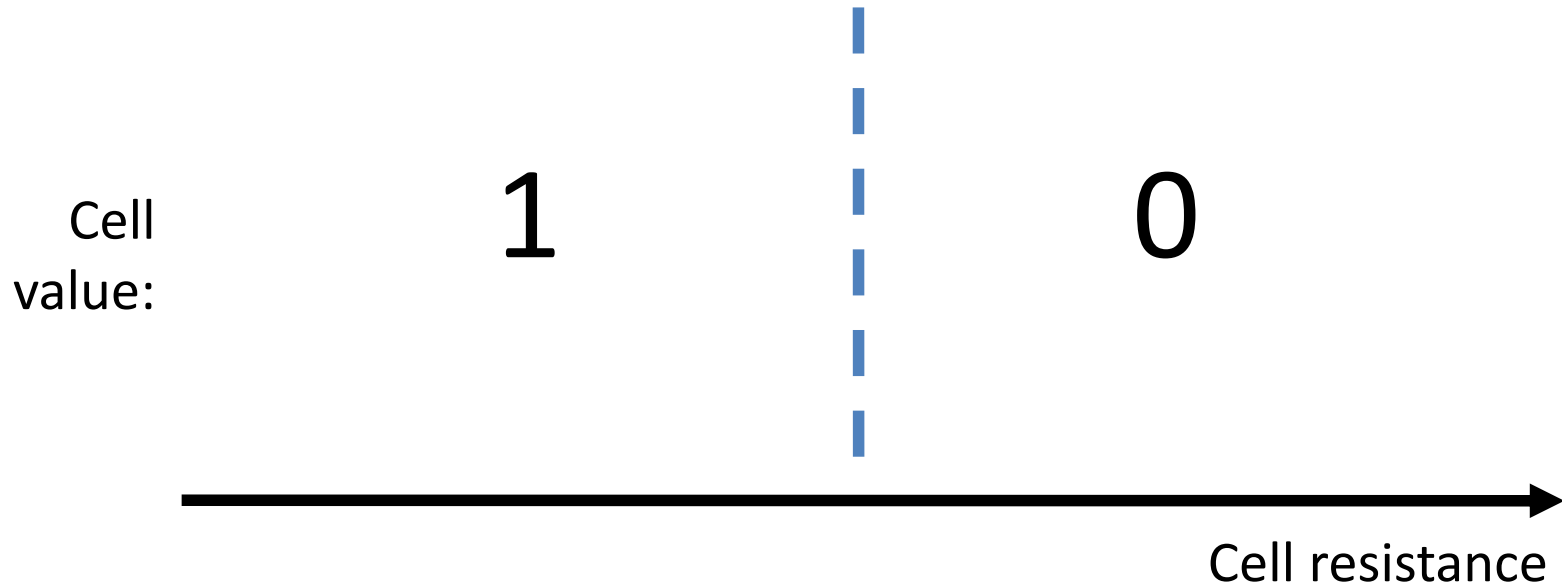
Cell resistance

Multi-Level Cell PCM

- Multi-level cell: more than 1 bit per cell
  - Further increases density by 2 to 4x [Lee+,ISCA'09]

- But MLC-PCM also has drawbacks
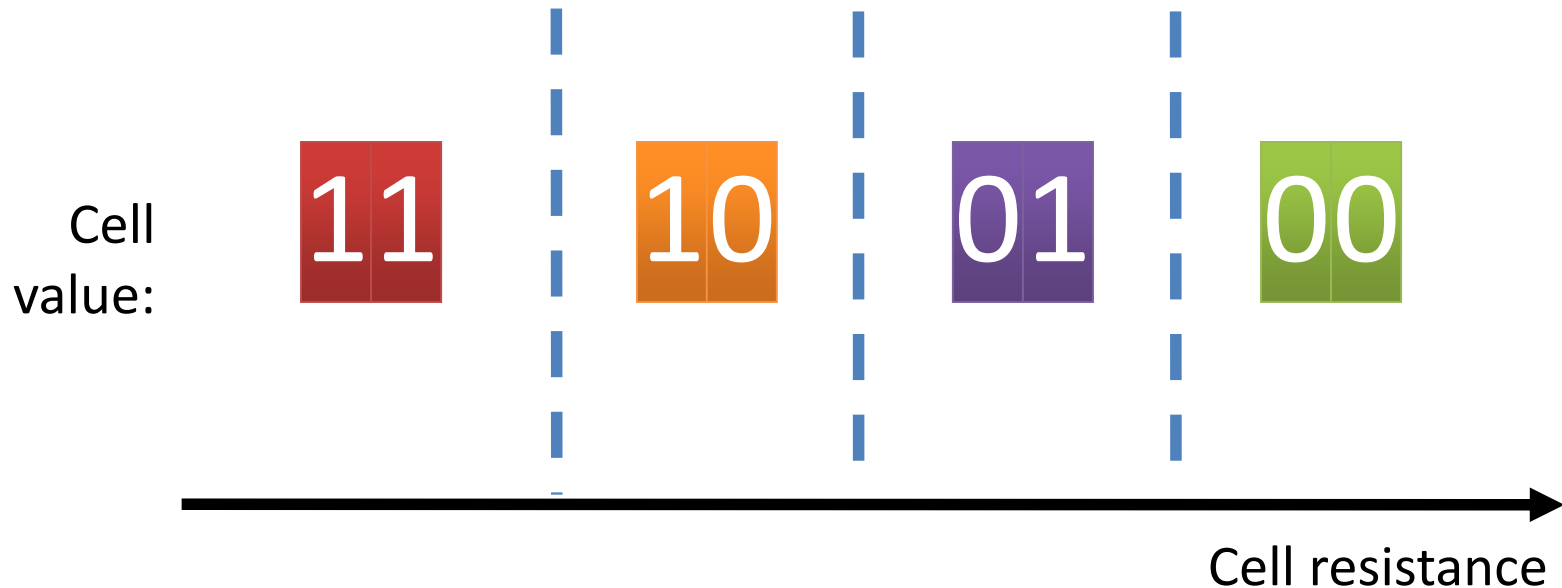 - Higher latency and energy than single-level cell PCM

MLC-PCM Resistance → Value

Bit 1   Bit 0

Cell value:

11   10   01   00

Cell resistance

MLC-PCM Resistance → Value

Less margin between values
→ need more precise sensing/modification of cell contents
→ higher latency/energy (~2x for reads and 4x for writes)

Cell value:

| 11 | 10 | 01 | 00 |

Cell resistance

Phase Change Memory Properties

- Surveyed prototypes from 2003-2008 (ITRS, IEDM, VLSI, ISSCC)
- Derived PCM parameters for F=90nm

- Lee, Ipek, Mutlu, Burger, "Architecting Phase Change Memory as a Scalable DRAM Alternative," ISCA 2009.
- Lee et al., "Phase Change Technology and the Future of Main Memory," IEEE Micro Top Picks 2010.
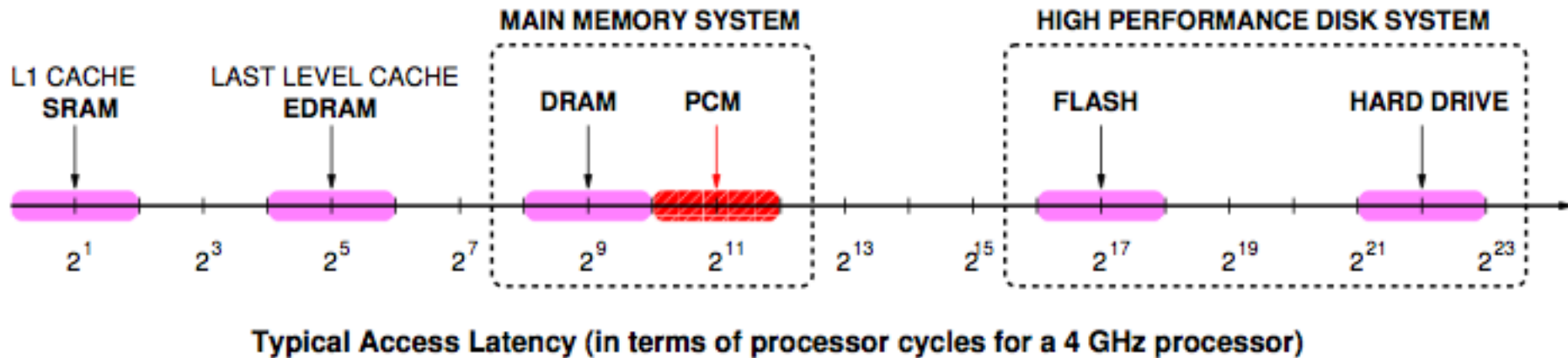
Table 1. Technology survey.

Parameter*		Published prototype								
	Horri[6]	Ahn[12]	Bedeschi[13]	Oh[14]	Pellizer[15]	Chen[5]	Kang[16]	Bedeschi[9]	Lee[10]	Lee[2]
Year	2003	2004	2004	2005	2006	2006	2006	2008	2008	**
Process, F (nm)	**	120	180	120	90	**	100	90	90	90
Array size (Mbytes)	**	64	8	64	**	**	256	256	512	**
Material	GST, N-d	GST, N-d	GST	GST	GST	GS, N-d	GST	GST	GST	GST, N-d
Cell size (μm^2)	**	0.290	0.290	**	0.097	60 nm^2	0.166	0.097	0.047	0.065 to 0.097
Cell size, F^2	**	20.1	9.0	**	12.0	**	16.6	12.0	5.8	9.0 to 12.0
Access device	**	**	BJT	FET	BJT	**	FET	BJT	Diode	BJT
Read time (ns)	**	70	48	68	**	**	62	**	55	48
Read current (μA)	**	**	40	**	**	**	**	**	**	40
Read voltage (V)	**	3.0	1.0	1.8	1.6	**	1.8	**	1.8	1.0
Read power (μW)	**	**	40	**	**	**	**	**	**	40
Read energy (pJ)	**	**	2.0	**	**	**	**	**	**	2.0
Set time (ns)	100	150	150	180	**	80	300	**	400	150
Set current (μA)	200	**	300	200	**	55	**	**	**	150
Set voltage (V)	**	**	2.0	**	**	1.25	**	**	**	1.2
Set power (μW)	**	**	300	**	**	34.4	**	**	**	90
Set energy (pJ)	**	**	45	**	**	2.8	**	**	**	13.5
Reset time (ns)	50	10	40	10	**	60	50	**	50	40
Reset current (μA)	600	600	600	600	400	90	600	300	600	300
Reset voltage (V)	**	**	2.7	**	1.8	1.6	**	1.6	**	1.6
Reset power (μW)	**	**	1620	**	**	80.4	**	**	**	480
Reset energy (pJ)	**	**	64.8	**	**	4.8	**	**	**	19.2
Write endurance (MLC)	10^7	10^9	10^6	**	10^8	10^4	**	10^5	10^5	10^8

* BJT: bipolar junction transistor; FET: field-effect transistor; GST: $Ge_2Sb_2Te_5$; MLC: multilevel cells; N-d: nitrogen doped.
** This information is not available in the publication cited.

Phase Change Memory Properties: Latency

- Latency comparable to, but slower than DRAM

MAIN MEMORY SYSTEM

HIGH PERFORMANCE DISK SYSTEM

L1 CACHE
SRAM

LAST LEVEL CACHE
EDRAM

DRAM   PCM

FLASH

HARD DRIVE

2^1 2^3 2^5 2^7 2^9 2^{11} 2^{13} 2^{15} 2^{17} 2^{19} 2^{21} 2^{23}

Typical Access Latency (in terms of processor cycles for a 4 GHz processor)

- Read Latency
  - 50ns: 4x DRAM, 10^{-3}x NAND Flash
- Write Latency
  - 150ns: 12x DRAM
- Write Bandwidth
  - 5-10 MB/s: 0.1x DRAM, 1x NAND Flash

Qureshi+, "Scalable high performance main memory system using phase-change memory technology," ISCA 2009.

Phase Change Memory Properties

- **Dynamic Energy**
  - 40 uA Rd, 150 uA Wr
  - 2-43x DRAM, 1x NAND Flash

- **Endurance**
  - Writes induce phase change at 650C
  - Contacts degrade from thermal expansion/contraction
  - 10^8 writes per cell
  - 10^{-8}x DRAM, 10^3x NAND Flash

- **Cell Size**
  - 9-12F^2 using BJT, single-level cells
  - 1.5x DRAM, 2-3x NAND   (will scale with feature size, MLC)

Phase Change Memory: Pros and Cons

- Pros over DRAM
  - Better technology scaling (capacity and cost)
  - Non volatile → Persistent
  - Low idle power (no refresh)

- Cons
  - Higher latencies: ~4-15x DRAM (especially write)
  - Higher active energy: ~2-50x DRAM (especially write)
  - Lower endurance (a cell dies after ~10^8 writes)
  - Reliability issues (resistance drift)

- Challenges in enabling PCM as DRAM replacement/helper:
  - Mitigate PCM shortcomings
  - Find the right way to place PCM in the system

PCM-based Main Memory (I)

- How should PCM-based (main) memory be organized?
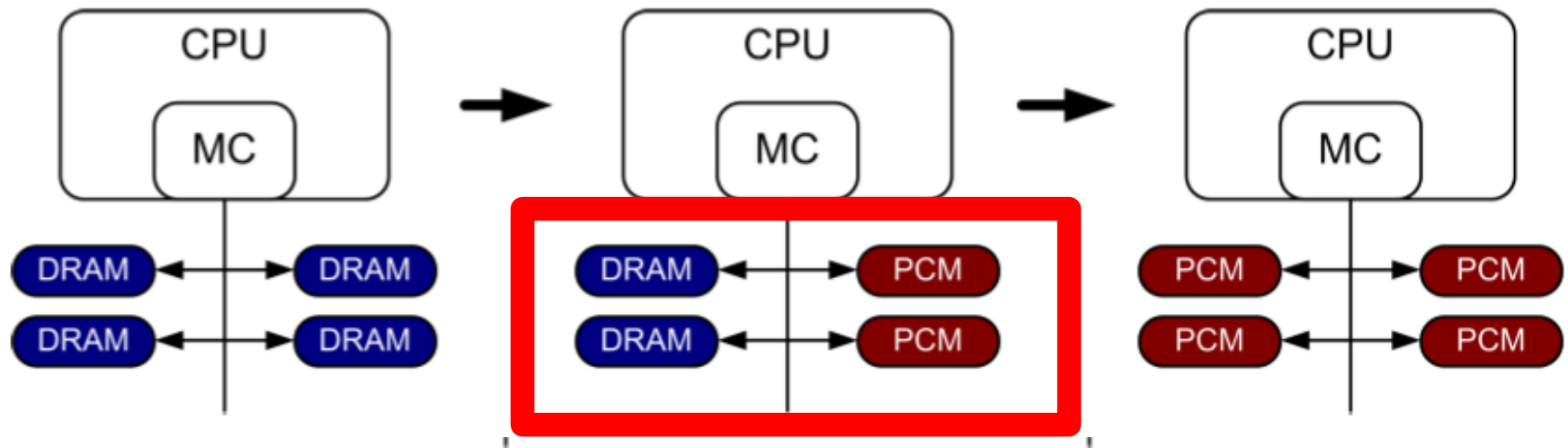
- Hybrid PCM+DRAM [Qureshi+ ISCA'09, Dhiman+ DAC'09]:
  - How to partition/migrate data between PCM and DRAM

PCM-based Main Memory (II)

- How should PCM-based (main) memory be organized?
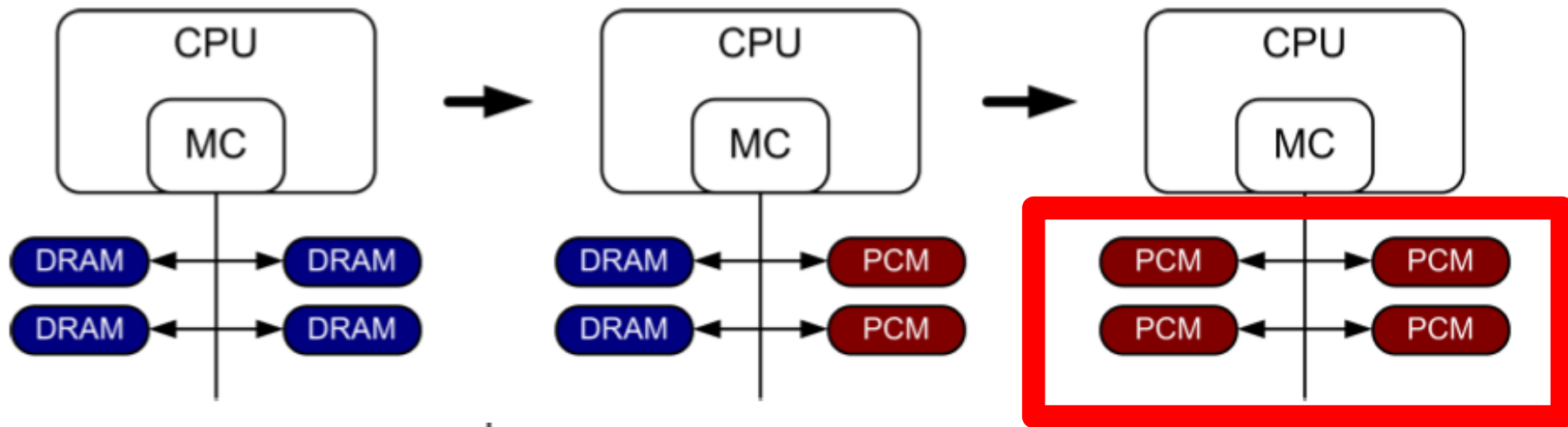
- Pure PCM main memory [Lee et al., ISCA'09, Top Picks'10]:
  - How to redesign entire hierarchy (and cores) to overcome PCM shortcomings

An Initial Study: Replace DRAM with PCM

- Lee, Ipek, Mutlu, Burger, "Architecting Phase Change Memory as a Scalable DRAM Alternative," ISCA 2009.
  - Surveyed prototypes from 2003-2008 (e.g. IEDM, VLSI, ISSCC)
  - Derived "average" PCM parameters for F=90nm

Density
  ▷ 9 - 12F^2 using BJT
  ▷ 1.5× DRAM

Latency
  ▷ 50ns Rd, 150ns Wr
  ▷ 4×, 12× DRAM

Endurance
  ▷ 1E+08 writes
  ▷ 1E-08× DRAM

Energy
  ▷ 40μA Rd, 150μA Wr
  ▷ 2×, 43× DRAM

SAFARI

Results: Naïve Replacement of DRAM with PCM

- Replace DRAM with PCM in a 4-core, 4MB L2 system
- PCM organized the same as DRAM: row buffers, banks, peripherals
- 1.6x delay, 2.2x energy, 500-hour average lifetime
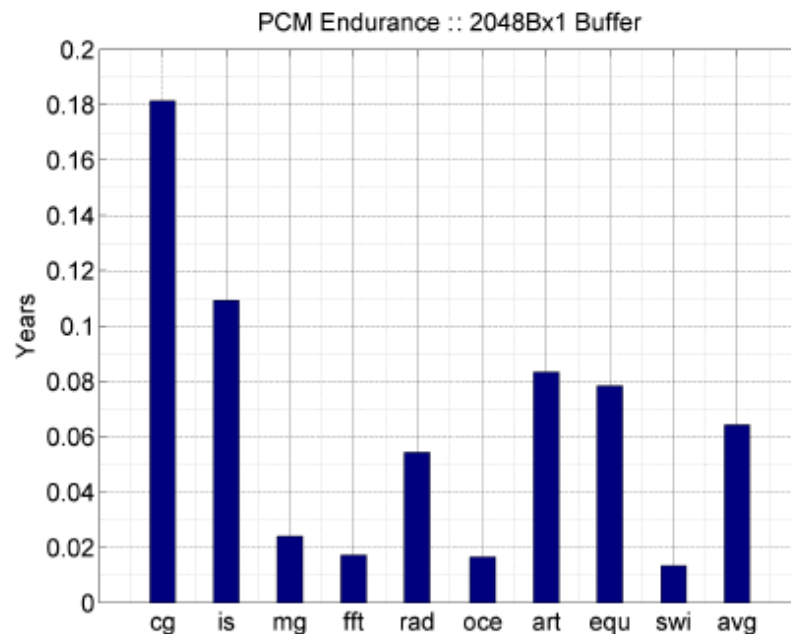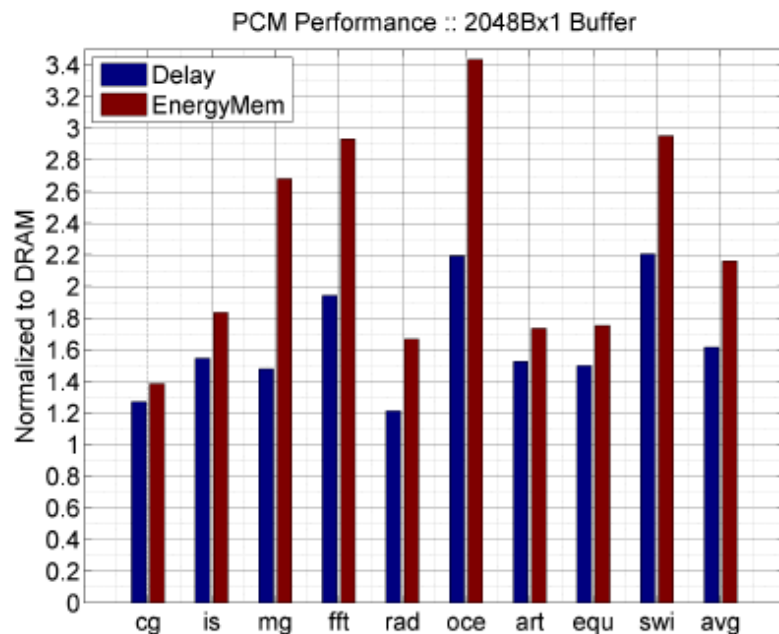
- Lee, Ipek, Mutlu, Burger, "Architecting Phase Change Memory as a Scalable DRAM Alternative," ISCA 2009.

Architecting PCM to Mitigate Shortcomings

- Idea 1: Use multiple narrow row buffers in each PCM chip
  → Reduces array reads/writes → better endurance, latency, energy

- Idea 2: Write into array at
  cache block or word
  granularity
  → Reduces unnecessary wear

DRAM
data array

PCM
data array

sense amplifiers
(buffer)

I/O

sense amplifiers

latches
(buffer)

I/O
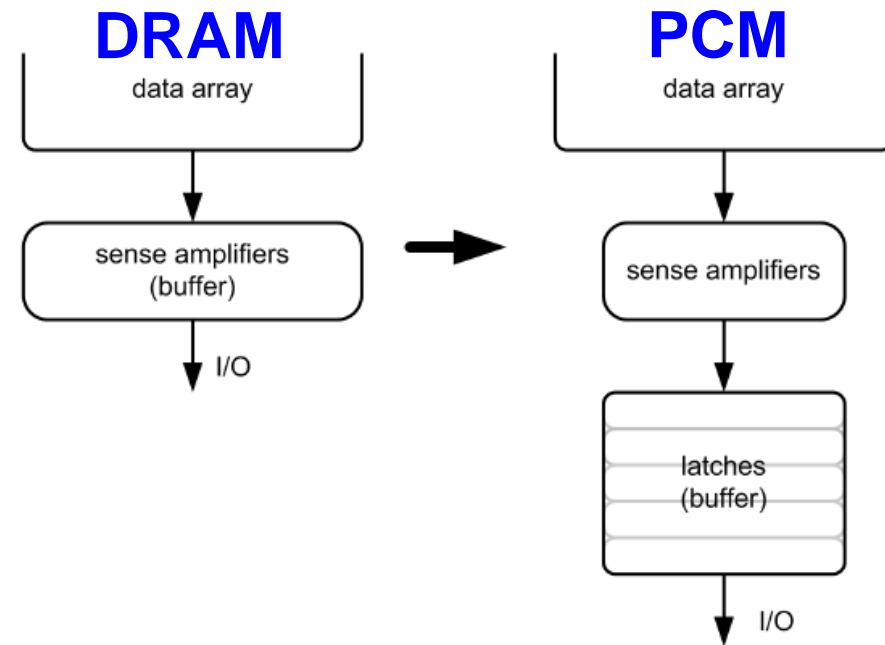
Results: Architected PCM as Main Memory

- **1.2x delay, 1.0x energy, 5.6-year average lifetime**
- Scaling improves energy, endurance, density
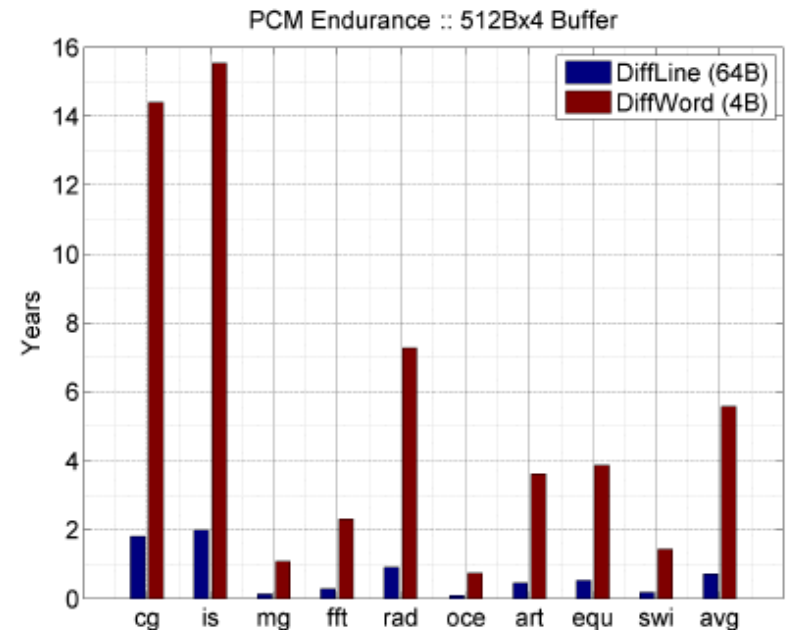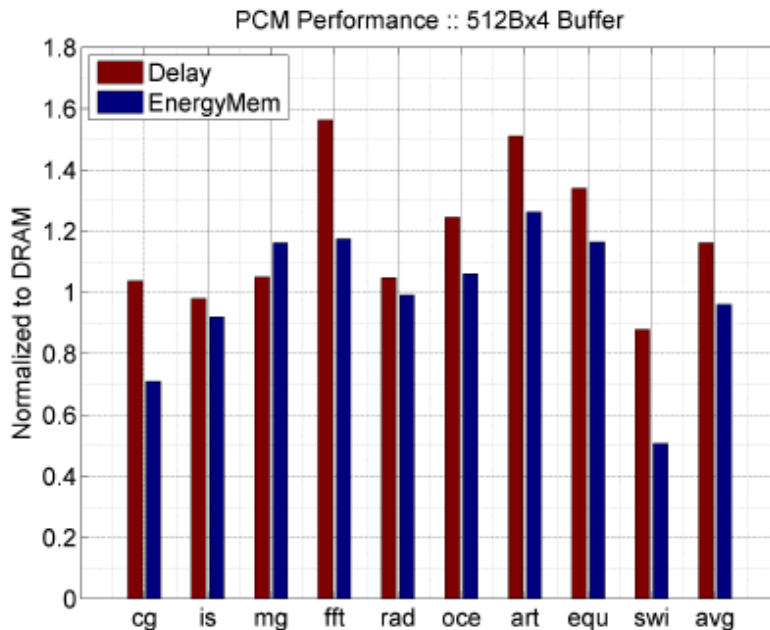
- Caveat 1: Worst-case lifetime is much shorter (no guarantees)
- Caveat 2: Intensive applications see large performance and energy hits
- Caveat 3: Optimistic PCM parameters?

PCM As Main Memory

- Benjamin C. Lee, Engin Ipek, Onur Mutlu, and Doug Burger,
  "Architecting Phase Change Memory as a Scalable DRAM Alternative"
  Proceedings of the 36th International Symposium on Computer Architecture (**ISCA**), pages 2-13, Austin, TX, June 2009. Slides (pdf)
  One of the 13 computer architecture papers of 2009 selected as Top Picks by IEEE Micro.
  Selected as a CACM Research Highlight.

Architecting Phase Change Memory as a Scalable DRAM Alternative

Benjamin C. Lee†   Engin Ipek†   Onur Mutlu‡   Doug Burger†

†Computer Architecture Group
Microsoft Research
Redmond, WA
{blee, ipek, dburger}@microsoft.com

‡Computer Architecture Laboratory
Carnegie Mellon University
Pittsburgh, PA
onur@cmu.edu

More on PCM As Main Memory (II)

- Benjamin C. Lee, Ping Zhou, Jun Yang, Youtao Zhang, Bo Zhao, Engin Ipek, Onur Mutlu, and Doug Burger,
"Phase Change Technology and the Future of Main Memory"
IEEE Micro, Special Issue: Micro's Top Picks from 2009 Computer Architecture Conferences (**MICRO TOP PICKS**), Vol. 30, No. 1, pages 60-70, January/February 2010.

PHASE-CHANGE TECHNOLOGY AND THE FUTURE OF MAIN MEMORY

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Intel Optane Memory (Idea Realized in 2019)

- Non-volatile main memory
- Based on 3D-XPoint Technology

SAFARI https://www.storagereview.com/intel_optane_dc_persistent_memory_module_pmm

More on PCM Based Main Memory

- HanBin Yoon, Justin Meza, Naveen Muralimanohar, Norman P. Jouppi, and Onur Mutlu,
  "Efficient Data Mapping and Buffering Techniques for Multi-Level Cell Phase-Change Memories"
  ACM Transactions on Architecture and Code Optimization (**TACO**), Vol. 11, No. 4, December 2014. [Slides (ppt) (pdf)]
  Presented at the 10th HiPEAC Conference, Amsterdam, Netherlands, January 2015. [Slides (ppt) (pdf)]
  Best (student) presentation award.

Efficient Data Mapping and Buffering Techniques for Multilevel Cell Phase-Change Memories

HANBIN YOON[*] and JUSTIN MEZA, Carnegie Mellon University
NAVEEN MURALIMANOHAR, Hewlett-Packard Labs
NORMAN P. JOUPPI[**], Google Inc.
ONUR MUTLU, Carnegie Mellon University
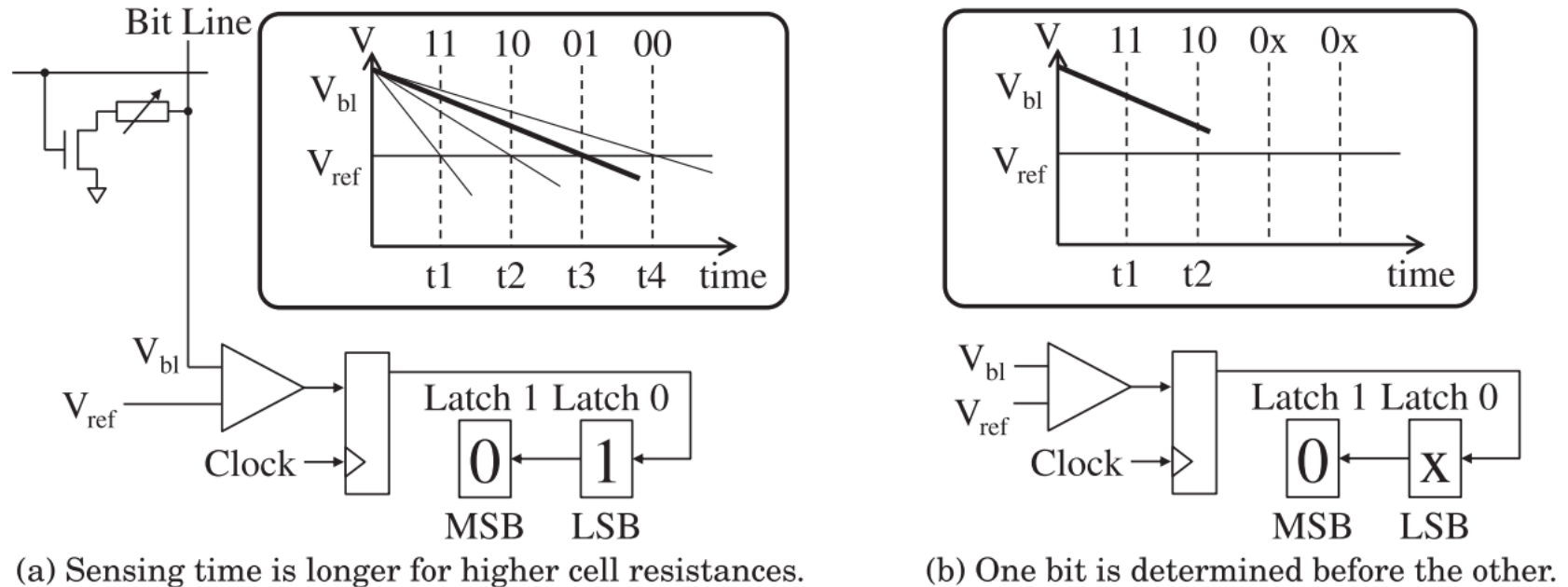
Some PCM Bits Take Longer to Read…

(a) Sensing time is longer for higher cell resistances.

(b) One bit is determined before the other.

Fig. 3.   MLC PCM cell read operation [Qureshi et al. 2010b].

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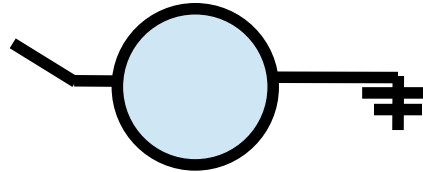# Observation 1: Read Asymmetry

- *The <u>read</u> latency/energy of Bit 1 is lower than that of Bit 0*

- This is due to how MLC-PCM cells are read

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Observation 1: Read Asymmetry
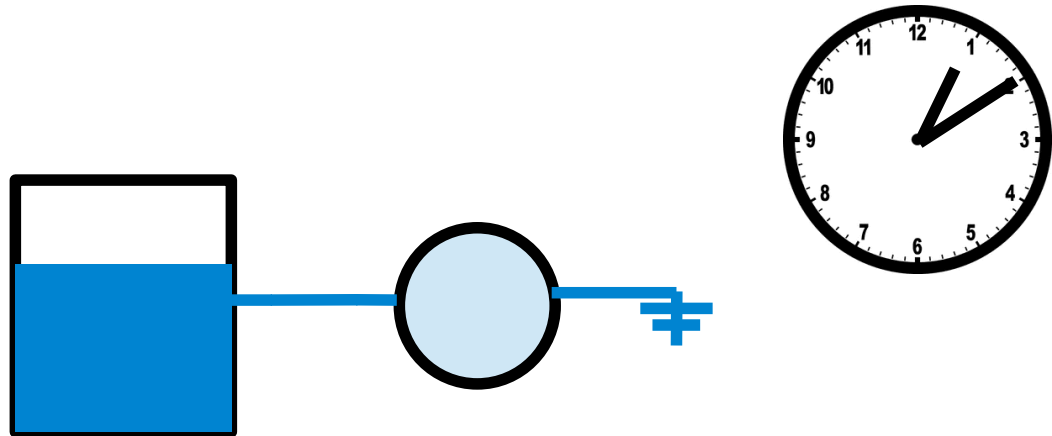
Simplified example
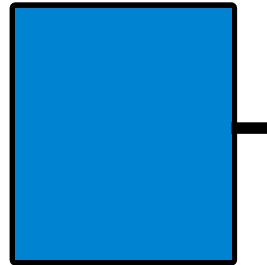
Capacitor filled
with reference
voltage

MLC-PCM cell
with unknown
resistance

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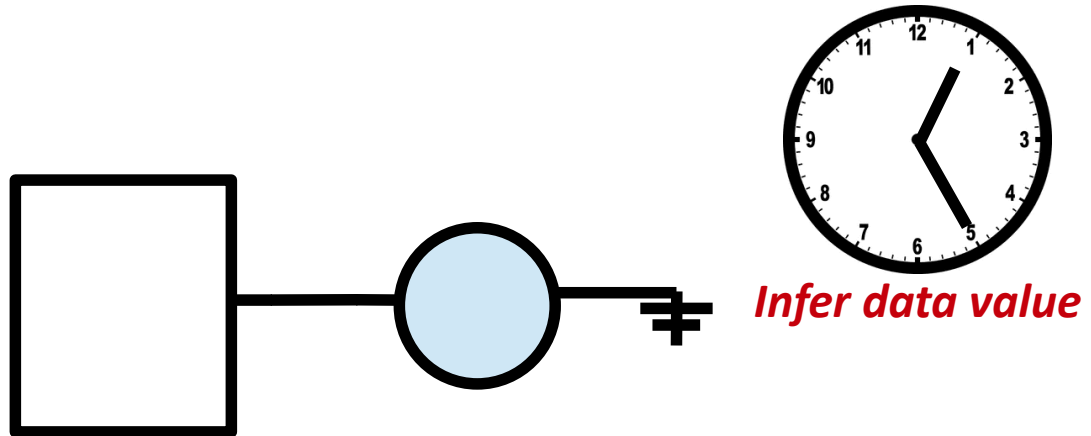
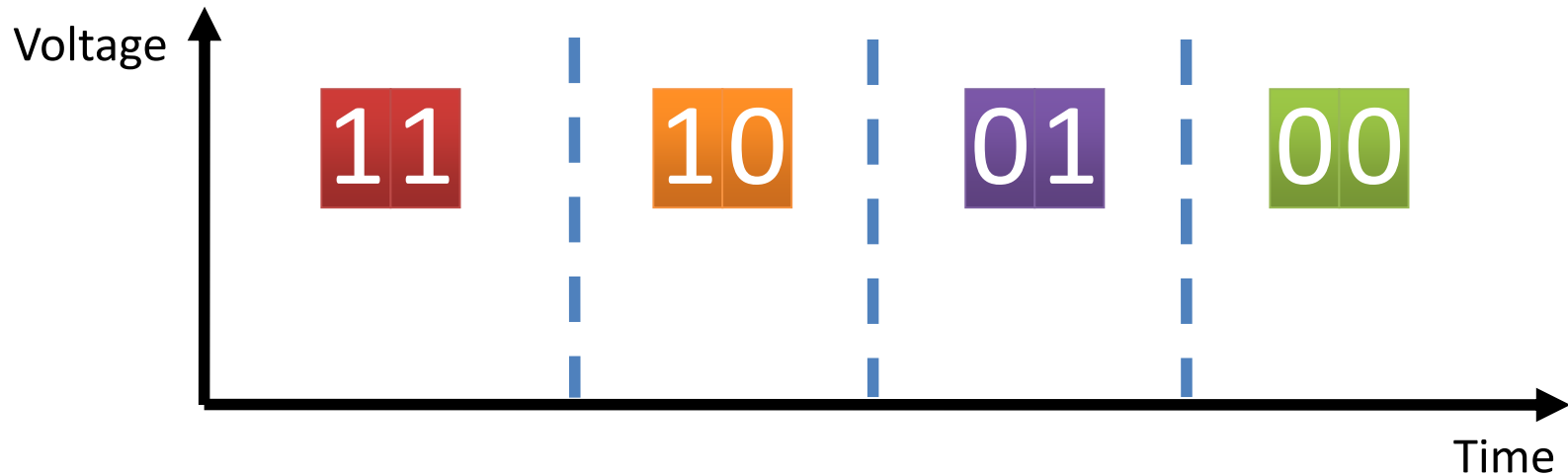# Observation 1: Read Asymmetry

Simplified example

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Observation 1: Read Asymmetry

Simplified example

Infer data value

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Observation 1: Read Asymmetry

Voltage

Time

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Observation 1: Read Asymmetry

Observation 1: Read Asymmetry

Initial voltage (fully charged capacitor)

Voltage

11 10 01 00

Time

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Observation 1: Read Asymmetry

PCM cell connected → draining capacitor

Voltage

11 10 01 00

Time

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Observation 1: Read Asymmetry

Capacitor drained → data value known (01)

Voltage

11　10　01　00

Time

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40

Observation 1: Read Asymmetry

- In existing devices
  - Both MLC bits are read at the same time
  - Must wait *maximum time* to read both bits

- However, *we can infer information about Bit 1 before this time*

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Observation 1: Read Asymmetry

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Observation 1: Read Asymmetry
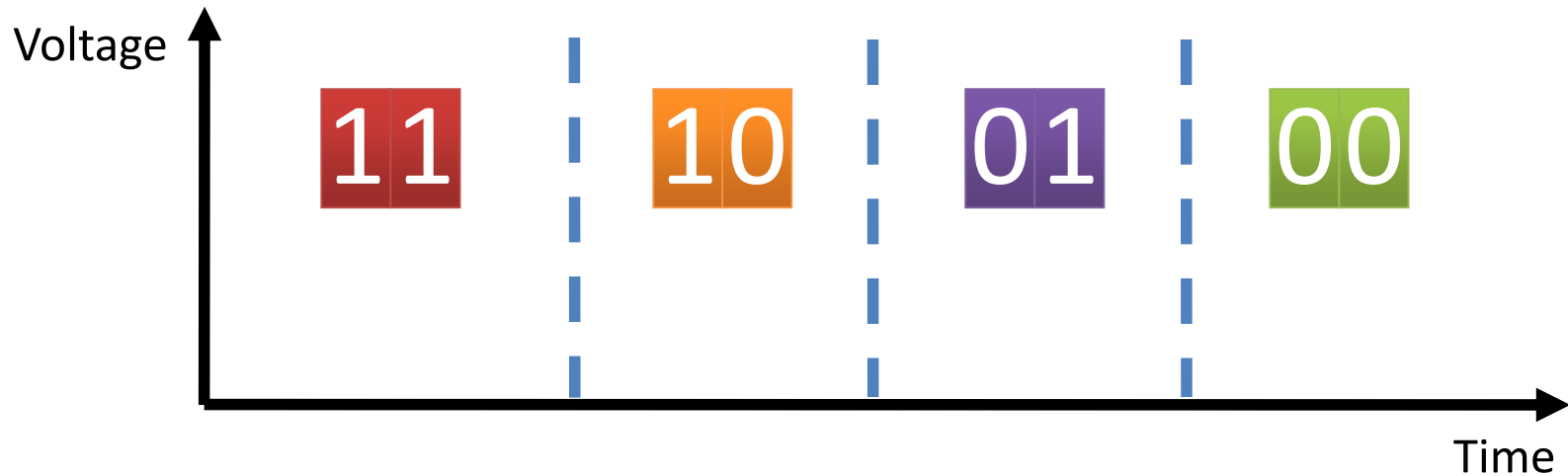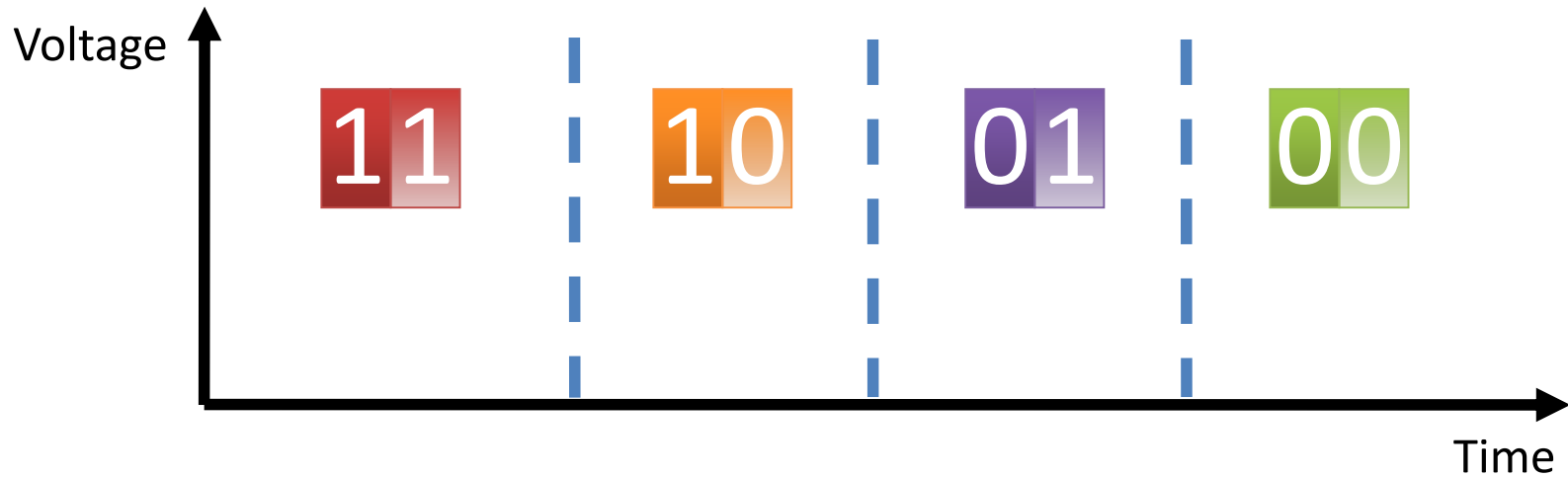
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Observation 1: Read Asymmetry

Time to determine Bit 1's value

Voltage

11 10 01 00

Time

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44

Observation 1: Read Asymmetry

Time to determine Bit 0's value

Voltage

11 10 01 00

Time

SAFARI

45

Some PCM Bits Take Longer to Write…

Efficient Data Mapping and Buffering Techniques for MLC PCM   40:7

(a) All possible cell state transitions.

(b) Cell state transitions when modifying only the MSB *or* the LSB.

Fig. 4.   MLC PCM cell write latencies [Joshi et al. 2011; Nirschl et al. 2007; Happ et al. 2006].

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More on PCM Latencies and Exploiting Them
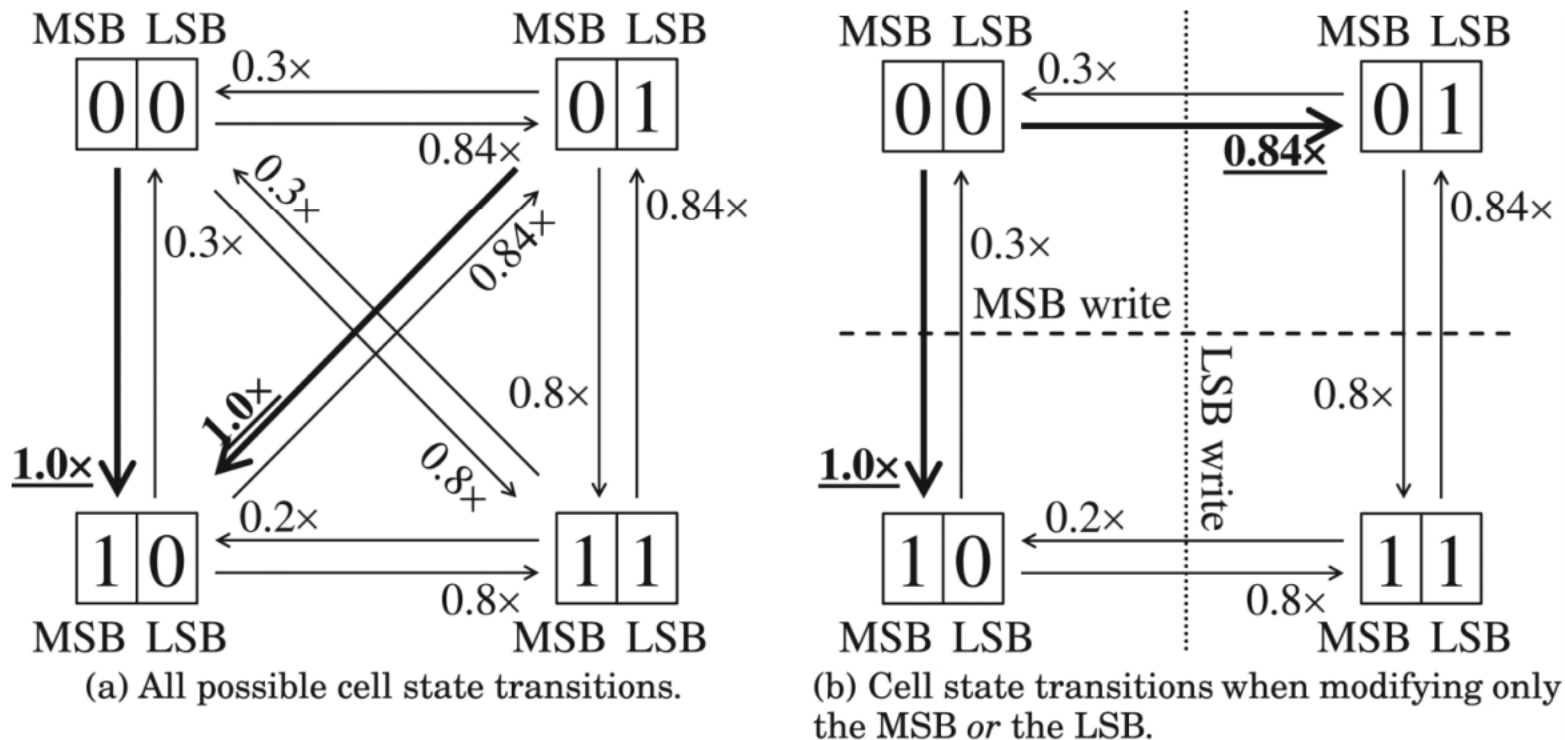
HanBin Yoon, Justin Meza, Naveen Muralimanohar, Norman P. Jouppi, and Onur Mutlu,
"Efficient Data Mapping and Buffering Techniques for Multi-Level Cell Phase-Change Memories"
ACM Transactions on Architecture and Code Optimization (**TACO**), Vol. 11, No. 4, December 2014. [Slides (ppt) (pdf)]
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Best (student) presentation award.

Efficient Data Mapping and Buffering Techniques for Multilevel Cell Phase-Change Memories

HANBIN YOON[*] and JUSTIN MEZA, Carnegie Mellon University
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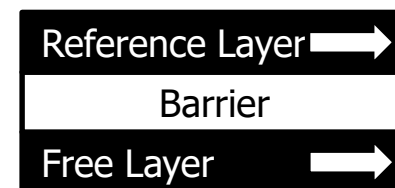NORMAN P. JOUPPI[**], Google Inc.
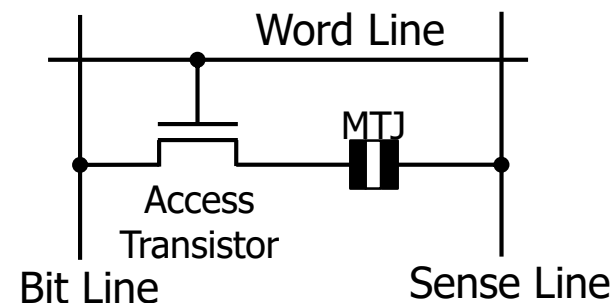ONUR MUTLU, Carnegie Mellon University

STT-RAM as Main Memory

STT-MRAM as Main Memory

- Magnetic Tunnel Junction (MTJ) device
  - Reference layer: Fixed magnetic orientation
  - Free layer: Parallel or anti-parallel

- Magnetic orientation of the free layer determines logical state of device
  - High vs. low resistance

- Write: Push large current through MTJ to change orientation of free layer

- Read: Sense current flow

- Kultursay et al., "Evaluating STT-RAM as an Energy-Efficient Main Memory Alternative," ISPASS 2013.

Logical 0

Reference Layer	→
Barrier	
Free Layer	→

Logical 1

Reference Layer	→
Barrier	
Free Layer	←

Word Line

MTJ

Access Transistor

Bit Line   Sense Line

STT-MRAM: Pros and Cons

- Pros over DRAM
  - Better technology scaling (capacity and cost)
  - Non volatile → Persistent
  - Low idle power (no refresh)

- Cons
  - Higher write latency
  - Higher write energy
  - Poor density (currently)
  - Reliability?

- Another level of freedom
  - Can trade off non-volatility for lower write latency/energy (by reducing the size of the MTJ)

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Architected STT-MRAM as Main Memory

- 4-core, 4GB main memory, multiprogrammed workloads
- ~6% performance loss, ~60% energy savings vs. DRAM
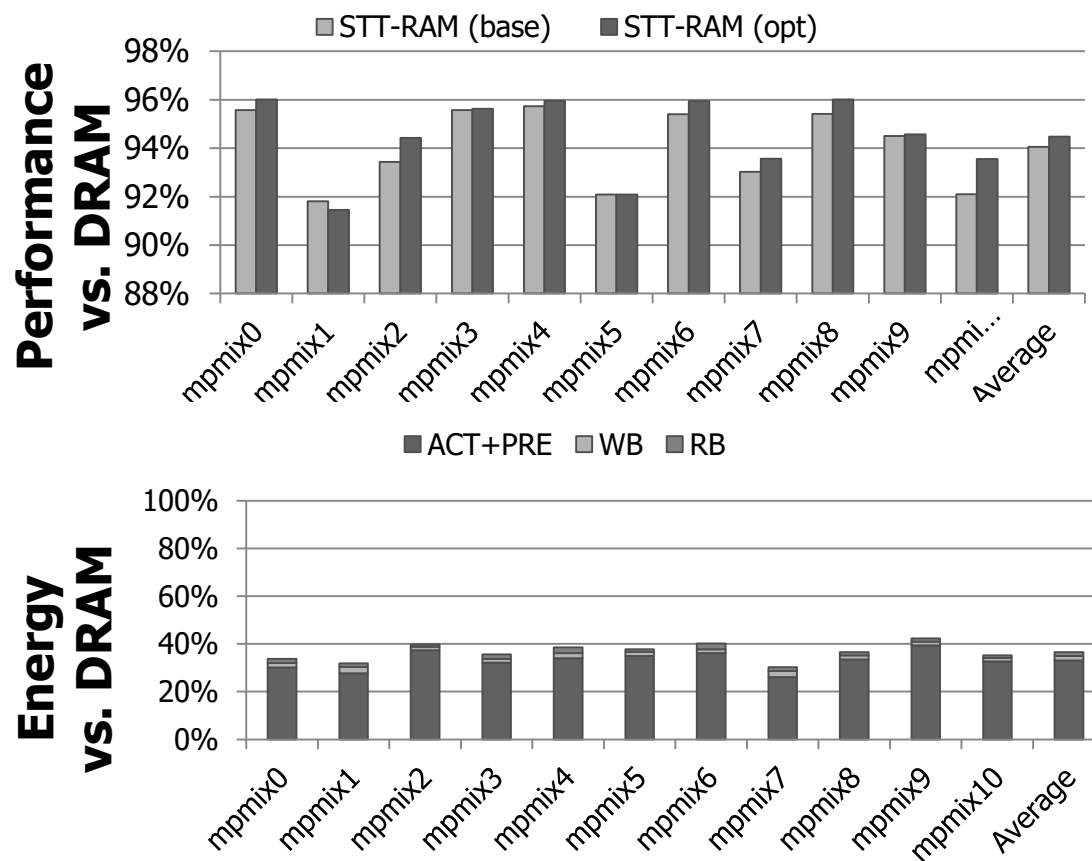
Kultursay+, "Evaluating STT-RAM as an Energy-Efficient Main Memory Alternative," ISPASS 2013.

More on STT-MRAM as Main Memory

- Emre Kultursay, Mahmut Kandemir, Anand Sivasubramaniam, and Onur Mutlu,
"Evaluating STT-RAM as an Energy-Efficient Main Memory Alternative"
Proceedings of the 2013 IEEE International Symposium on Performance Analysis of Systems and Software (**ISPASS**), Austin, TX, April 2013. Slides (pptx) (pdf)
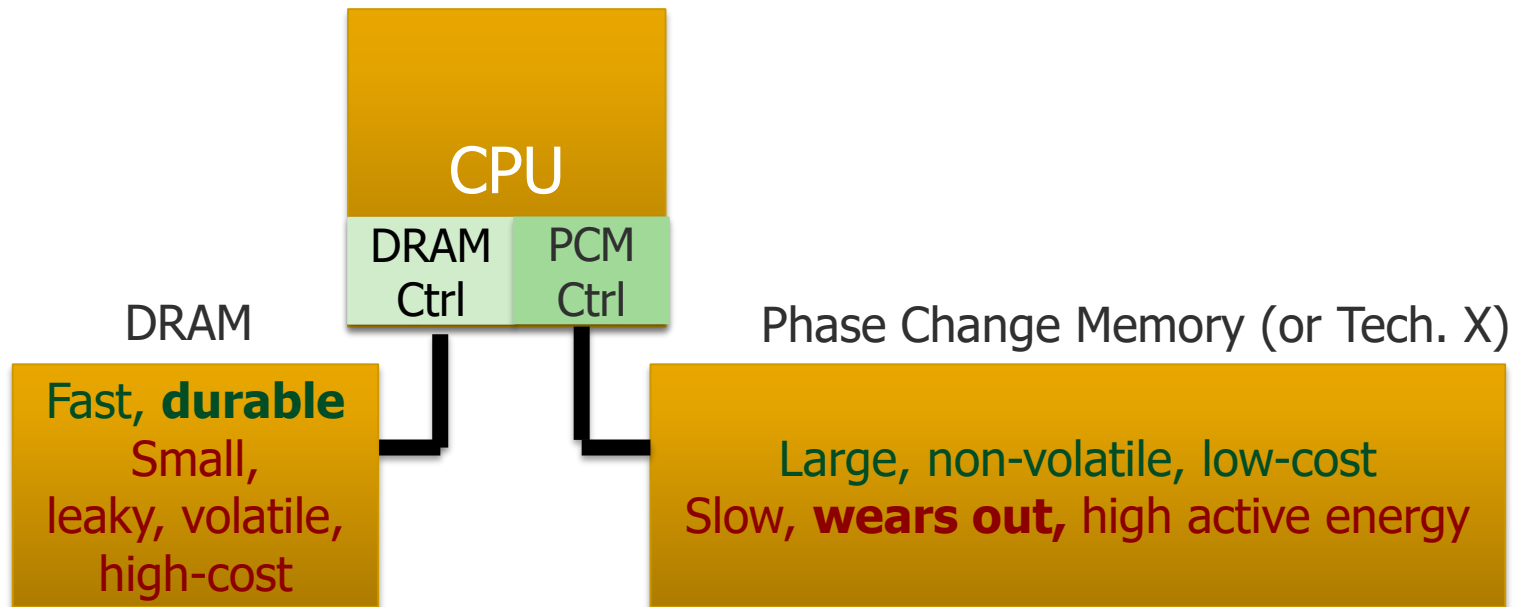
Evaluating STT-RAM as an Energy-Efficient Main Memory Alternative

Emre Kültürsay*, Mahmut Kandemir*, Anand Sivasubramaniam*, and Onur Mutlu†
*The Pennsylvania State University and †Carnegie Mellon University

Hybrid Main Memory

A More Viable Approach: Hybrid Memory Systems

CPU

DRAM Ctrl   PCM Ctrl

DRAM

Fast, **durable**
Small,
leaky, volatile,
high-cost

Phase Change Memory (or Tech. X)

Large, non-volatile, low-cost
Slow, **wears out,** high active energy

Hardware/software manage data allocation and movement
to achieve the best of multiple technologies

Meza+, "Enabling Efficient and Scalable Hybrid Memories," IEEE Comp. Arch. Letters, 2012.
Yoon+, "Row Buffer Locality Aware Caching Policies for Hybrid Memories," ICCD 2012 Best
Paper Award.

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Providing the Best of Multiple Metrics

with

Multiple Memory Technologies

Heterogeneous, Configurable, Programmable Memory Systems
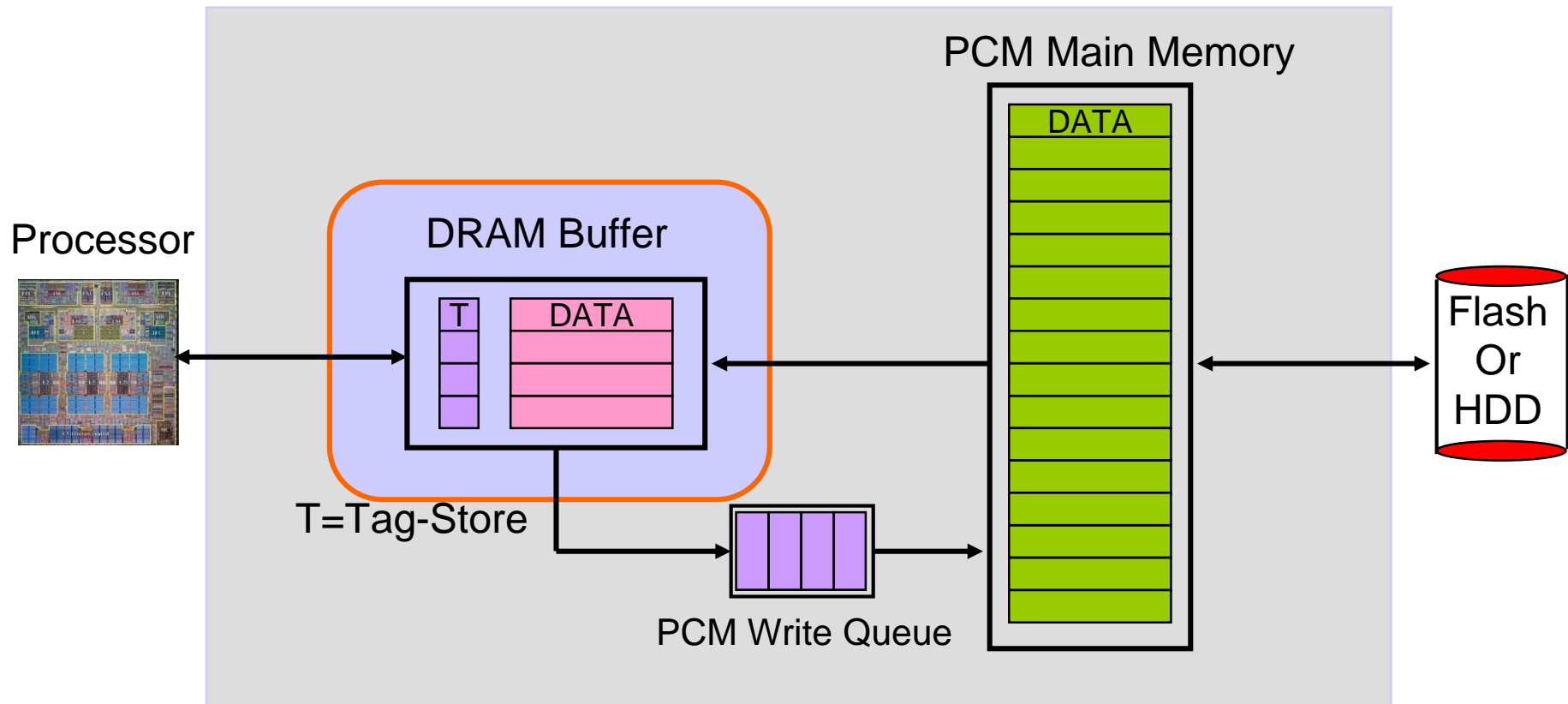
Hybrid Memory Systems: Issues

- Cache vs. Main Memory

- Granularity of Data Move/Manage-ment: Fine or Coarse

- Hardware vs. Software vs. HW/SW Cooperative

- When to migrate data?

- How to design a scalable and efficient large cache?

- ...

One Option: DRAM as a Cache for PCM

- PCM is main memory; DRAM caches memory rows/blocks
  - Benefits: Reduced latency on DRAM cache hit; write filtering
- Memory controller hardware manages the DRAM cache
  - Benefit: Eliminates system software overhead

- Three issues:
  - What data should be placed in DRAM versus kept in PCM?
  - What is the granularity of data movement?
  - How to design a low-cost hardware-managed DRAM cache?

- Two idea directions:
  - Locality-aware data placement **[Yoon+ , ICCD 2012]**
  - Cheap tag stores and dynamic granularity **[Meza+, IEEE CAL 2012]**

DRAM as a Cache for PCM

- Goal: Achieve the best of both DRAM and PCM/NVM
  - Minimize amount of DRAM w/o sacrificing performance, endurance
  - DRAM as cache to tolerate PCM latency and write bandwidth
  - PCM as main memory to provide large capacity at good cost and power

Qureshi+, "Scalable high performance main memory system using phase-change memory technology," ISCA 2009.

Write Filtering Techniques

- Lazy Write: Pages from disk installed only in DRAM, not PCM
- Partial Writes: Only dirty lines from DRAM page written back
- Page Bypass: Discard pages with poor reuse on DRAM eviction
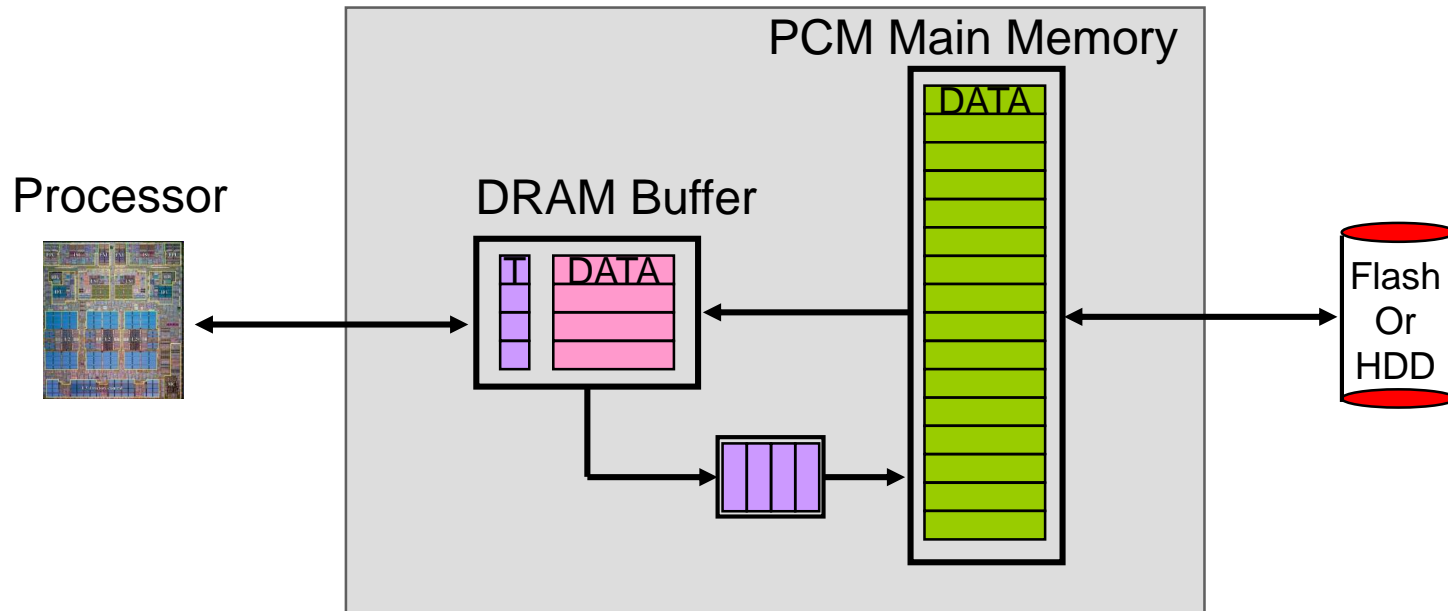
- Qureshi et al., "Scalable high performance main memory system using phase-change memory technology," ISCA 2009.

Results: DRAM as PCM Cache (I)

- Simulation of 16-core system, 8GB DRAM main-memory at 320 cycles, HDD (2 ms) with Flash (32 us) with Flash hit-rate of 99%

- Assumption: PCM 4x denser, 4x slower than DRAM

- DRAM block size = PCM page size (4kB)

Qureshi+, "Scalable high performance main memory system using phase-change memory technology," ISCA 2009.
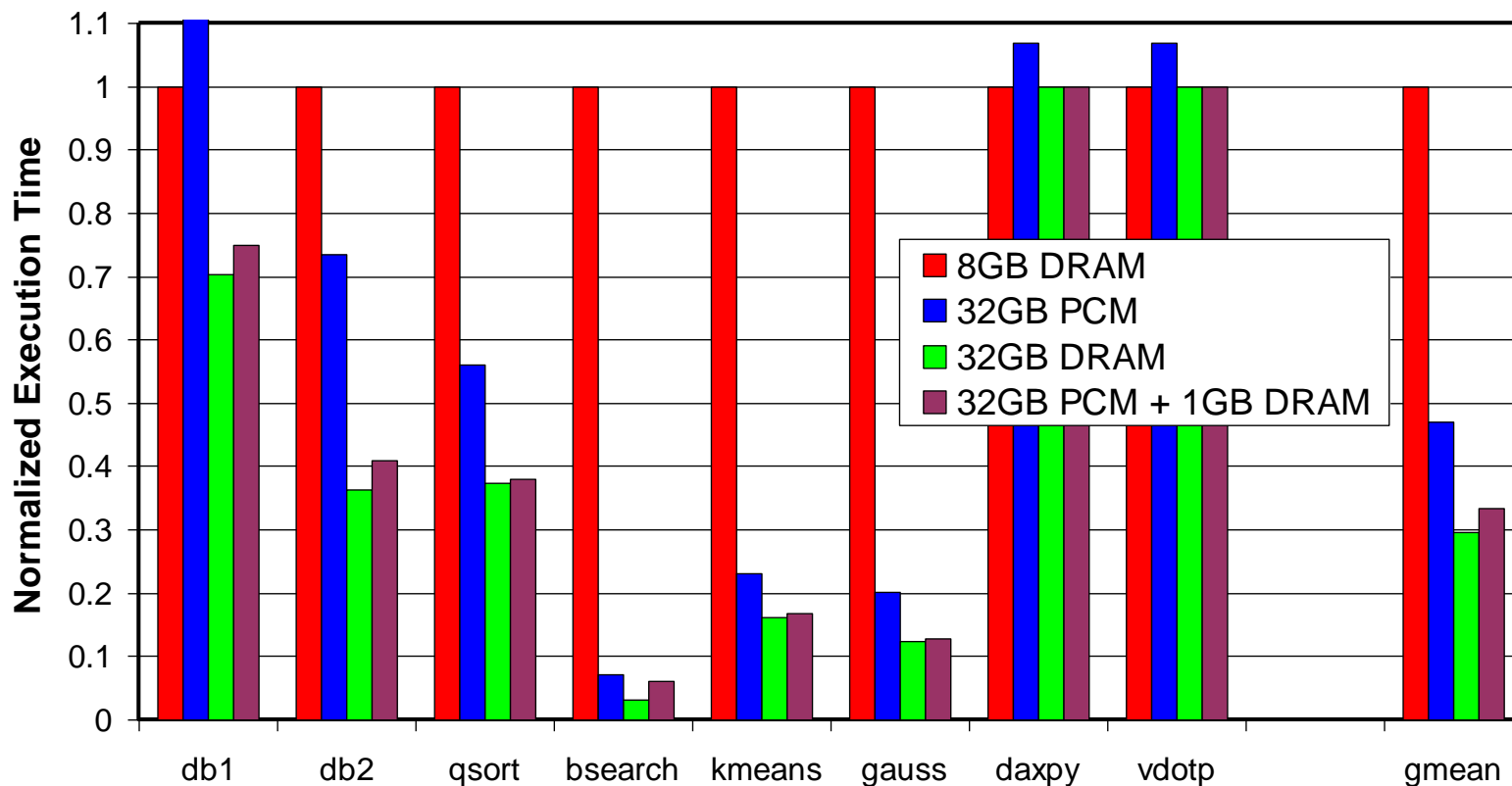
Results: DRAM as PCM Cache (II)

- PCM-DRAM Hybrid performs similarly to similar-size DRAM
- Significant energy savings with PCM-DRAM Hybrid
- Average lifetime: 9.7 years (no guarantees)

Legend:
- 8GB DRAM
- Hybrid (32GB PCM+ 1GB DRAM)
- 32GB DRAM

Qureshi+, "Scalable high performance main memory system using phase-change memory technology," ISCA 2009.
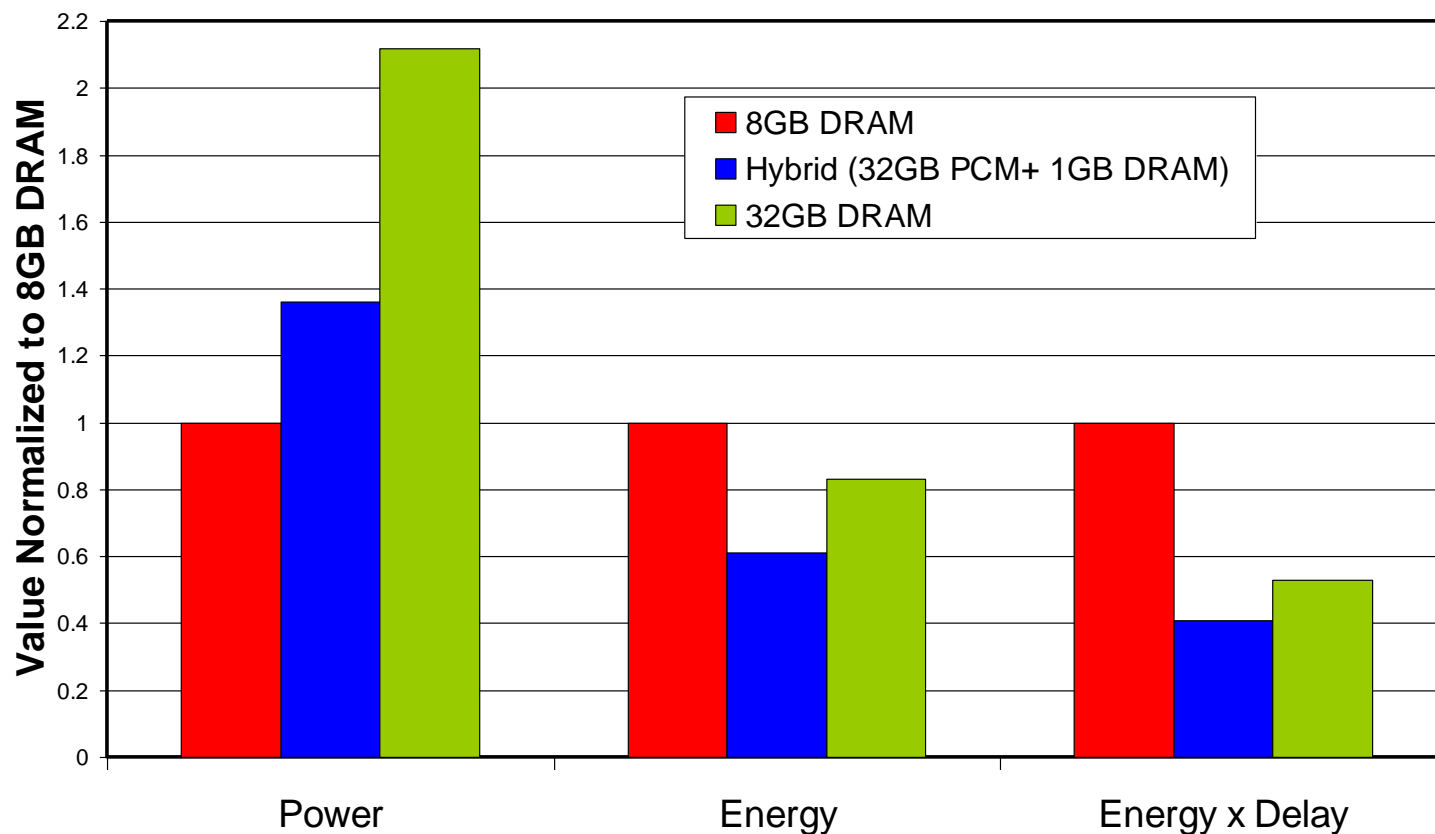
More on DRAM-PCM Hybrid Memory

- **Scalable High-Performance Main Memory System Using Phase-Change Memory Technology**.
Moinuddin K. Qureshi, Viji Srinivasan, and Jude A. Rivers
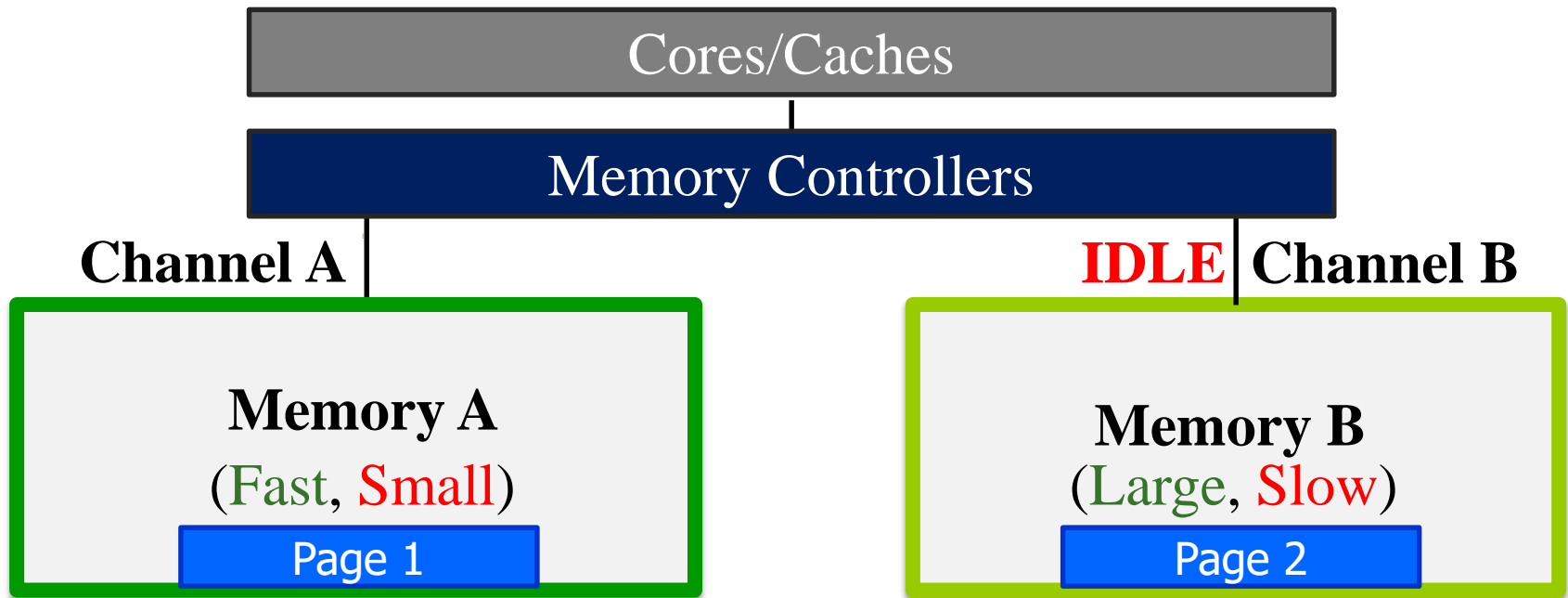*Appears in the International Symposium on Computer Architecture (ISCA) 2009*.

Scalable High Performance Main Memory System Using Phase-Change Memory Technology

Moinuddin K. Qureshi   Vijayalakshmi Srinivasan   Jude A. Rivers

IBM Research
T. J. Watson Research Center, Yorktown Heights NY 10598
{mkquresh, viji, jarivers}@us.ibm.com

Data Placement in Hybrid Memory

Cores/Caches

Memory Controllers

Channel A   **IDLE** **Channel B**

Memory A
(Fast, Small)
Page 1

Memory B
(Large, Slow)
Page 2

Which memory do we place each page in,
to **maximize system performance**?

- Memory A is fast, but small
- Load should be balanced on both channels?
- Page migrations have performance and energy overhead

Data Placement Between DRAM and PCM

- Idea: Characterize data access patterns and guide data placement in hybrid memory

- Streaming accesses: As fast in PCM as in DRAM

- Random accesses: Much faster in DRAM

- Idea: Place random access data with some reuse in DRAM; streaming data in PCM

- Yoon+, "Row Buffer Locality-Aware Data Placement in Hybrid Memories," ICCD 2012 Best Paper Award.

Key Observation & Idea

- Row buffers exist in both DRAM and PCM
  - Row hit latency **similar** in DRAM & PCM [Lee+ ISCA'09]
  - Row miss latency **small** in DRAM, **large** in PCM

- Place data in DRAM which
  - is likely to miss in the row buffer (low row buffer locality)→ miss penalty is smaller in DRAM

    AND

  - is reused many times → cache only the data worth the movement cost and DRAM space

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Hybrid vs. All-PCM/DRAM [ICCD'12]

31% better performance than all PCM, within 29% of all DRAM performance

Yoon+, "Row Buffer Locality-Aware Data Placement in Hybrid Memories," ICCD 2012 Best Paper Award.
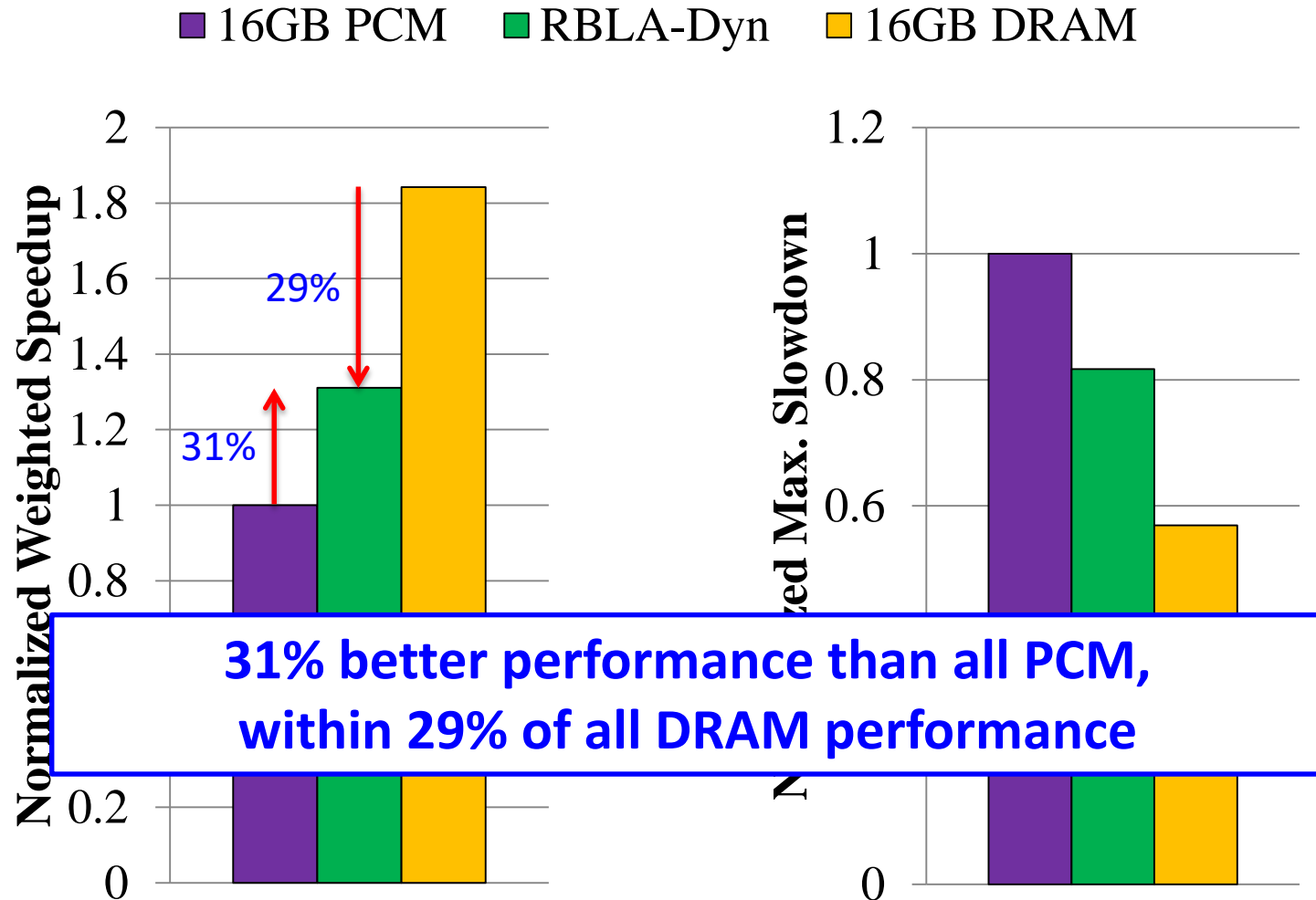
More on Hybrid Memory Data Placement

- HanBin Yoon, Justin Meza, Rachata Ausavarungnirun, Rachael Harding, and Onur Mutlu,
"Row Buffer Locality Aware Caching Policies for Hybrid Memories"
Proceedings of the 30th IEEE International Conference on Computer Design (**ICCD**), Montreal, Quebec, Canada, September 2012. Slides (pptx) (pdf)
Best paper award (in Computer Systems and Applications track).

Row Buffer Locality Aware Caching Policies for Hybrid Memories

HanBin Yoon, Justin Meza, Rachata Ausavarungnirun, Rachael A. Harding and Onur Mutlu
Carnegie Mellon University
{hanbinyoon,meza,rachata,onur}@cmu.edu, rhardin@mit.edu

Weaknesses of Existing Solutions

- They are all heuristics that consider only a **limited part** of **memory access behavior**

- **Do not *directly* capture the overall system performance impact** of data placement decisions

- Example: None capture **memory-level parallelism** (MLP)
  - Number of ***concurrent* memory requests** from the same application when a page is accessed
  - Affects how much page migration helps performance

Importance of Memory-Level Parallelism

Before migration:

requests to Page 1 — Mem. B

After migration:

requests to Page 1 — Mem. A

T

time

Migrating one page
reduces stall time by T

Before migration:

requests to Page 2 — Mem. B

requests to Page 3 — Mem. B

After migration:

requests to Page 2 — Mem. A

requests to Page 3 — Mem. B

time

Must migrate two pages
to reduce stall time by T:
migrating one page alone
does not help

Page migration decisions **need to consider MLP**

Our Goal [CLUSTER 2017]

A **generalized** mechanism that

1. Directly estimates the **performance benefit of migrating a page** between **any two types of memory**

2. Places **only** the **performance-critical data** in the fast memory

Utility-Based Hybrid Memory Management

- A memory manager that works for *any* hybrid memory
  - e.g., DRAM-NVM, DRAM-RLDRAM

- **Key Idea**
  - For each page, use **comprehensive** characteristics to calculate estimated *utility* (i.e., performance impact) of migrating page from one memory to the other in the system

  - **Migrate only pages with the highest utility** (i.e., pages that improve system performance the most when migrated)

- Li+, "Utility-Based Hybrid Memory Management", CLUSTER 2017.

Key Mechanisms of UH-MEM

- For each page, estimate **utility** using a **performance model**
  - **Application stall time reduction**

    How much would migrating a page benefit the performance of the application that the page belongs to?
 - **Application performance sensitivity**

    How much does the improvement of a single application's performance increase the *overall* system performance?

    $$Utility = \Delta StallTime_i \times Sensitivity_i$$

- **Migrate** only pages whose utility exceed the migration threshold from slow memory to fast memory

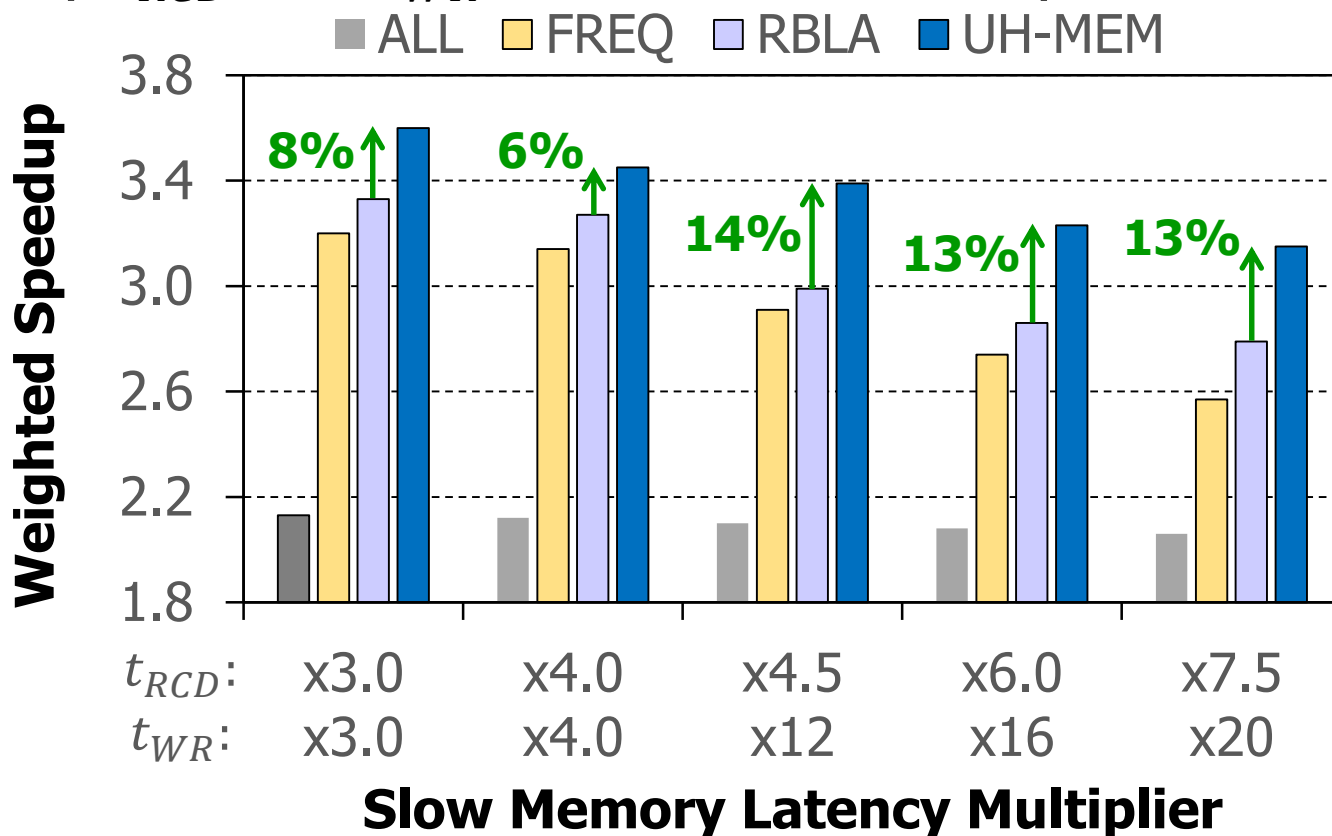- Periodically **adjust migration threshold**

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Results: System Performance
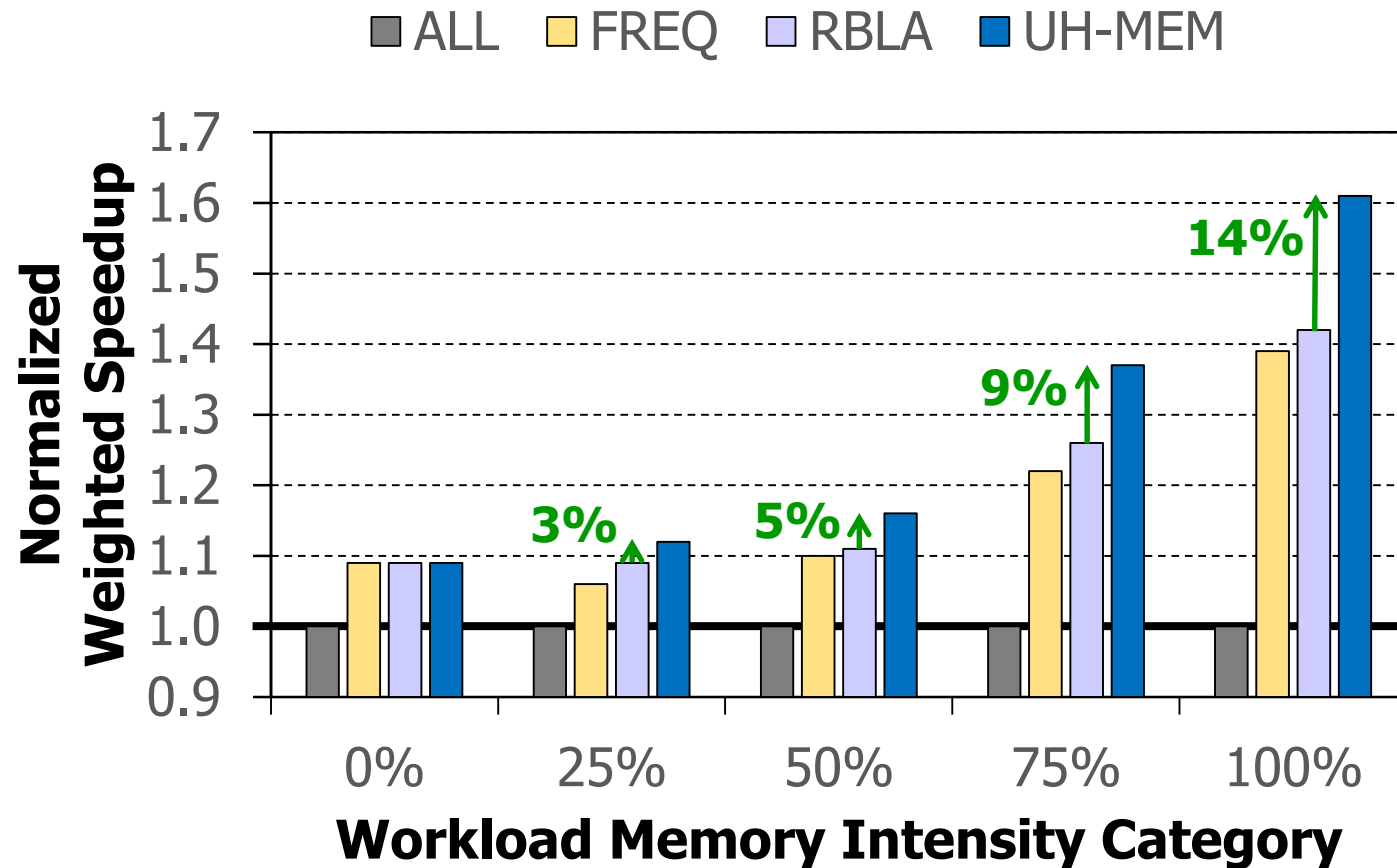
UH-MEM improves system performance
over the best state-of-the-art hybrid memory manager

Results: Sensitivity to Slow Memory Latency

- We vary t_{RCD} and t_{WR} of the slow memory

**UH-MEM improves system performance
for a wide variety of hybrid memory systems**

More on UH-MEM

- Yang Li, Saugata Ghose, Jongmoo Choi, Jin Sun, Hui Wang, and Onur Mutlu,
"Utility-Based Hybrid Memory Management"
Proceedings of the 19th IEEE Cluster Conference (**CLUSTER**), Honolulu, Hawaii, USA, September 2017.
[Slides (pptx) (pdf)]

Utility-Based Hybrid Memory Management

Yang Li[†]   Saugata Ghose[†]   Jongmoo Choi[‡]   Jin Sun[†]   Hui Wang[★]   Onur Mutlu[+†]

[†]*Carnegie Mellon University*   [‡]*Dankook University*   [★]*Beihang University*   [+]*ETH Zürich*
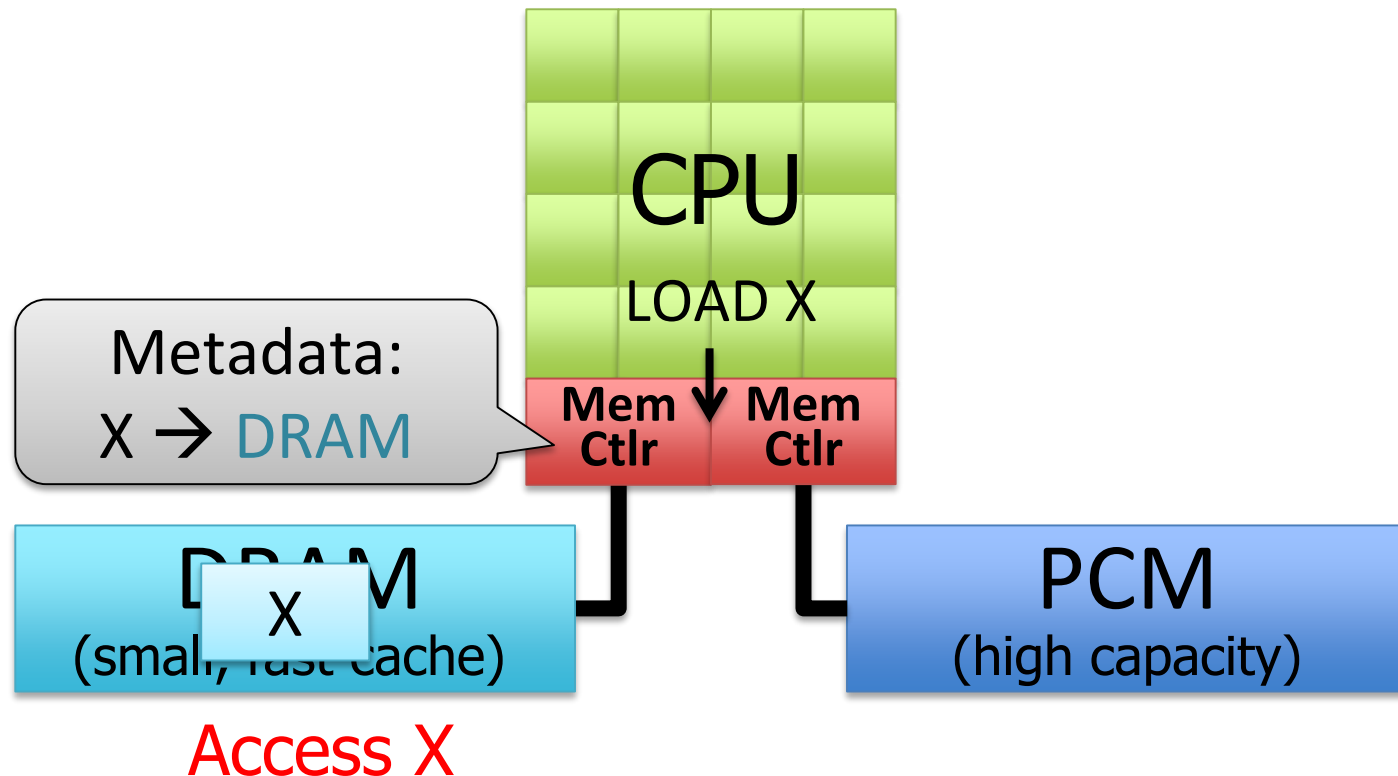
Enabling
an Emerging Technology
to Augment DRAM

Managing Hybrid Memories

Another Challenge

Designing Effective Large (DRAM) Caches

One Problem with Large DRAM Caches

- A large DRAM cache requires a large metadata (tag + block-based information) store

- How do we design an efficient DRAM cache?

Idea 1: Tags in Memory

- **Store tags in the same row as data in DRAM**
  - Store metadata in same row as their data
  - Data and metadata can be accessed together

DRAM row →

| Cache block 0 | Cache block 1 | Cache block 2 | Tag 0 | Tag 1 | Tag 2 |
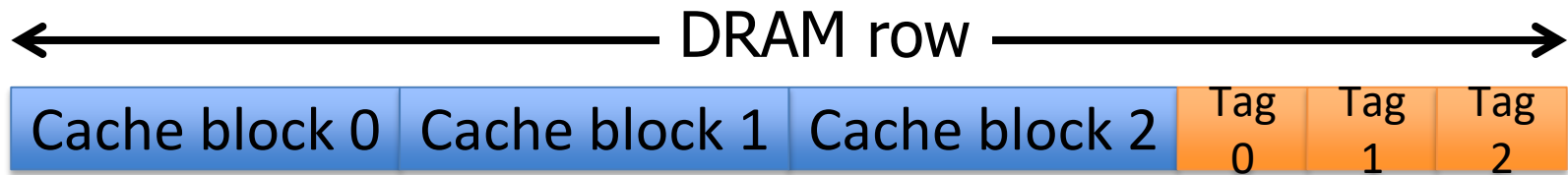
- **Benefit: No on-chip tag storage overhead**
- **Downsides:**
  - Cache hit determined only after a DRAM access
 - Cache hit requires two DRAM accesses

Idea 2: Cache Tags in SRAM

- Recall Idea 1: Store all metadata in DRAM
  - To reduce metadata storage overhead

- Idea 2: Cache in on-chip SRAM frequently-accessed metadata
  - Cache only a small amount to keep SRAM size small

Idea 3: Dynamic Data Transfer Granularity

- Some applications benefit from caching more data
  - They have good spatial locality
- Others do not
  - Large granularity wastes bandwidth and reduces cache utilization

- Idea 3: Simple dynamic caching granularity policy
  - Cost-benefit analysis to determine best DRAM cache block size
  - Group main memory into sets of rows
  - Different sampled row sets follow different fixed caching granularities
  - The rest of main memory follows the best granularity
    - Cost–benefit analysis: access latency versus number of cachings
    - Performed every quantum

TIMBER Performance
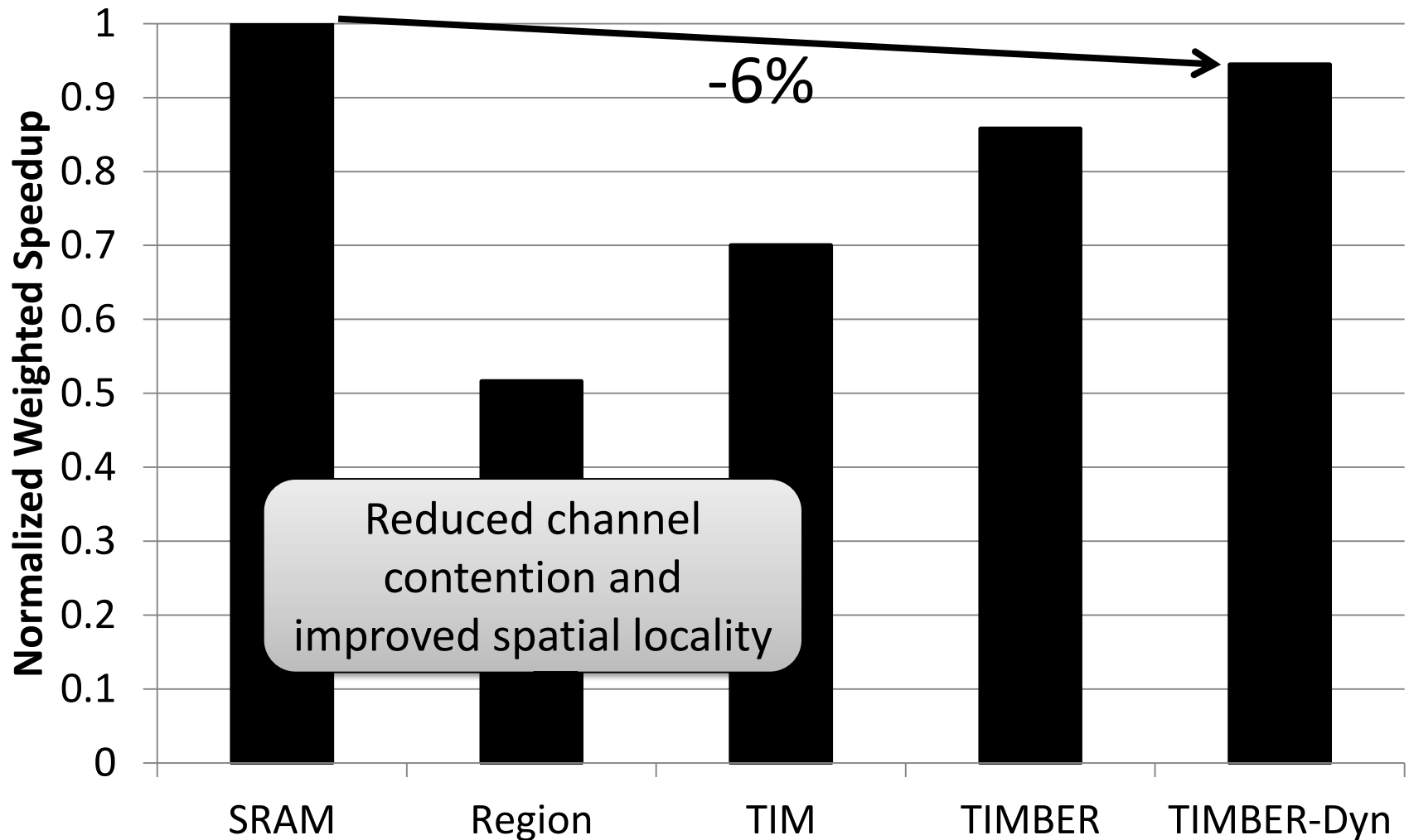
Meza, Chang, Yoon, Mutlu, Ranganathan, "Enabling Efficient and Scalable Hybrid Memories," IEEE Comp. Arch. Letters, 2012.

TIMBER Energy Efficiency
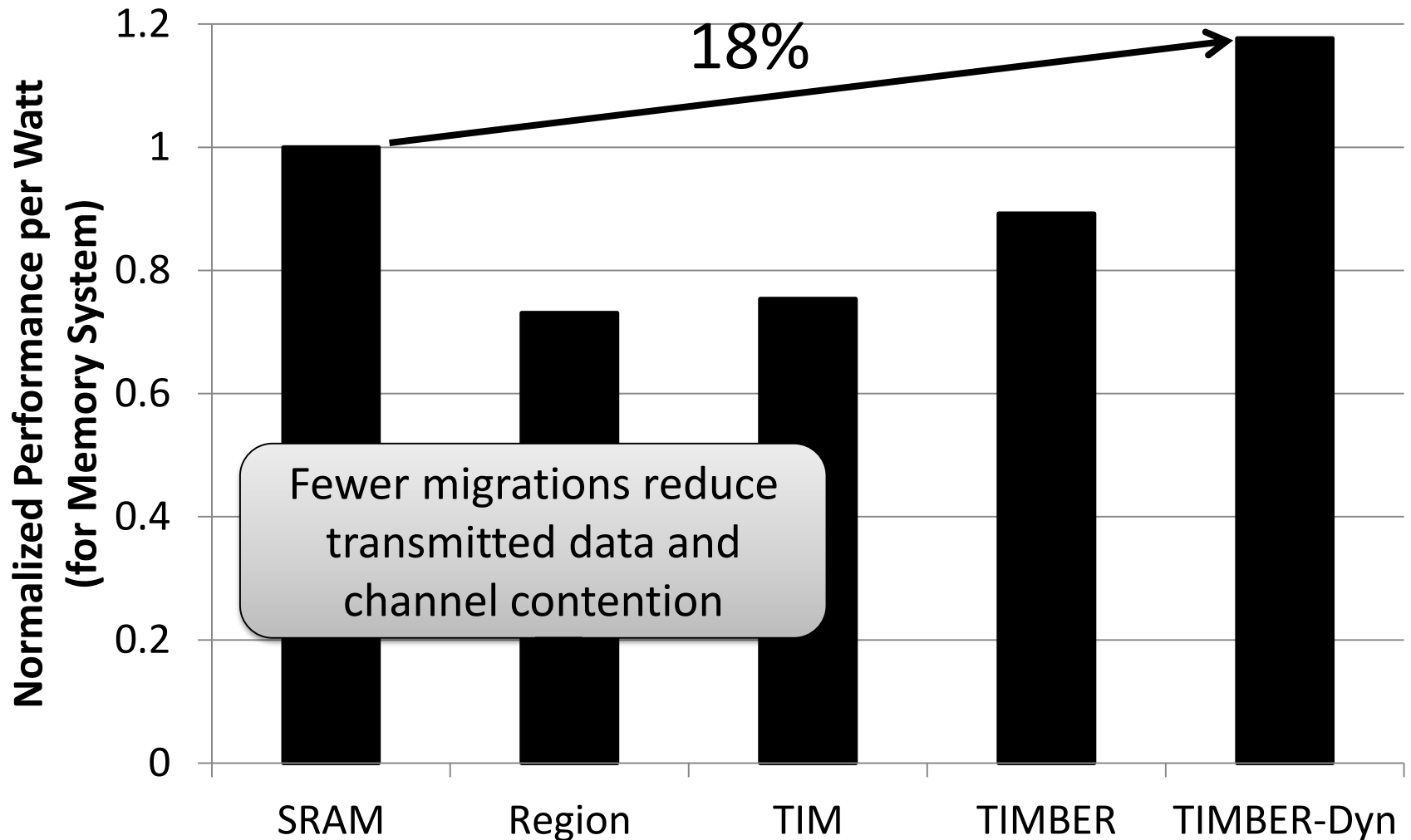
Meza, Chang, Yoon, Mutlu, Ranganathan, "Enabling Efficient and Scalable Hybrid Memories," IEEE Comp. Arch. Letters, 2012.

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On Large DRAM Cache Design

- Justin Meza, Jichuan Chang, HanBin Yoon, Onur Mutlu, and Parthasarathy Ranganathan,
  "Enabling Efficient and Scalable Hybrid Memories Using Fine-Granularity DRAM Cache Management"
  IEEE Computer Architecture Letters (**CAL**), February 2012.

Enabling Efficient and Scalable Hybrid Memories Using Fine-Granularity DRAM Cache Management

Justin Meza*   Jichuan Chang†   HanBin Yoon*   Onur Mutlu*   Parthasarathy Ranganathan†
*Carnegie Mellon University   †Hewlett-Packard Labs
{meza,hanbinyoon,onur}@cmu.edu   {jichuan.chang,partha.ranganathan}@hp.com

DRAM Caches: Many Recent Options

Table 1: Summary of Operational Characteristics of Different State-of-the-Art DRAM Cache Designs – We assume perfect way prediction for Unison Cache. Latency is relative to the access time of the off-package DRAM (see Section 6 for baseline latencies). We use different colors to indicate the high (dark red), medium (white), and low (light green) overhead of a characteristic.

Scheme	DRAM Cache Hit	DRAM Cache Miss	Replacement Traffic	Replacement Decision	Large Page Caching
Unison [32]	In-package traffic: 128 B (data + tag read and update) Latency: ~1x	In-package traffic: 96 B (spec. data + tag read) Latency: ~2x	On every miss Footprint size [31]	Hardware managed, set-associative, LRU	Yes
Alloy [50]	In-package traffic: 96 B (data + tag read) Latency: ~1x	In-package traffic: 96 B (spec. data + tag read) Latency: ~2x	On some misses Cacheline size (64 B)	Hardware managed, direct-mapped, stochastic [20]	Yes
TDC [38]	In-package traffic: 64 B Latency: ~1x TLB coherence	In-package traffic: 0 B Latency: ~1x TLB coherence	On every miss Footprint size [28]	Hardware managed, fully-associative, FIFO	No
HMA [44]	In-package traffic: 64 B Latency: ~1x	In-package traffic: 0 B Latency: ~1x	Software managed, high replacement cost		Yes
Banshee (This work)	In-package traffic: 64 B Latency: ~1x	In-package traffic: 0 B Latency: ~1x	Only for hot pages Page size (4 KB)	Hardware managed, set-associative, frequency based	Yes

Yu+, "Banshee: Bandwidth-Efficient DRAM Caching via Software/Hardware Cooperation," MICRO 2017.

Banshee [MICRO 2017]

- **Tracks presence in cache using TLB and Page Table**
  - No tag store needed for DRAM cache
  - Enabled by a new lightweight lazy TLB coherence protocol

- **New bandwidth-aware frequency-based replacement policy**
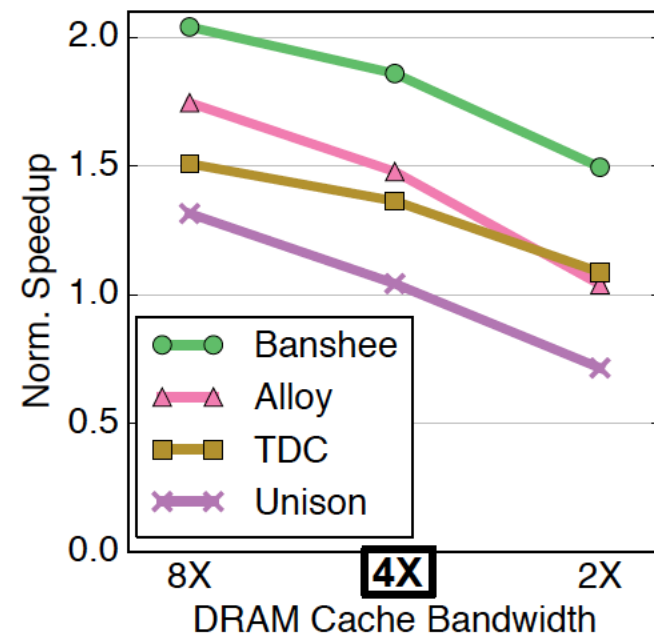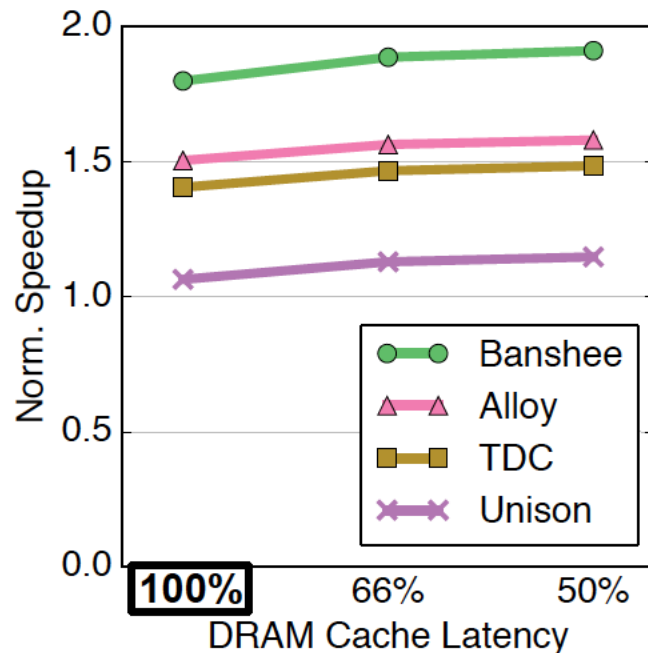
More on Banshee

- Xiangyao Yu, Christopher J. Hughes, Nadathur Satish, Onur Mutlu, and Srinivas Devadas,
  "Banshee: Bandwidth-Efficient DRAM Caching via Software/Hardware Cooperation"
  Proceedings of the 50th International Symposium on Microarchitecture (**MICRO**), Boston, MA, USA, October 2017.

Banshee: Bandwidth-Efficient DRAM Caching via Software/Hardware Cooperation

Xiangyao Yu[1]   Christopher J. Hughes[2]   Nadathur Satish[2]   Onur Mutlu[3]   Srinivas Devadas[1]

[1]MIT   [2]Intel Labs   [3]ETH Zürich

Other Opportunities with Emerging Technologies

- **Merging of memory and storage**
  - e.g., a single interface to manage all data

- **New applications**
  - e.g., ultra-fast checkpoint and restore

- **More robust system design**
  - e.g., reducing data loss

- **Processing tightly-coupled with memory**
  - e.g., enabling efficient search and filtering

Recall: In-Memory
Bulk Bitwise Operations

In-Memory Bulk Bitwise Operations

- We can support in-DRAM COPY, ZERO, AND, OR, NOT, MAJ
- At low cost
- Using analog computation capability of DRAM
  - Idea: activating multiple rows performs computation
- 30-60X performance and energy improvement
  - Seshadri+, "Ambit: In-Memory Accelerator for Bulk Bitwise Operations Using Commodity DRAM Technology," MICRO 2017.

- New memory technologies enable even more opportunities
  - Memristors, resistive RAM, phase change mem, STT-MRAM, …
  - Can operate on data with minimal movement

Pinatubo: RowClone and Bitwise Ops in PCM

Pinatubo: A Processing-in-Memory Architecture for Bulk Bitwise Operations in Emerging Non-volatile Memories

Shuangchen Li[1], Cong Xu[2], Qiaosha Zou[1,5], Jishen Zhao[3], Yu Lu[4], and Yuan Xie[1]

University of California, Santa Barbara[1], Hewlett Packard Labs[2]
University of California, Santa Cruz[3], Qualcomm Inc.[4], Huawei Technologies Inc.[5]
{shuangchenli, yuanxie}ece.ucsb.edu[1]

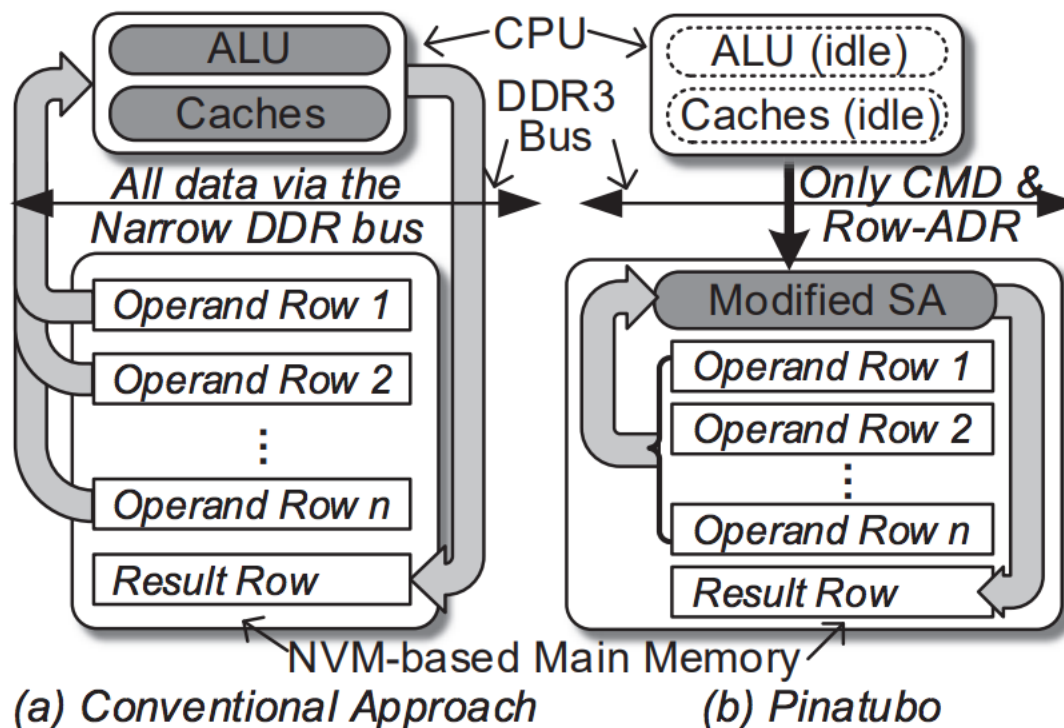# Pinatubo: RowClone and Bitwise Ops in PCM

Figure 2: Overview: (a) Computing-centric approach, moving tons of data to CPU and write back. (b) The proposed Pinatubo architecture, performs n-row bitwise operations inside NVM in one step.

New: In-Memory Crossbar Array Operations

In-Memory Crossbar Array Operations

- Some emerging NVM technologies have crossbar array structure
  - Memristors, resistive RAM, phase change mem, STT-MRAM, …

- Crossbar arrays can be used to perform dot product operations using "analog computation capability"
  - Can operate on multiple pieces of data using Kirchoff's laws
    - Bitline current is a sum of products of wordline V x (1 / cell R)
  - Computation is in analog domain inside the crossbar array

- Need peripheral circuitry for D->A and A->D conversion of inputs and outputs

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In-Memory Crossbar Computation
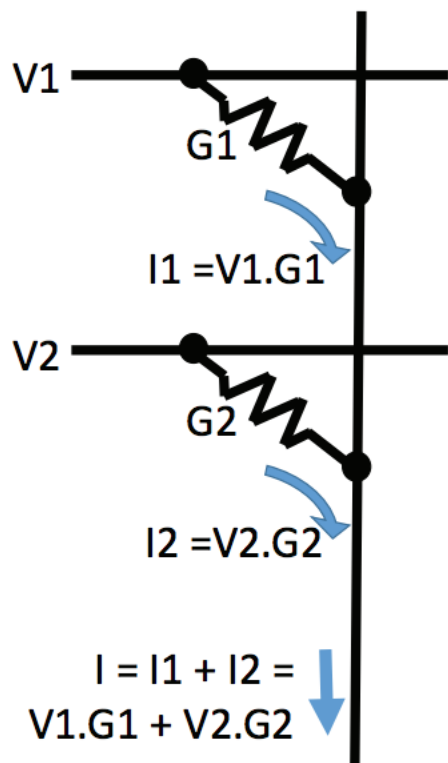
(a) Multiply-Accumulate operation
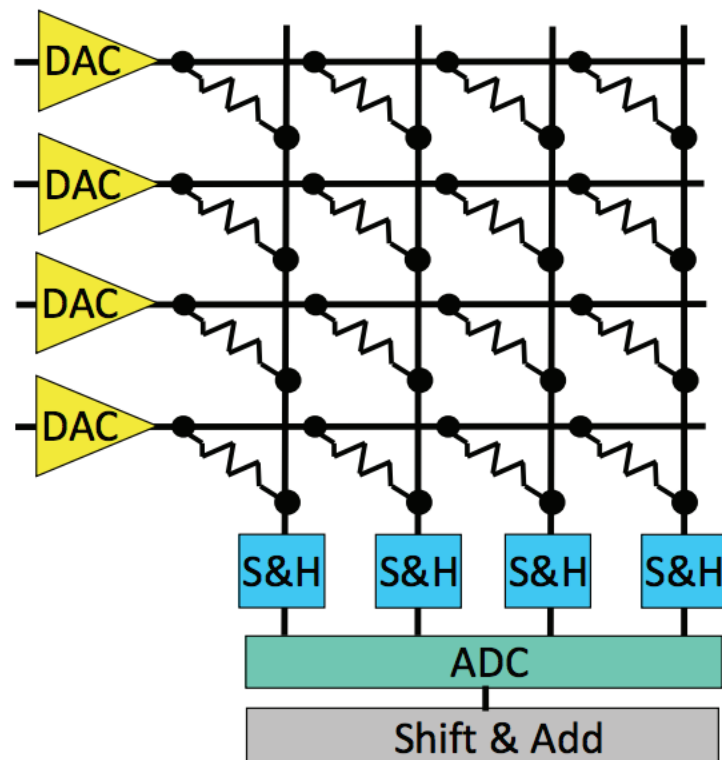
(b) Vector-Matrix Multiplier

Fig. 1. (a) Using a bitline to perform an analog sum of products operation. (b) A memristor crossbar used as a vector-matrix multiplier.

In-Memory Crossbar Computation

$$\left(\begin{array}{cccc} i_1 & i_2 & i_3 & i_4 \end{array} \right) = \left(O_1\ O_2\ O_3\ O_4 \right)$$

$$I_1 = \frac{1}{R_{11}}V_1 + \frac{1}{R_{21}}V_2 + \frac{1}{R_{31}}V_3 + \frac{1}{R_{41}}V_4$$
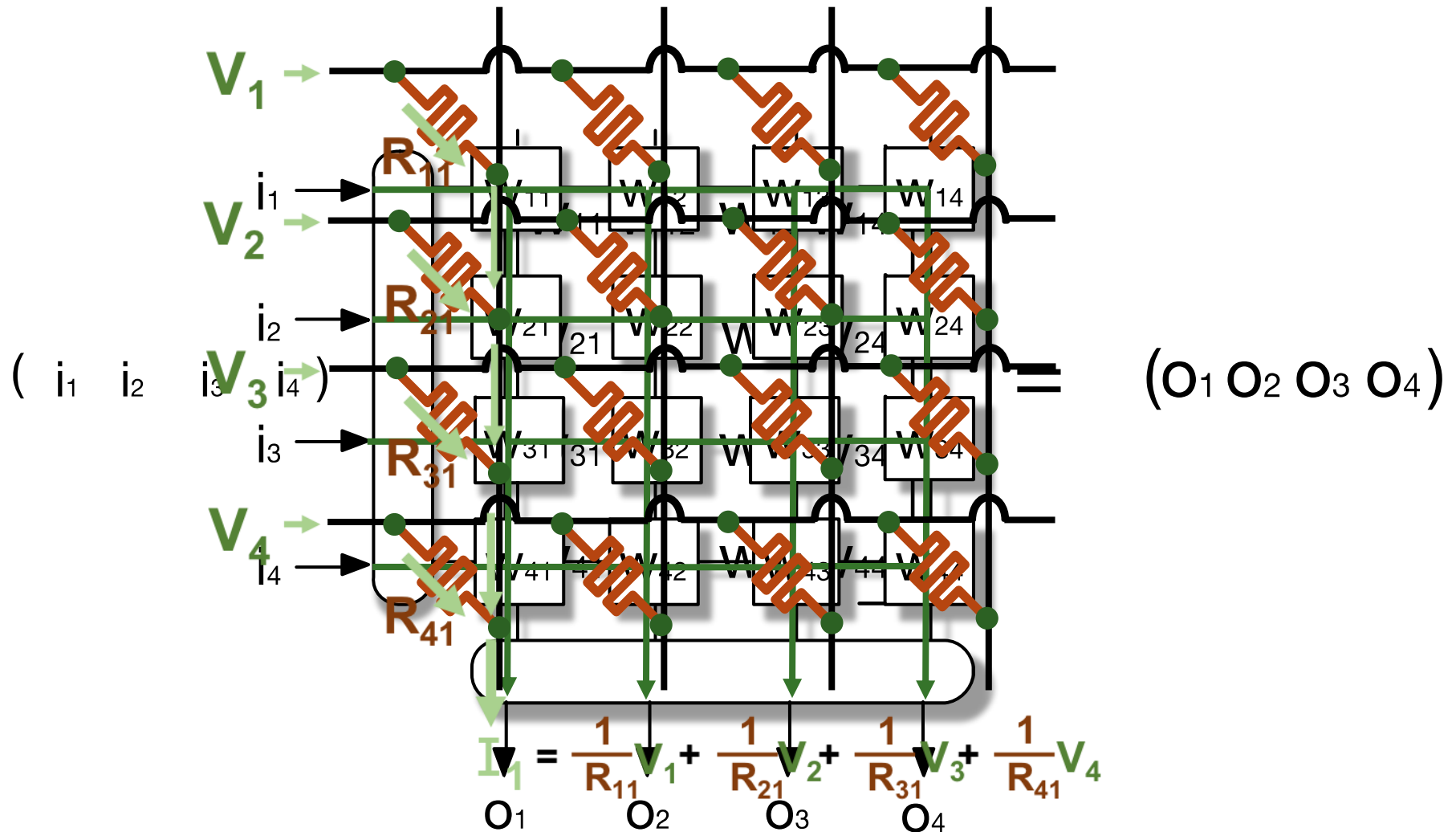
Required Peripheral Circuitry
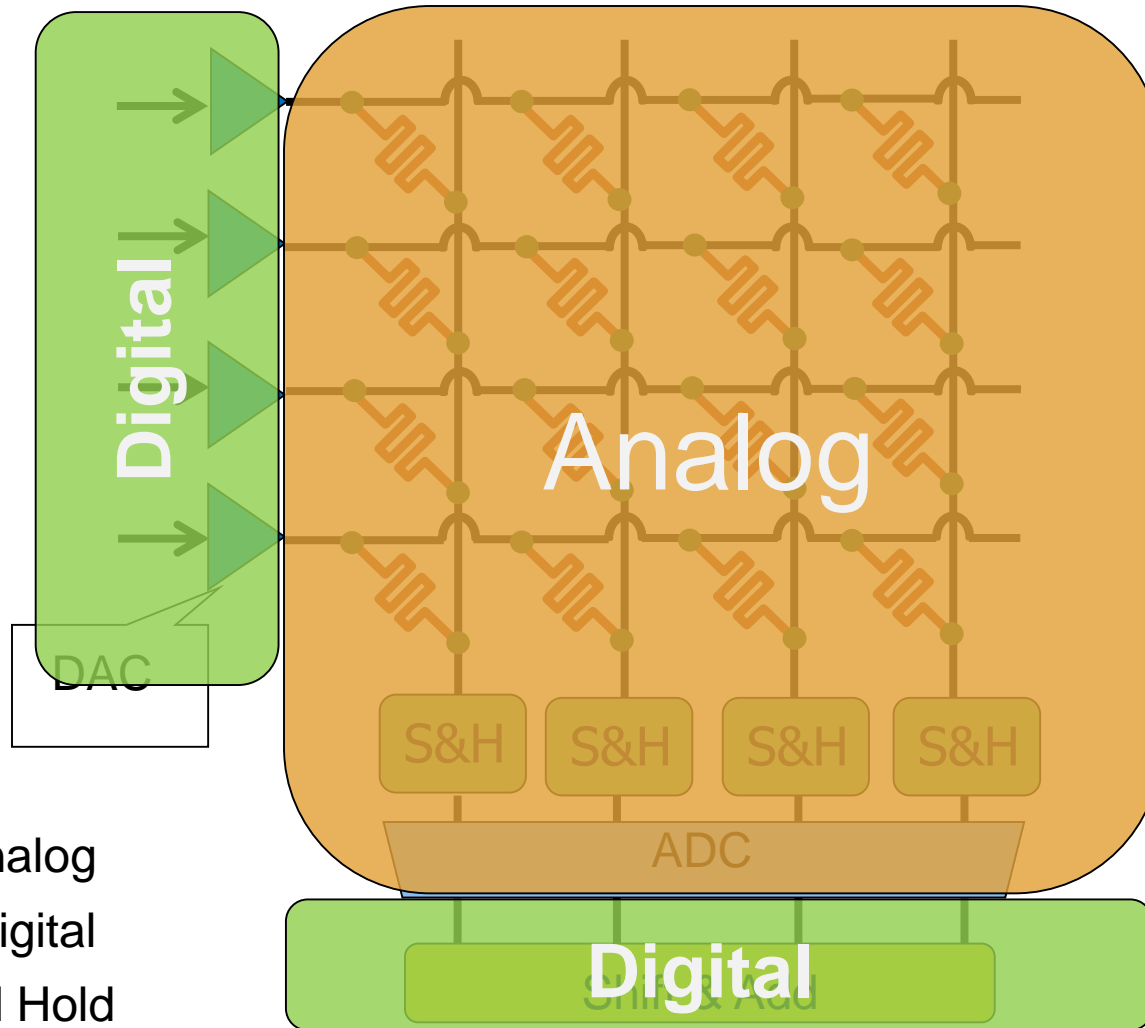
DAC: Digital to Analog

ADC: Analog to Digital

S&H: Sample and Hold

Shift and add: used to summarize the final output

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An Example of 2D Convolution

Output feature map

Structure information
Input: 5*5 (blue)
Kernel (filter): 3*3 (grey)
Output: 5*5 (green)

Computation information
Stride: 1
Padding: 1 (white)

Output Dim = (Input + 2*Padding
- Kernel) / Stride + 1
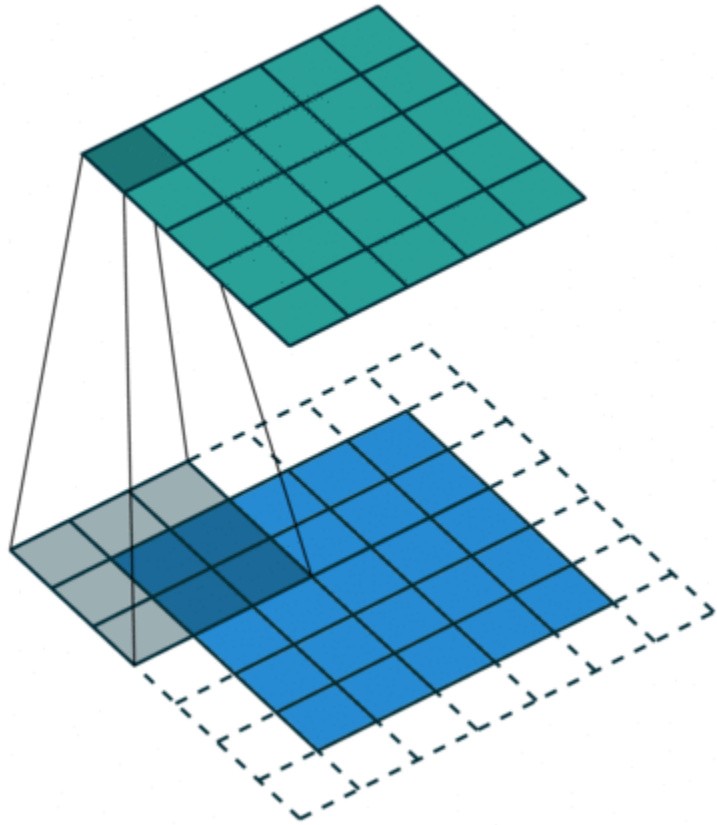
Input feature map

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Mapping Computation onto the Crossbar

Input   Kernel   Output

A convolution operation in neural network application

Padding: 2
Stride: 1

An NVM-based PIM array

A NVM cell
A weight value
PIM Array

SAFARI
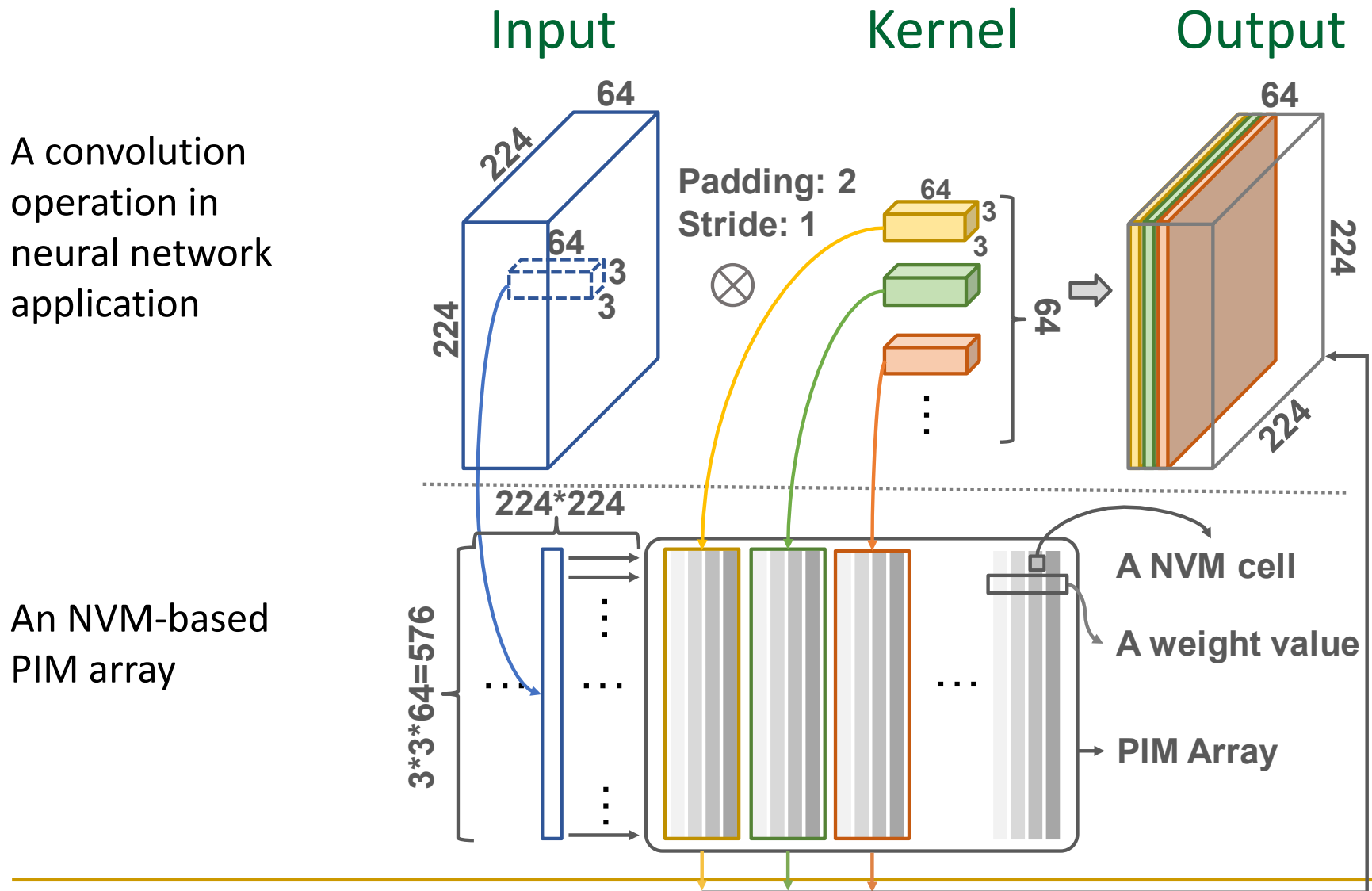
An Overview of NVM-Based PIM System
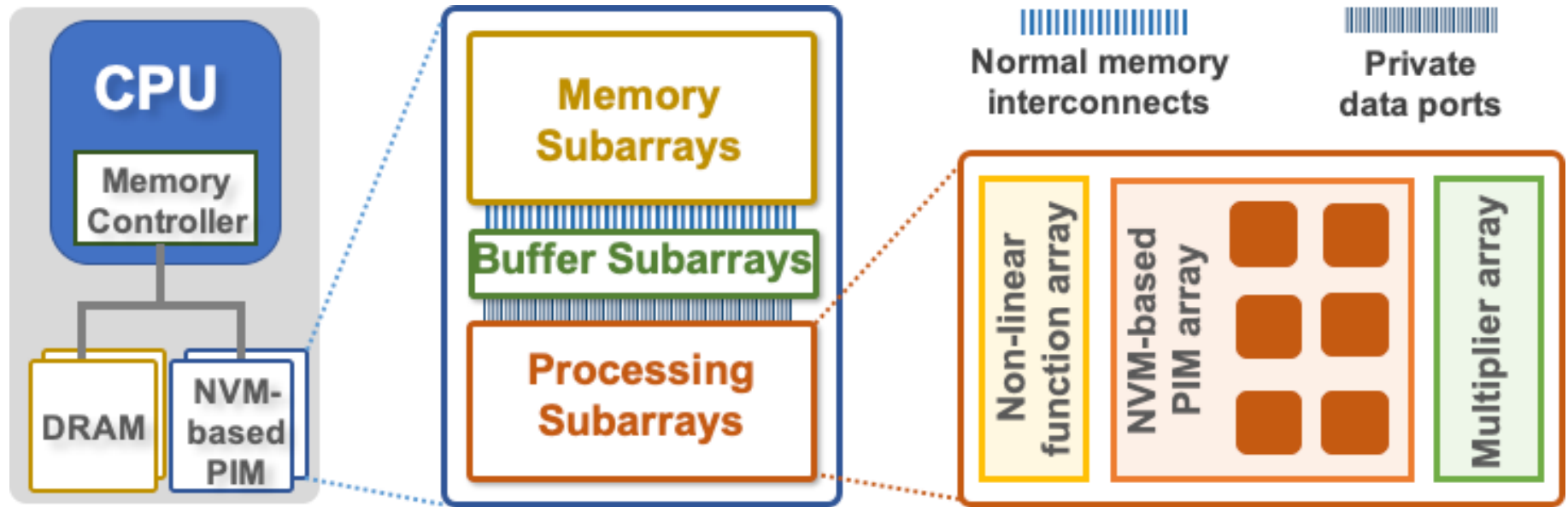
NVM-based PIM array:
       core processing unit for vector-matrix multiplication

Non-linear function array:
       processing unit for non-linear functions (e.g., ReLU operations in neural networks)

Multiplier array:
       handles element-wise operations

Example Readings on NVM-Based PIM

- Shafiee+, "ISAAC: A Convolutional Neural Network Accelerator with In-Situ Analog Arithmetic in Crossbars", ISCA 2016.

- Chi+, "PRIME: A Novel Processing-in-memory Architecture for Neural Network Computation in ReRAM-based Main Memory", ISCA 2016.

- Prezioso+, "Training and Operation of an Integrated Neuromorphic Network based on Metal-Oxide Memristors", Nature 2015

- Ambrogio+, "Equivalent-accuracy accelerated neural-network training using analogue memory", Nature 2018.

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We Did Not Cover The Rest of the Slides. They Are For Your Benefit.

Computer Architecture
Lecture 15: Emerging Memory Technologies

Prof. Onur Mutlu

ETH Zürich

Fall 2020

13 November 2020

Other Opportunities with Emerging Technologies

- **Merging of memory and storage**
  - e.g., a single interface to manage all data

- **New applications**
  - e.g., ultra-fast checkpoint and restore

- **More robust system design**
  - e.g., reducing data loss

- **Processing tightly-coupled with memory**
  - e.g., enabling efficient search and filtering

TWO-LEVEL STORAGE MODEL

CPU

`0101`
`1010`
`0110`

Ld/St

MEMORY

DRAM

FILE I/O

STORAGE

HDD

VOLATILE

FAST

BYTE ADDR

NONVOLATILE

SLOW

BLOCK ADDR

TWO-LEVEL STORAGE MODEL

CPU

MEMORY

STORAGE

Ld/St

DRAM

FILE I/O

HDD

NVM

PCM, STT-RAM

VOLATILE

FAST

BYTE ADDR

NONVOLATILE

SLOW

BLOCK ADDR
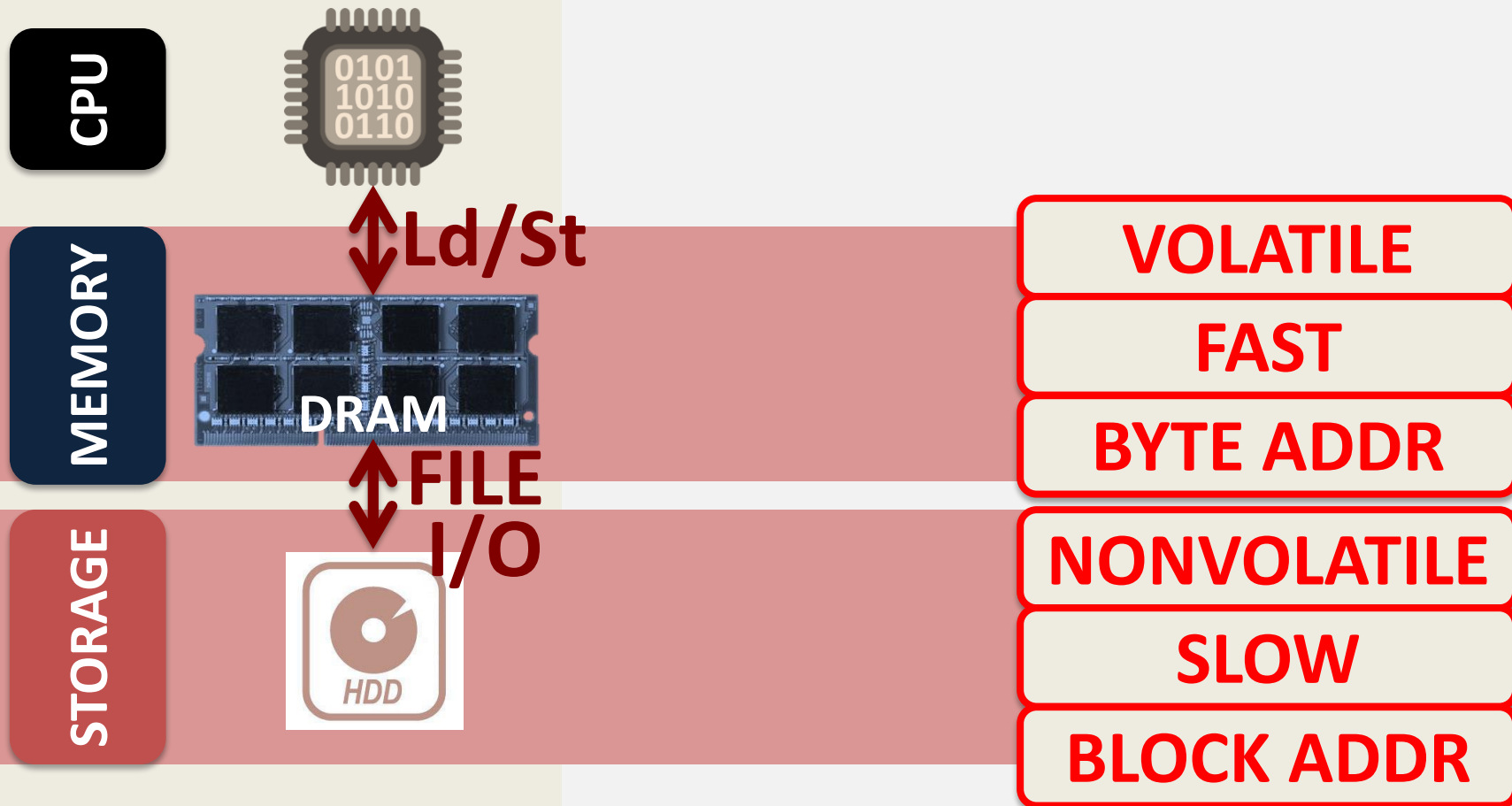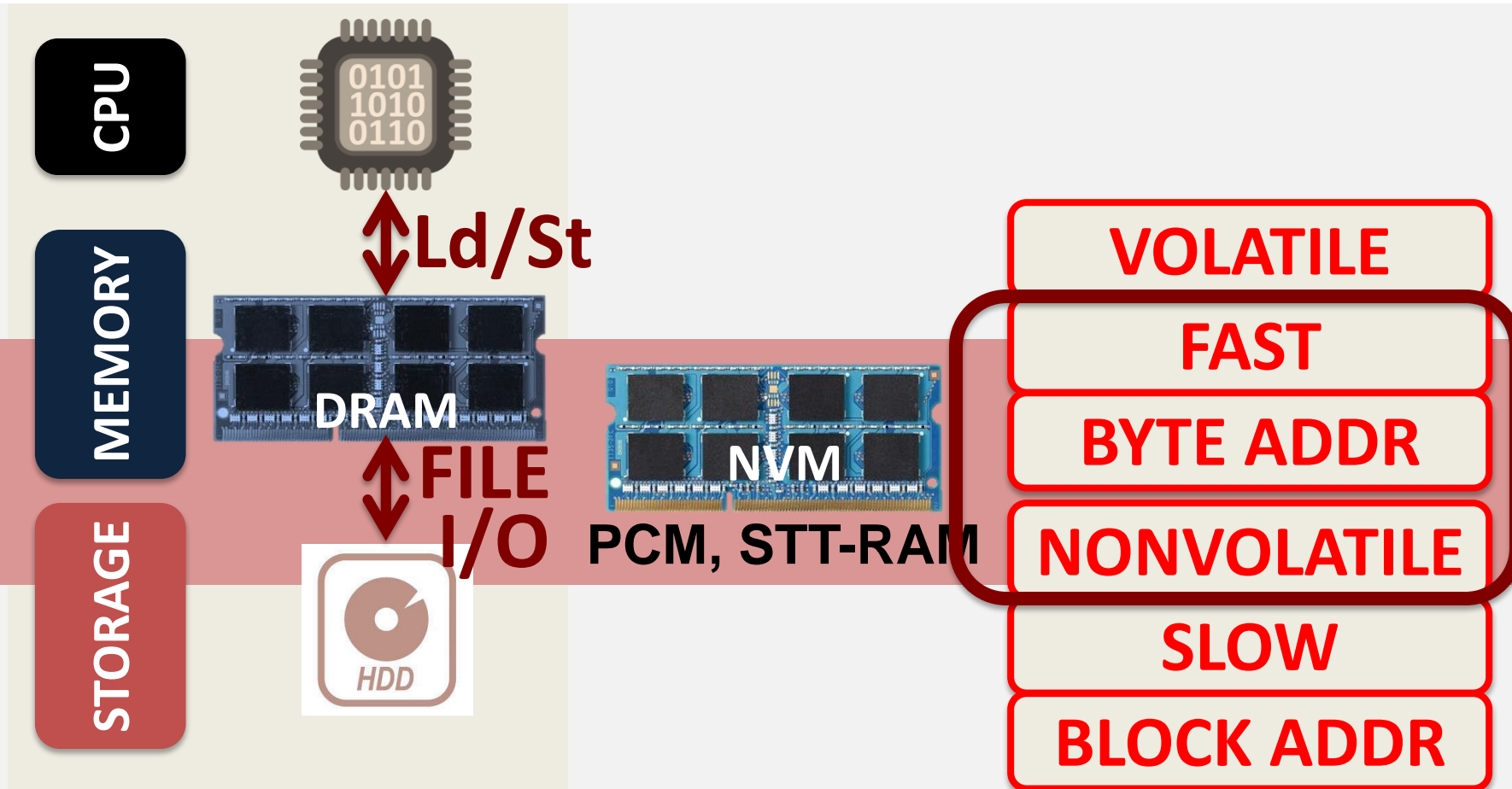
Non-volatile memories combine characteristics of memory and storage

Two-Level Memory/Storage Model

- The traditional two-level storage model is a bottleneck with NVM
  - **Volatile** data in memory → a **load/store** interface
  - **Persistent** data in storage → a **file system** interface
  - Problem: Operating system (OS) and file system (FS) code to locate, translate, buffer data become performance and energy bottlenecks with fast NVM stores

Two-Level Store

Load/Store

fopen, fread, fwrite, …

Virtual memory

Processor and caches

Operating system and file system

Address translation

Main Memory

Persistent (e.g., Phase-Change) Storage (SSD/HDD) Memory
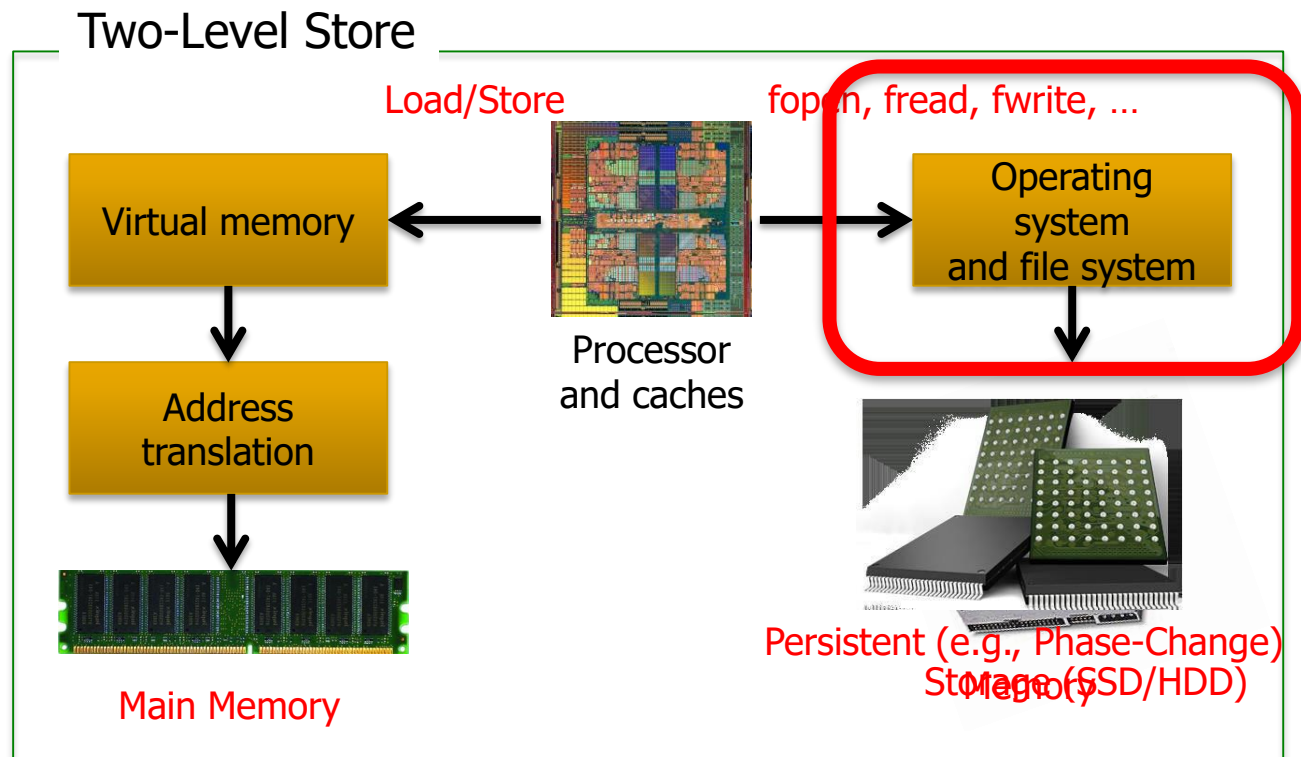
Unified Memory and Storage with NVM

- **Goal:** Unify memory and storage management in a single unit to eliminate wasted work to locate, transfer, and translate data
  - Improves both energy and performance
  - Simplifies programming model as well

Unified Memory/Storage

Persistent Memory Manager

Processor and caches

Load/Store   Feedback

Persistent (e.g., Phase-Change) Memory

Meza+, "A Case for Efficient Hardware-Software Cooperative Management of Storage and Memory," WEED 2013.

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PERSISTENT MEMORY

Ld/St

NVM

CPU
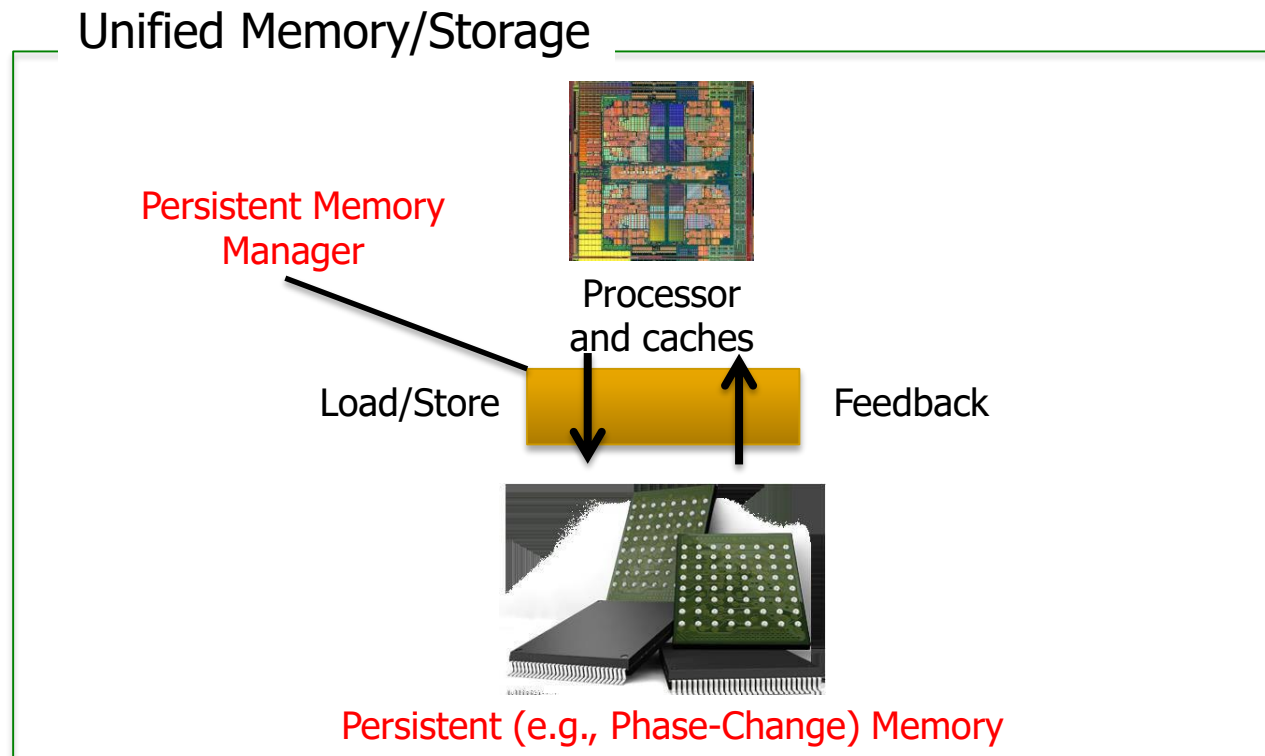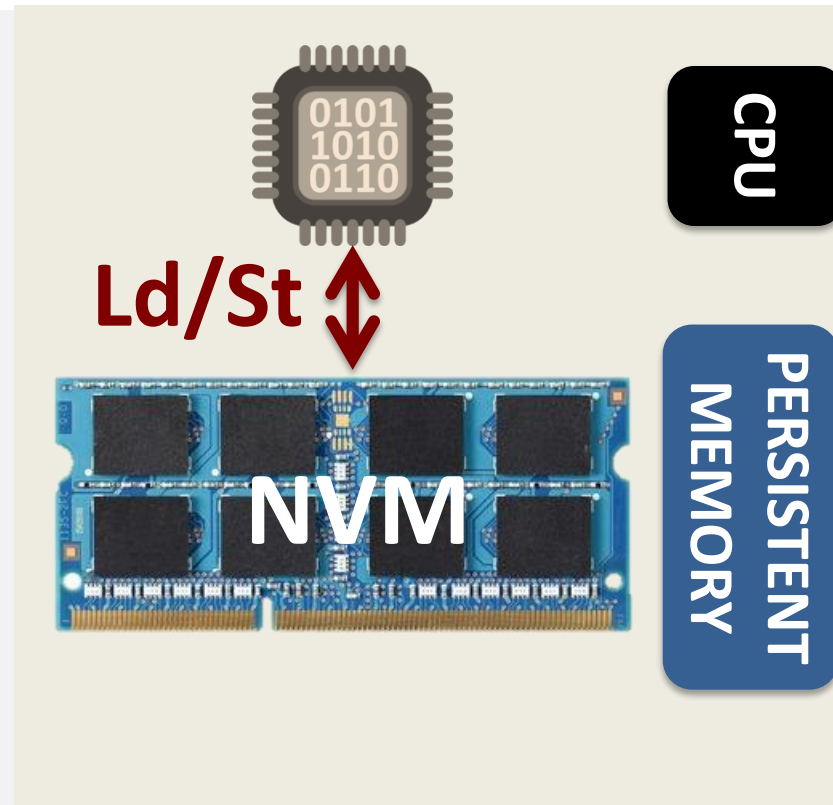
PERSISTENT MEMORY

Provides an opportunity to manipulate persistent data directly

The Persistent Memory Manager (PMM)

```
1  int main(void) {
2    // data in file.dat is persistent
3    FILE myData = "file.dat";          Persistent objects
4    myData = new int[64];
5  }
6  void updateValue(int n, int value) {
7    FILE myData = "file.dat";
8    myData[n] = value; // value is persistent
9  }
```
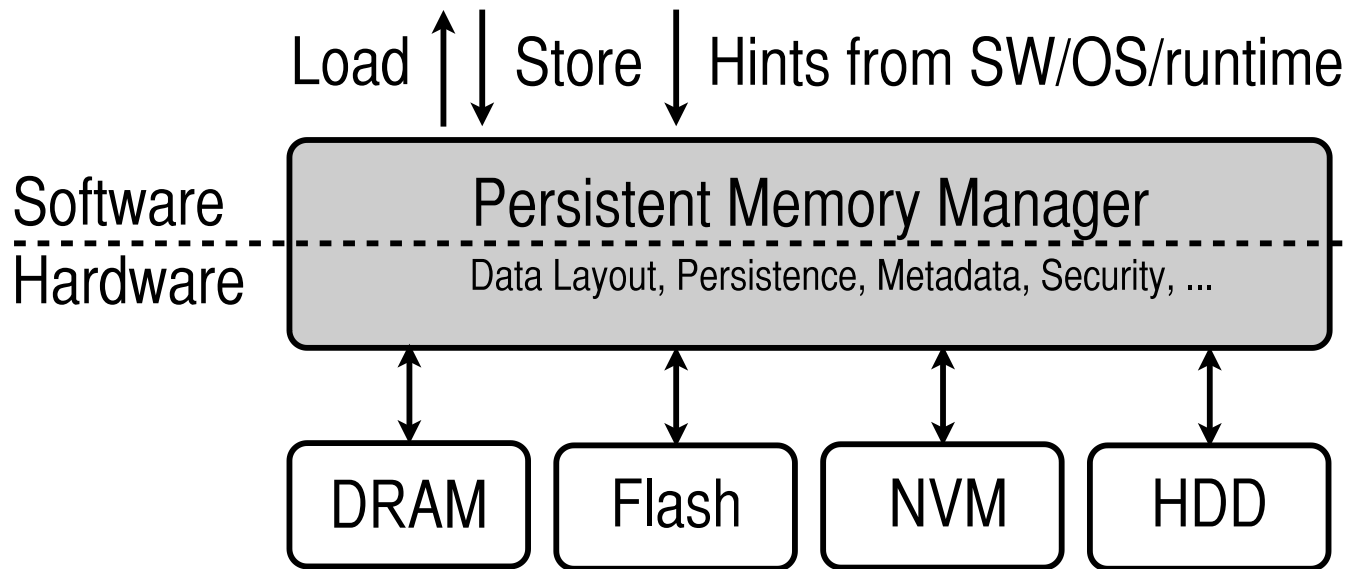
Load ↑↓ Store ↓ Hints from SW/OS/runtime

Software

Hardware

Persistent Memory Manager

Data Layout, Persistence, Metadata, Security, ...

DRAM   Flash   NVM   HDD

PMM uses access and hint information to allocate, locate, migrate and access data in the heterogeneous array of devices

The Persistent Memory Manager (PMM)

- Exposes a load/store interface to access persistent data
  - Applications can directly access persistent memory → no conversion, translation, location overhead for persistent data

- Manages data placement, location, persistence, security
  - To get the best of multiple forms of storage

- Manages metadata storage and retrieval
  - This can lead to overheads that need to be managed

- Exposes hooks and interfaces for system software
  - To enable better data placement and management decisions

- Meza+, "A Case for Efficient Hardware-Software Cooperative Management of Storage and Memory," WEED 2013.

Efficient Data Mapping among Heterogeneous Devices

- A persistent memory exposes a large, persistent address space
  - But it may use many different devices to satisfy this goal
  - From fast, low-capacity volatile DRAM to slow, high-capacity non-volatile HDD or Flash
  - And other NVM devices in between

- Performance and energy can benefit from good placement of data among these devices
  - Utilizing the strengths of each device and avoiding their weaknesses, if possible
  - For example, consider two important application characteristics: locality and persistence
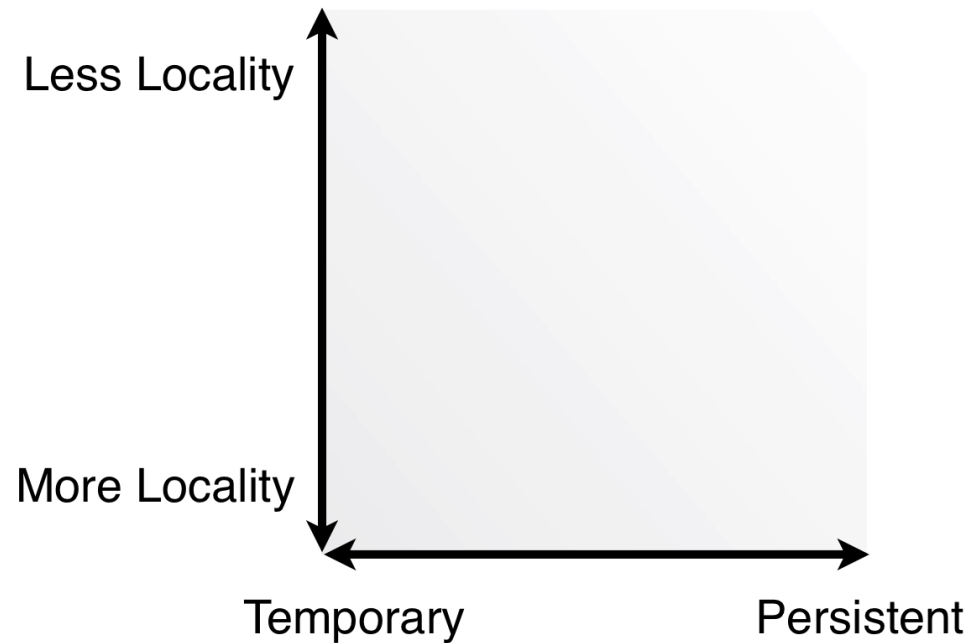
Efficient Data Mapping among Heterogeneous Devices

Efficient Data Mapping among Heterogeneous Devices

Columns in a column store that are
scanned through only infrequently
→ place on Flash

Less Locality

X

More Locality

Temporary   Persistent

Efficient Data Mapping among Heterogeneous Devices

Columns in a column store that are
scanned through only infrequently
→ place on Flash

Less Locality

X

Frequently-updated index for a
Content Delivery Network (CDN)
→ place in DRAM

X

More Locality

Temporary   Persistent
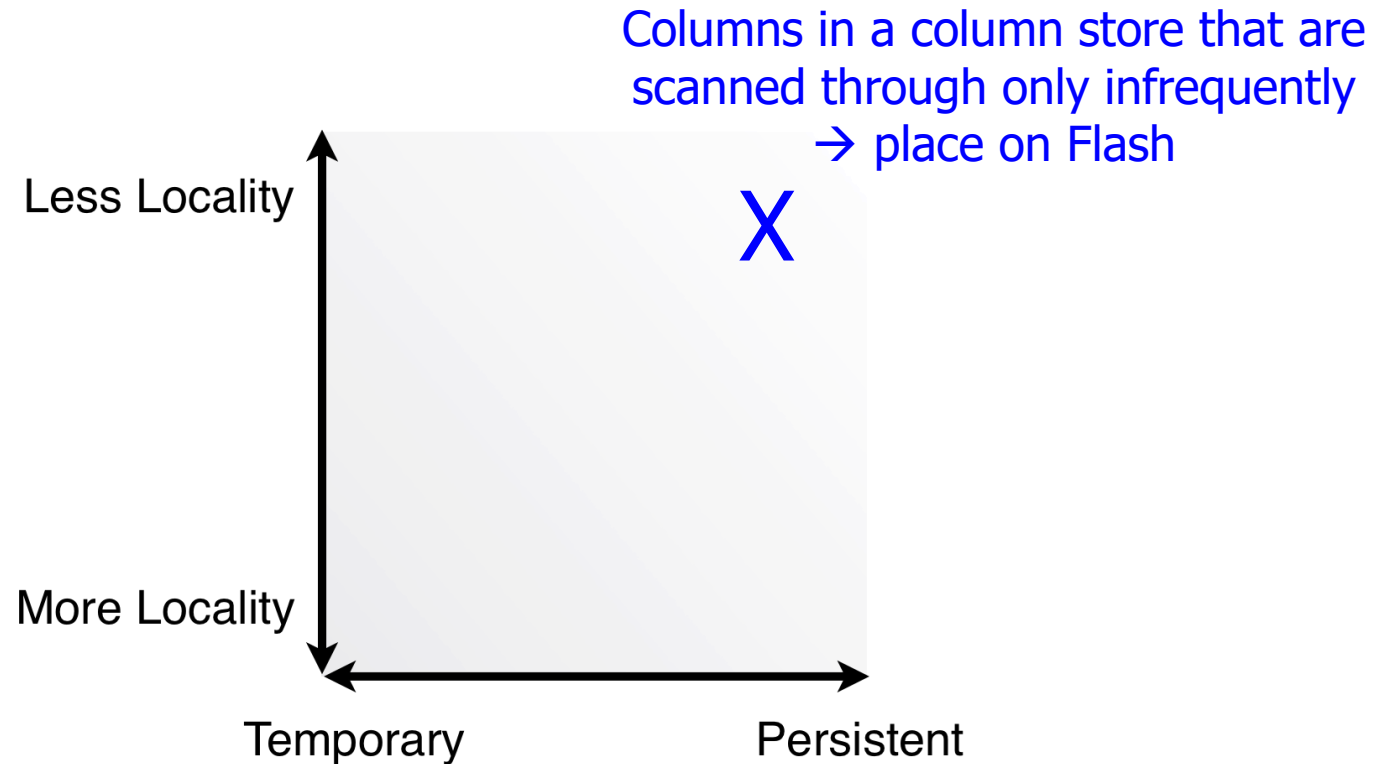
Applications or system software can provide hints for data placement

Evaluated Systems

- **HDD Baseline**
  - Traditional system with volatile DRAM memory and persistent HDD storage
  - Overheads of operating system and file system code and buffering
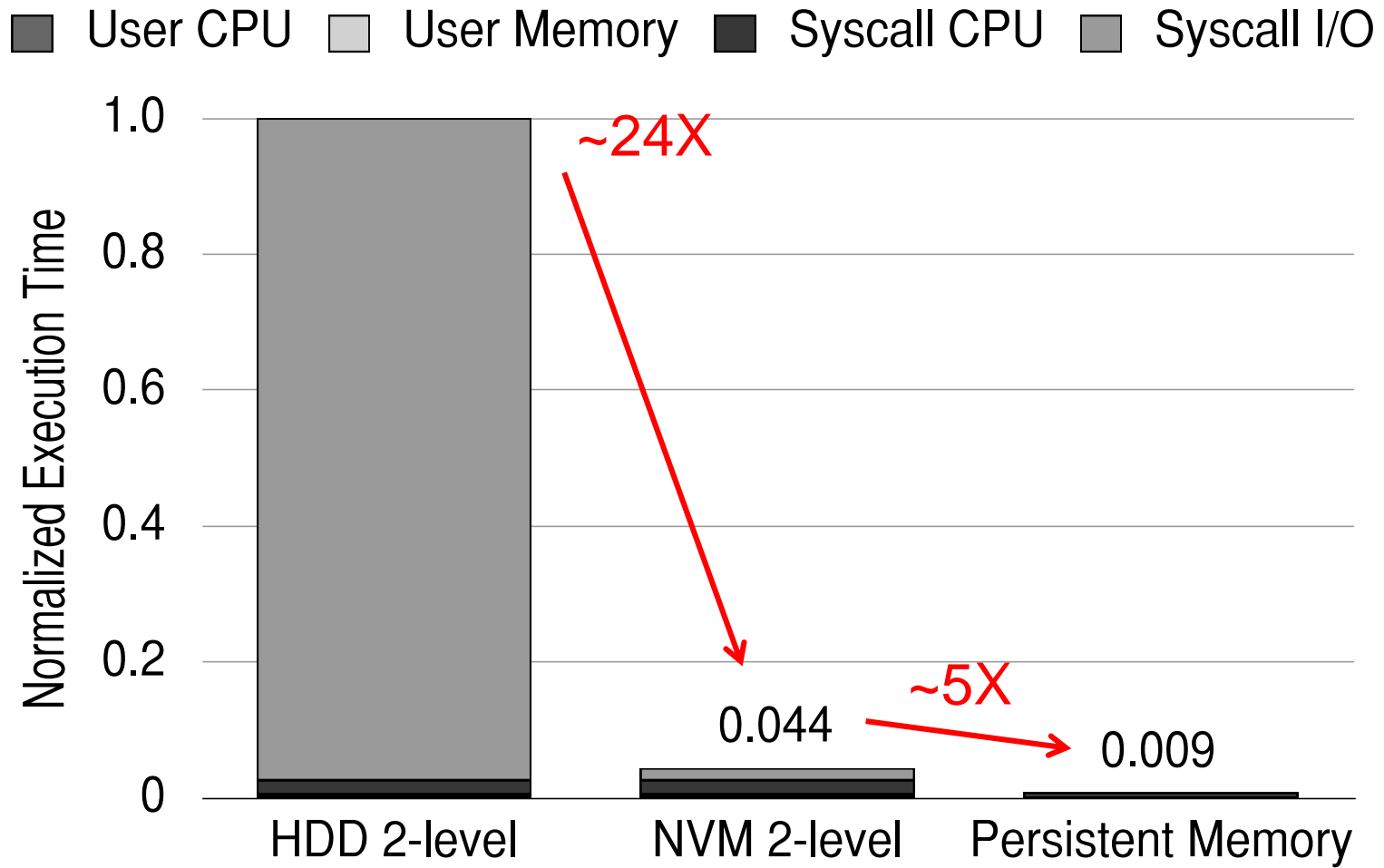
- **NVM Baseline (NB)**
  - Same as HDD Baseline, but HDD is replaced with NVM
  - Still has OS/FS overheads of the two-level storage model

- **Persistent Memory (PM)**
  - Uses only NVM (no DRAM) to ensure full-system persistence
  - All data accessed using loads and stores
  - Does not waste time on system calls
  - Data is manipulated directly on the NVM device

Performance Benefits of a Single-Level Store

Legend: ■ User CPU □ User Memory ■ Syscall CPU ■ Syscall I/O

Y-axis: Normalized Execution Time (0 to 1.0)

~24X, ~5X

0.044, 0.009

HDD 2-level, NVM 2-level, Persistent Memory

Meza+, "A Case for Efficient Hardware-Software Cooperative Management of Storage and Memory," WEED 2013.

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Energy Benefits of a Single-Level Store

Legend: User CPU, Syscall CPU, DRAM, NVM, HDD

Y-axis: Fraction of Total Energy (0 to 1.0)

X-axis categories: HDD 2-level, NVM 2-level, Persistent Memory

~16X, ~5X

NVM 2-level: 0.065
Persistent Memory: 0.013

Meza+, "A Case for Efficient Hardware-Software Cooperative Management of Storage and Memory," WEED 2013.

SAFARI
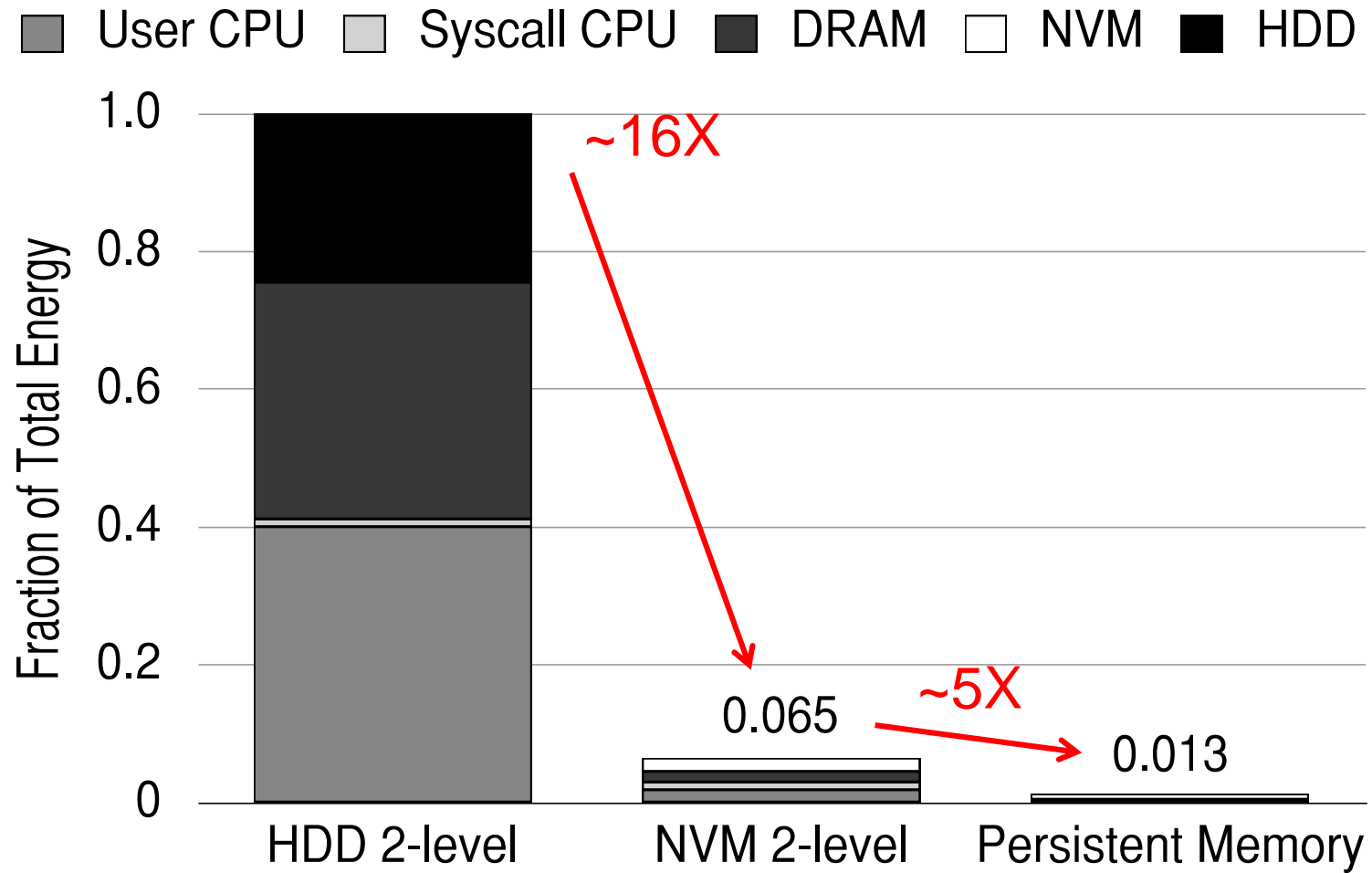
On Persistent Memory Benefits & Challenges

- Justin Meza, Yixin Luo, Samira Khan, Jishen Zhao, Yuan Xie, and Onur Mutlu,
  "A Case for Efficient Hardware-Software Cooperative Management of Storage and Memory"
  Proceedings of the 5th Workshop on Energy-Efficient Design *(**WEED**)*, Tel-Aviv, Israel, June 2013. Slides (pptx) Slides (pdf)

A Case for Efficient Hardware/Software Cooperative Management of Storage and Memory

Justin Meza[*]   Yixin Luo[*]   Samira Khan[*‡]   Jishen Zhao[†]   Yuan Xie[†§]   Onur Mutlu[*]
[*]Carnegie Mellon University   [†]Pennsylvania State University   [‡]Intel Labs   [§]AMD Research

Challenge and Opportunity

Combined
Memory & Storage

Challenge and Opportunity

A Unified Interface to **All Data**

Intel Optane Persistent Memory (2019)

- Non-volatile main memory
- Based on 3D-XPoint Technology

UPMEM Processing-in-DRAM Engine (2019)

- Processing in DRAM Engine

- Includes **standard DIMM modules**, with a **large number of DPU processors** combined with DRAM chips.

- Replaces **standard** DIMMs
  - DDR4 R-DIMM modules
    - 8GB+128 DPUs (16 PIM chips)
    - Standard 2x-nm DRAM process
 - **Large amounts of** compute & memory bandwidth

8GB/128xDPU PIM R-DIMM Module

CPU (x86, ARM, RV...) ⟷ DDR Data bus

UPMEM PIM chip (×8) ... × N
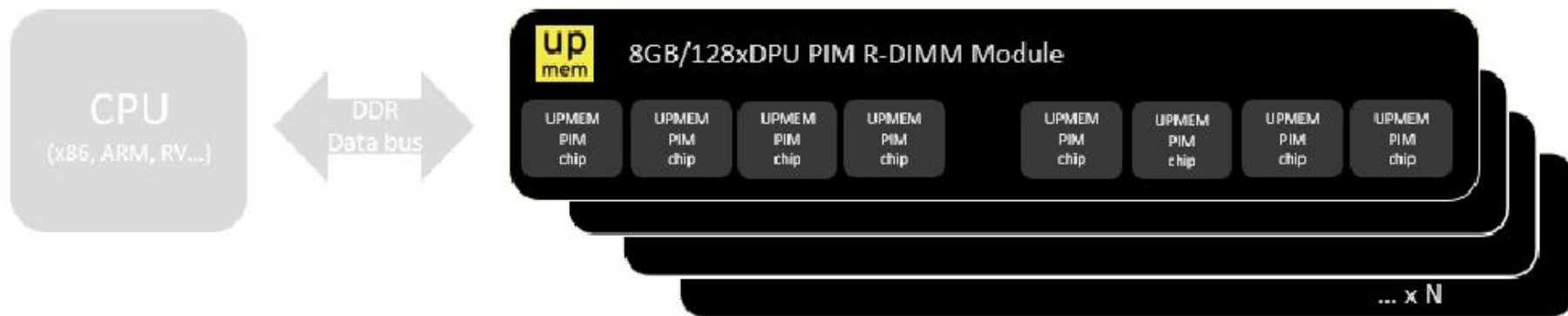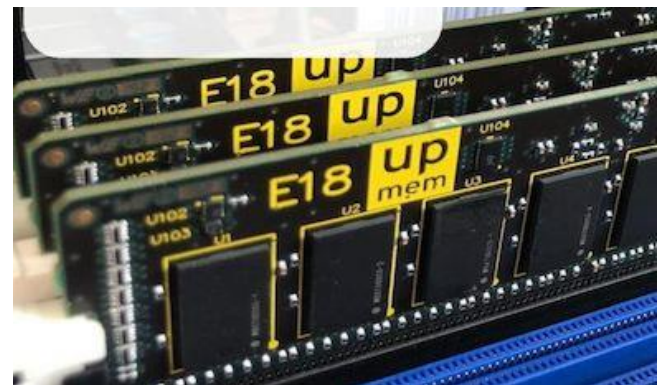
One Key Challenge in Persistent Memory

- **How to ensure consistency of system/data if all memory is persistent?**

- Two extremes
  - Programmer transparent: Let the system handle it
  - Programmer only: Let the programmer handle it

- Many alternatives in-between…

CRASH CONSISTENCY PROBLEM

Add a node to a linked list

2. Link to prev   *1. Link to next*
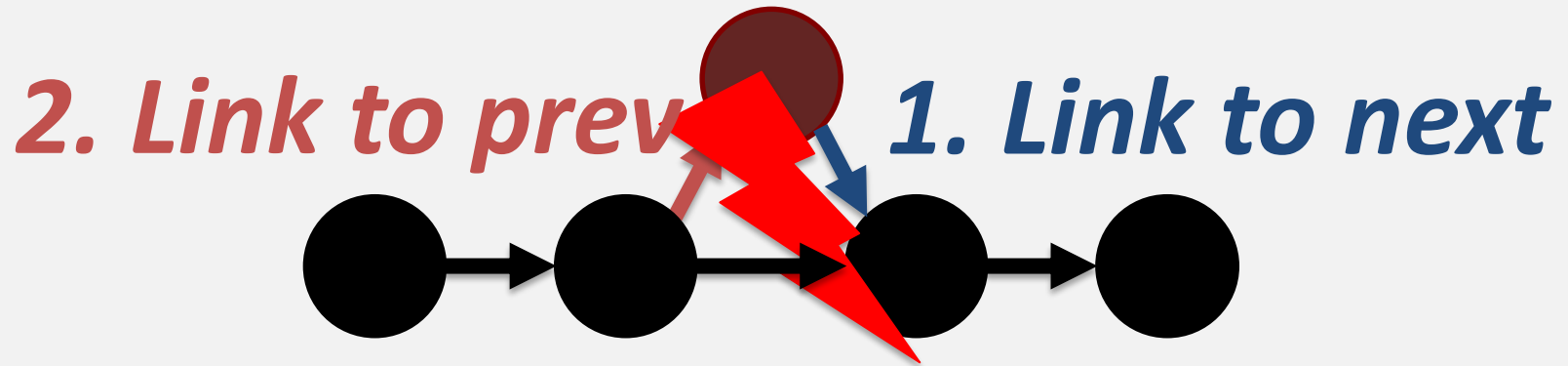
System crash can result in inconsistent memory state

CURRENT SOLUTIONS

Explicit interfaces to manage consistency

    – **NV-Heaps [ASPLOS'11], BPFS [SOSP'09], Mnemosyne [ASPLOS'11]**

```
AtomicBegin {
        Insert a new node;
} AtomicEnd;
```

Limits adoption of NVM
Have to rewrite code with clear partition between volatile and non-volatile data

Burden on the programmers

CURRENT SOLUTIONS

Explicit interfaces to manage consistency

- **NV-Heaps [ASPLOS'11], BPFS [SOSP'09], Mnemosyne [ASPLOS'11]**

Example Code
update a node in a persistent hash table

```
void hashtable_update(hashtable_t* ht,
                      void *key, void *data)
{
    list_t* chain = get_chain(ht, key);
    pair_t* pair;
    pair_t updatePair;
    updatePair.first = key;
    pair = (pair_t*) list_find(chain,
                               &updatePair);
    pair->second = data;
}
```

CURRENT SOLUTIONS

```
void TMhashtable_update(TMARCGDECL
hashtable_t* ht, void *key,
void*data){
  list_t* chain = get_chain(ht, key);
  pair_t* pair;
  pair_t updatePair;
  updatePair.first = key;
  pair = (pair_t*) TMLIST_FIND(chain,
                     &updatePair);
  pair->second = data;
}
```

CURRENT SOLUTIONS

Manual declaration of persistent components

```
void TMhashtable_update(TMARCGDECL
hashtable_t* ht, void *key,
void*data){
  list_t* chain = get_chain(ht, key);
  pair_t* pair;
  pair_t updatePair;
  updatePair.first = key;
  pair = (pair_t*) TMLIST_FIND(chain,
                    &updatePair);
  pair->second = data;
}
```

CURRENT SOLUTIONS

Manual declaration of persistent components

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void TMhashtable_update(TMARGDECL
hashtable_t* ht, void *key,
void*data){
  list_t* chain = get_chain(ht, key);
  pair_t* pair;
  pair_t updatePair;
  updatePair.first = key;
  pair = (pair_t*) TMLIST_FIND(chain,
                    &updatePair);
  pair->second = data;
}
```

Need a new implementation

CURRENT SOLUTIONS

Manual declaration of persistent components

```
void TMhashtable_update(TMARCGDECL
hashtable_t* ht, void *key,
void*data){
  list_t* chain = get_chain(ht, key);
  pair_t* pair;
  pair_t updatePair;
  updatePair.first = key;
  pair = (pair_t*) TMLIST_FIND(chain,
                              &updatePair);
  pair->second = data;
}
```

Need a new implementation

Third party code can be inconsistent

CURRENT SOLUTIONS

Manual declaration of persistent components

```
void TMhashtable_update(TMARCGDECL
hashtable_t* ht, void *key,
void*data){
  list_t* chain = get_chain(ht, key);
  pair_t* pair;
  pair_t updatePair;
  updatePair.first = key;
  pair = (pair_t*) TMLIST_FIND(chain,
                             &updatePair);
  pair->second = data;
}
```

Need a new implementation

Prohibited Operation `=`

Third party code can be inconsistent

Burden on the programmers

OUR APPROACH: ThyNVM

Goal:
Software transparent consistency in persistent memory systems

Key Idea:
**Periodically checkpoint state; recover to previous checkpt on crash**

ThyNVM: Summary

A new hardware-based checkpointing mechanism

- **Checkpoints** at *multiple granularities* to reduce both checkpointing latency and metadata overhead

- **Overlaps** *checkpointing* and *execution to* reduce checkpointing latency

- **Adapts** to *DRAM and NVM* characteristics

Performs within 4.9% of an *idealized DRAM* with zero cost consistency

2. OVERLAPPING CHECKPOINTING AND EXECUTION

time
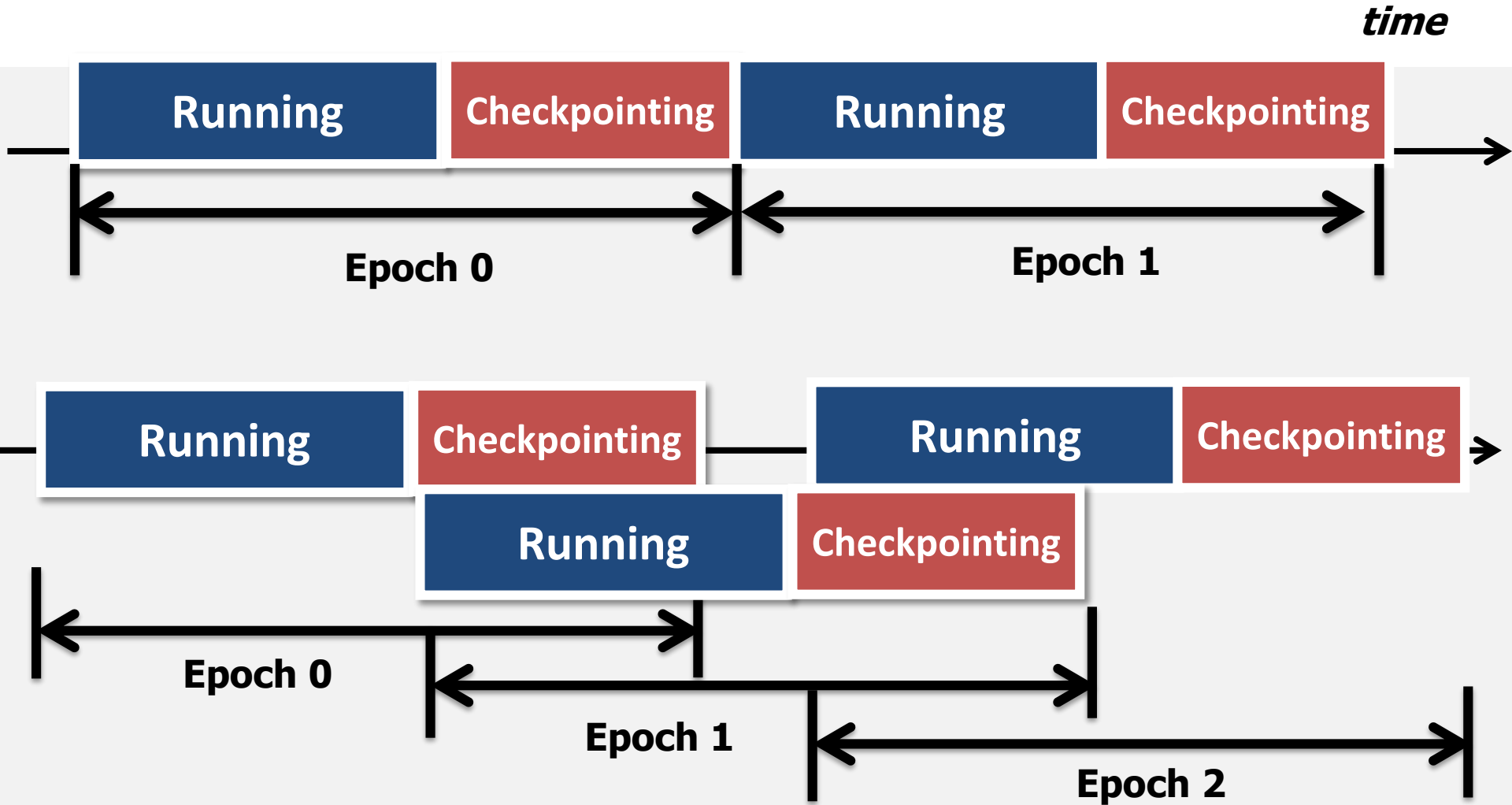
More About ThyNVM

- Jinglei Ren, Jishen Zhao, Samira Khan, Jongmoo Choi, Yongwei Wu, and Onur Mutlu,
"ThyNVM: Enabling Software-Transparent Crash Consistency in Persistent Memory Systems"
Proceedings of the 48th International Symposium on Microarchitecture (**MICRO**), Waikiki, Hawaii, USA, December 2015.
[Slides (pptx) (pdf)] [Lightning Session Slides (pptx) (pdf)] [Poster (pptx) (pdf)]
[Source Code]

ThyNVM: Enabling Software-Transparent Crash Consistency in Persistent Memory Systems

Jinglei Ren[*†]   Jishen Zhao[‡]   Samira Khan[†′]   Jongmoo Choi[+†]   Yongwei Wu[*]   Onur Mutlu[†]

[†]Carnegie Mellon University   [*]Tsinghua University
[‡]University of California, Santa Cruz   [′]University of Virginia   [+]Dankook University

Programming Ease
to Exploit Persistence

Tools/Libraries to Help Programmers

- Himanshu Chauhan, Irina Calciu, Vijay Chidambaram, Eric Schkufza, Onur Mutlu, and Pratap Subrahmanyam,
"NVMove: Helping Programmers Move to Byte-Based Persistence"
*Proceedings of the 4th Workshop on Interactions of NVM/Flash with Operating Systems and Workloads (**INFLOW**)*, Savannah, GA, USA, November 2016.
[Slides (pptx) (pdf)]

NVMOVE: Helping Programmers Move to Byte-Based Persistence

Himanshu Chauhan *
UT Austin

Irina Calciu
VMware Research Group

Vijay Chidambaram
UT Austin

Eric Schkufza
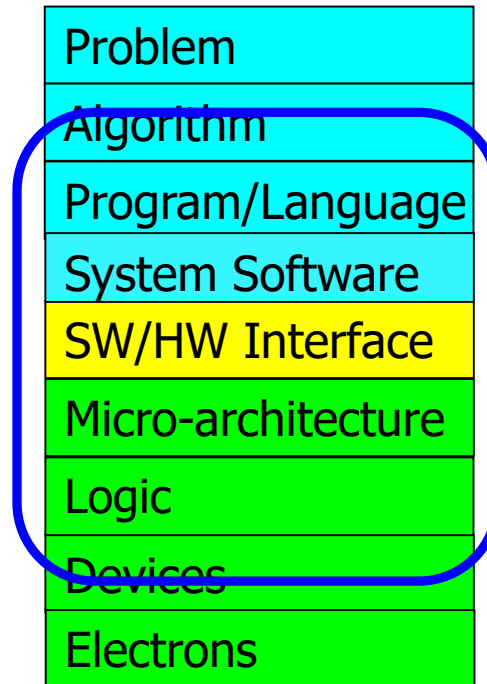VMware Research Group

Onur Mutlu
ETH Zürich

Pratap Subrahmanyam
VMware

The Future of Emerging Technologies is Bright

- **Regardless of challenges**
  - in underlying technology and overlying problems/requirements

Can enable:

- Orders of magnitude improvements

- New applications and computing systems

Problem
Algorithm
Program/Language
System Software
SW/HW Interface
Micro-architecture
Logic
Devices
Electrons

Yet, we have to

- Think across the stack

- Design enabling systems

If In Doubt, Refer to Flash Memory

- A very "doubtful" emerging technology
  - for at least two decades

Proceedings of the IEEE, Sept. 2017

INVITED PAPER

Error Characterization, Mitigation, and Recovery in Flash-Memory-Based Solid-State Drives

By Yu Cai, Saugata Ghose, Erich F. Haratsch, Yixin Luo, and Onur Mutlu

ABSTRACT | NAND flash memory is ubiquitous in everyday life today because its capacity has continuously increased and

Many Research & Design Opportunities

- Enabling completely persistent memory

- Computation in/using NVM based memories

- Hybrid memory systems

- Security and privacy issues in persistent memory

- Reliability and endurance related problems

- ...