A Case for Richer Cross-layer Abstractions: Bridging the Semantic Gap with Expressive Memory

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Published in ISCA 2018

Presented by Philippe Voinov
Background

- ISAs traditionally only convey program functionality
- High-level program semantics never reach hardware
Background - Cache tiling

Image from video “Matrix multiplication: tiled implementation” https://www.youtube.com/watch?v=aMvCEEBIBto
Background - DRAM system structure

- DRAM systems have a very hierarchical structure
- Distributing load well throughout this structure can have performance benefits

Background - Implications

- OS and hardware try to predict program behavior
- Compilers and programmers may try to optimize for architecture
Previous work

- Fine-grained hints as ISA instructions
- Program annotations to convey semantics
- Hardware-software co-designs
Problem

- Optimizing program execution is difficult without hints
- Fine-grained hints require large changes for each optimization
- Platform-specific directives are not portable
Goal

Create a general cross-layer interface to communicate higher-level program semantics to various system components.
Novelty of XMem

- Can pass information used for multiple optimizations
- Describes properties of data, rather than directive for hardware
- Is highly extensible
Key approach - Example

\[
A = \text{malloc}(\text{size}); \\
\text{Atom1} = \text{CreateAtom}(\text{"INT"}, \text{"Regular"}, \ldots); \\
\text{MapAtom}(\text{Atom1}, A, \text{size}); \\
\text{ActivateAtom}(\text{Atom1}); \\
\ldots \\
\text{Atom2} = \text{CreateAtom}(\text{"INT"}, \text{"Irregular"}, \ldots); \\
\text{UnMapAtom}(\text{Atom1}, A, \text{size}); \\
\text{MapAtom}(\text{Atom2}, A, \text{size}); \\
\text{ActivateAtom}(\text{Atom2});
\]
Key approach - Atoms

- Atoms describe data which is semantically similar
- Programs explicitly specify atoms
- Atoms are immutable
- Atoms can be mapped to memory or deactivated
- Each virtual address maps to at most one atom
Key approach - Attributes of an atom

- Paper defines a specific set of attributes, but this can be extended
- *Data value properties* (eg. float32, sparse)
- *Access properties* (eg. accessed with specific stride, read only)
- *Data locality properties* (working set size and reuse for caching)
Mechanisms - Overview

Figure 3: XMem: Overview of the components.
Key approach - Design choices

- Minimize runtime overhead of tracking and retrieving semantics
- Summarize atoms in software, track in hardware
- **Centralized tracking**: Atoms have an ID that the entire system recognizes
- **Attribute translation**: OS simplifies attributes for each hardware component
Mechanisms - XMemLib

- **CreateAtom**
  - Compiler populates the atom segment with passed attributes
  - OS loads the atom segment

- **MapAtom and UnMapAtom**
  - Translated to dedicated ISA instructions
  - AMU modifies the Atom Address Map

- **ActivateAtom and DeactivateAtom**
  - Translated to dedicated ISA instructions
  - AMU modifies the Atom Status Table
Mechanisms - malloc

- Optimizations may require data placed at specific location in physical memory
- OS must know about atoms when allocating memory
- Atom ID is passed by compiler to malloc, and by malloc to the OS

\[
\begin{align*}
    A &= \text{malloc} (\text{size}) ; \\
    \text{AtomMap}(\text{atomID}, A, \text{size}) &\quad \leftrightarrow \quad A &= \text{malloc} (\text{size}, \text{atomID}) ; \\
    \text{AtomMap}(\text{atomID}, A, \text{size})
\end{align*}
\]
Mechanisms - Atom Address Map (AAM)

- Uses PA instead of VA to simplify table design
- 512 byte granularity by default (~0.2% storage overhead)
- Continuous list of atom IDs indexed by physical address
Mechanisms - Atom Management Unit (AMU)

- Hardware unit which manages the AAM and AST
- Handles ATOM_(UN)MAP and ATOM_(DE)ACTIVATE
- Handles ATOM_LOOKUP and has a lookaside buffer
Key results - Methodology

- XMem modelled in zsim and evaluated with DRAMSim2
- Two separate use cases evaluated

<table>
<thead>
<tr>
<th>Table 3: Simulation configuration for Use Case 1.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
</tr>
<tr>
<td>3.6 GHz, Westmere-like [82] OOO, 4-wide issue,</td>
</tr>
<tr>
<td>128-entry ROB, 32-entry LQ and SQ</td>
</tr>
<tr>
<td>L1 Cache</td>
</tr>
<tr>
<td>32KB Inst and 32KB Data, 8 ways, 4 cycles, LRU</td>
</tr>
<tr>
<td>L2 Cache</td>
</tr>
<tr>
<td>128KB private per core, 8 ways, 8 cycles, DRRIP [83]</td>
</tr>
<tr>
<td>L3 Cache</td>
</tr>
<tr>
<td>8MB (1MB/core, partitioned), 16 ways, 27 cycles, DRRIP</td>
</tr>
<tr>
<td>Prefetcher</td>
</tr>
<tr>
<td>Multi-stride prefetcher [33] at L3, 16 strides</td>
</tr>
<tr>
<td>DRAM</td>
</tr>
<tr>
<td>DDR3-1066, 2 channels, 1 rank/channel, 8 banks/rank,</td>
</tr>
<tr>
<td>17GB/s (2.1GB/s/core), FR-FCFS [84], open-row policy [85]</td>
</tr>
</tbody>
</table>
Key results - Case 1 - Cache management

- Tests run against the Polybench suite
- Cache tiling optimization performed by PLUTO (polyhedral locality optimizer)
- XMem provides information on
  - Access pattern and intensity
  - Data reuse and working set size
- The hardware cache will
  - Prioritize keeping high-reuse data in the cache
  - Pin part of the working set if it doesn’t fully fit in cache
- The prefetcher will
  - Prefetch data based on the provided access patterns
Key results - Case 1 - Cache management

- Choosing too small tile size causes ~30% slowdown on average
- Choosing too large tile size causes thrashing (~65% slowdown)
- XMem reduces thrashing for ~25% slowdown

Figure 4: Execution time across different tile sizes (normalized to Baseline with the smallest tile size).
Key results - Case 1 - Cache management

- Both prefetching and pinning improvements contribute to performance.

**Figure 6:** XMem’s speedup over Baseline with different memory bandwidth availability.
Key results - Case 2 - Data placement in DRAM

- Different set of workloads than in case 1
- XMem provides information on access pattern and intensity
- System provides information on DRAM configuration
- Goal is to improve RBL and MLP
- The OS will
  - Isolate high RBL data structures in their own banks
  - Spread out other data structures evenly
- Baseline system uses randomized virtual-to-physical address mapping
Key results - Case 2 - Data placement in DRAM

- XMem based DRAM placement improves runtime by ~8.5% on average
- Reduces read latency by ~12% on average
- Works by improving row buffer locality and memory level parallelism

Figure 7: Speedup w/ XMem-based DRAM placement.
Summary - XMem

● Problem
  ○ Optimizing program execution is difficult without hints
  ○ Fine-grained hints require large changes for each optimization
  ○ Platform-specific directives are not portable

● Goal
  ○ Create a general cross-layer interface to communicate higher-level program semantics

● Result - XMem
  ○ Enables performant memory optimizations using high-level information
  ○ Uses the atom abstraction to describe semantics of data
  ○ More general and versatile than past work
  ○ Low overhead by pre-processing in software and tracking in hardware
Strengths

- Simple and well explained concept
- Low overhead implementation with significant benefits
- Adopting XMem in future systems seems realistic
Weaknesses

- Unclear why both MAP and ACTIVATE are necessary
- Unclear which cache setup was used in tests
- XMem tightly couples guest and host in virtualized environments
- Effects of remapping atoms on malloc-integration not explored
Questions and discussion
Thoughts and discussion

- Could a similarly general and declarative approach be used for non-memory-related optimizations?
- Could the ACTIVATE/DEACTIVATE concept be removed entirely?
- Which XMem attributes could be inferred by a compiler? How effective would that be compared to a programmer specifying attributes?