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Paper Review of ‘A2: Analog Malicious Hardware’

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A2: Analog Malicious Hardware

Kaiyuan Yang, Matthew Hicks, Qing Dong, Todd Austin, Dennis Sylvester

University of Michigan

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A2: Analog Malicious Hardware

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***Abstract*—While the move to smaller transistors has been a boon for performance it has dramatically increased the cost to fabricate chips using those smaller transistors. This forces the vast majority of chip design companies to trust a third party—often overseas—to fabricate their design. To guard against shipping chips with errors (intentional or otherwise) chip design companies rely on post-fabrication testing. Unfortunately, this type of testing leaves the door open to malicious modifications since attackers can craft attack triggers requiring a sequence of unlikely events, which will never be encountered by even the most diligent tester.**

In this paper, we show how a fabrication-time attacker can leverage analog circuits to create a hardware attack that is small (i.e., requires as little as one gate) and stealthy (i.e., requires an unlikely trigger sequence before effecting a chip's functionality). In the open spaces of an already placed and routed design, we construct a circuit that uses capacitors to siphon charge from nearby wires as they transition between digital values. When the capacitors fully charge, they deploy an attack that forces a victim flip-flop to a desired value. We weaponize this attack into a remotely-controllable privilege escalation by attaching the capacitor to a wire controllable and by selecting a victim flip-flop that holds the privilege bit for our processor. We implement this attack in an OR1200 processor and fabricate a chip. Experimental results show that our attacks work, show that our attacks elude activation by a diverse set of benchmarks, and suggest that our attacks evade known defenses.

***Keywords*-analog; attack; hardware; malicious; security; Trojan;**

I. Introduction

Hardware is the base of a system. All software executes on top of a processor. That software must trust that the hardware faithfully implements the specification. For many types of hardware flaws, software has no way to check if something went wrong [1], [2]. Even worse, if there is an attack in hardware, it can contaminate all layers of a system that depend on that hardware—violating high-level security policies correctly implemented by software.

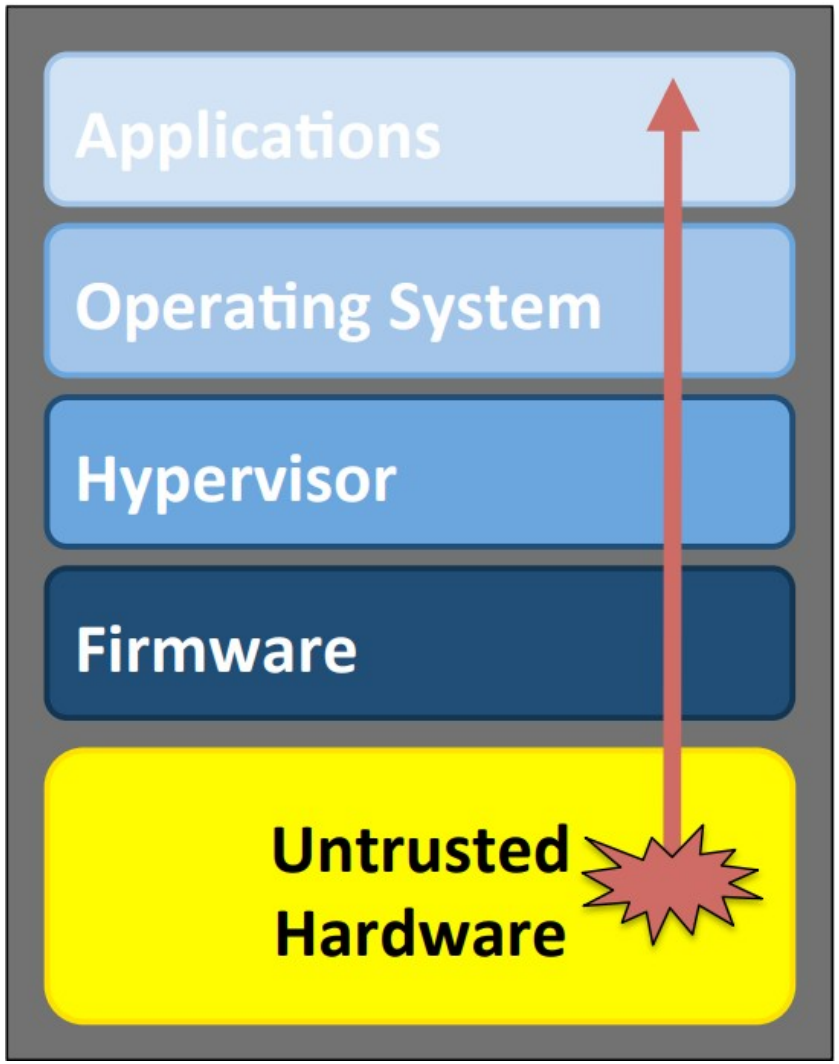
The trend of smaller transistors while beneficial for increased performance and lower power, has made fabricating a chip expensive. With every generation of transistor comes the cost of retooling for that smaller transistor. For example, it costs 15% more to setup the fabrication line for each successive process node and by 2020 it is expected that setting-up a fabrication line for the smallest transistor size will require a $20,000,000,000 upfront investment [3]. To amortize the cost of the initial tooling required to support a given transistor size, most hardware companies outsource fabrication.

Outsourcing of chip fabrication opens-up hardware to attack. The most pernicious fabrication-time attack is the dopant-level Trojan [4], [5]. Dopant-level Trojans convert trusted circuitry into malicious circuitry by changing the dopant ratio on the input pins to victim transistors. This effectively ties the input of the victim transistors to a logic level 0 or 1—a short circuit. Converting existing circuits makes dopant-level Trojans very difficult to detect since there are no added or removed gates or wires. In fact, detecting dopant-level Trojans requires a complete chip delayering and comprehensive imaging with a scanning electron microscope [6]. Unfortunately, this elusiveness comes at the cost of expressiveness. Dopant-level Trojans are limited by existing circuits, making it difficult to implement sophisticated attack triggers [5]. The lack of a sophisticated trigger means that dopant-level Trojans are more detectable by post-fabrication functional testing. Thus, dopant-level Trojans represent an extreme on a tradeoff space between detectability during physical inspection and detectability during testing.

To defend against malicious hardware inserted during fabrication, researchers have proposed two fundamental defenses: 1) use side-channel information (e.g., power and temperature) to characterize acceptable behavior in an effort to detect anomalous (i.e., malicious) behavior [7]–[10] and 2) add sensors to the chip that measure and characterize features of the chip's behavior (e.g., signal propagation delay) in order to identify dramatic changes in those features (presumably caused by activation of a malicious circuit) [11]–[13]. Using side channels as a defense works well against large Trojans added to purely combinational circuits where it is possible to test all inputs and there exists a reference chip to compare against. While this accurately describes most existing fabrication-time attacks, we show that it is possible to implement a stealthy and powerful processor attack using only a single added gate. Adding sensors to the design would seem to adapt the side-channel approach to more complex, combinational circuits, but we design an attack that operates in the analog domain until it directly modifies processor

Background

Why Secure Hardware Matters



A system with insecure hardware means an insecure system

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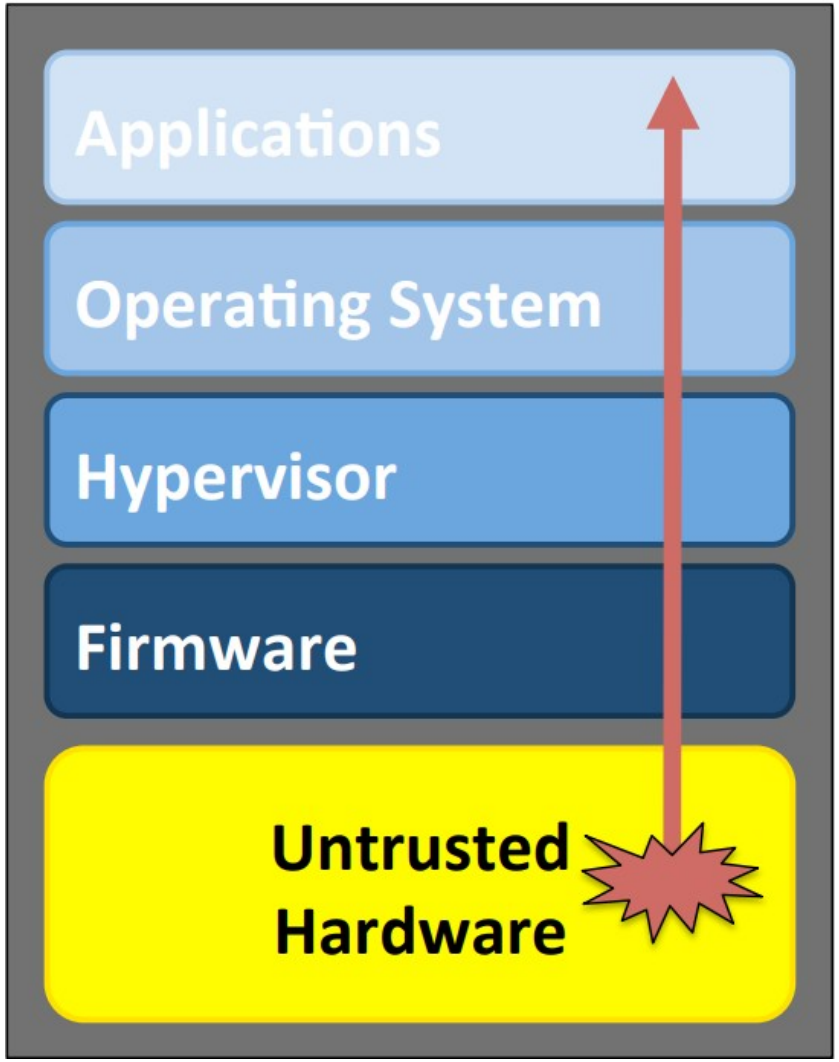

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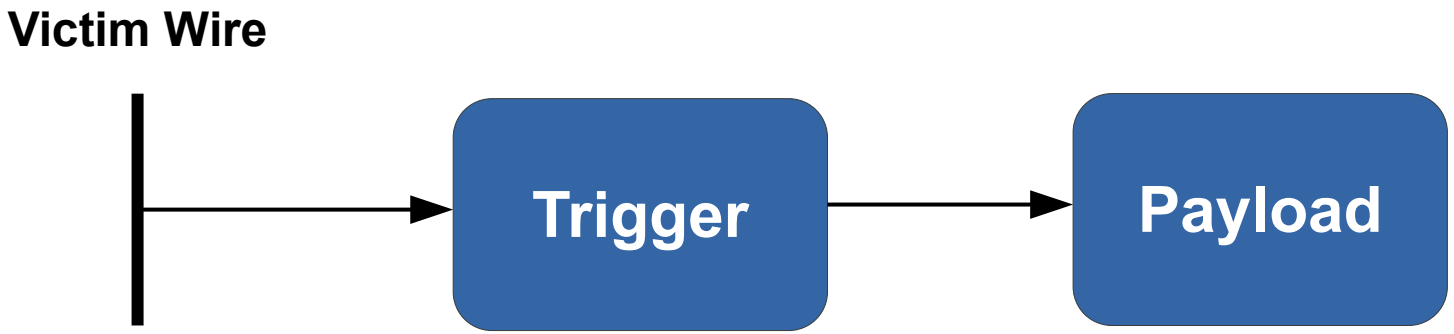
How does a hardware attack work?

Typical Trigger Based Hardware Attacks



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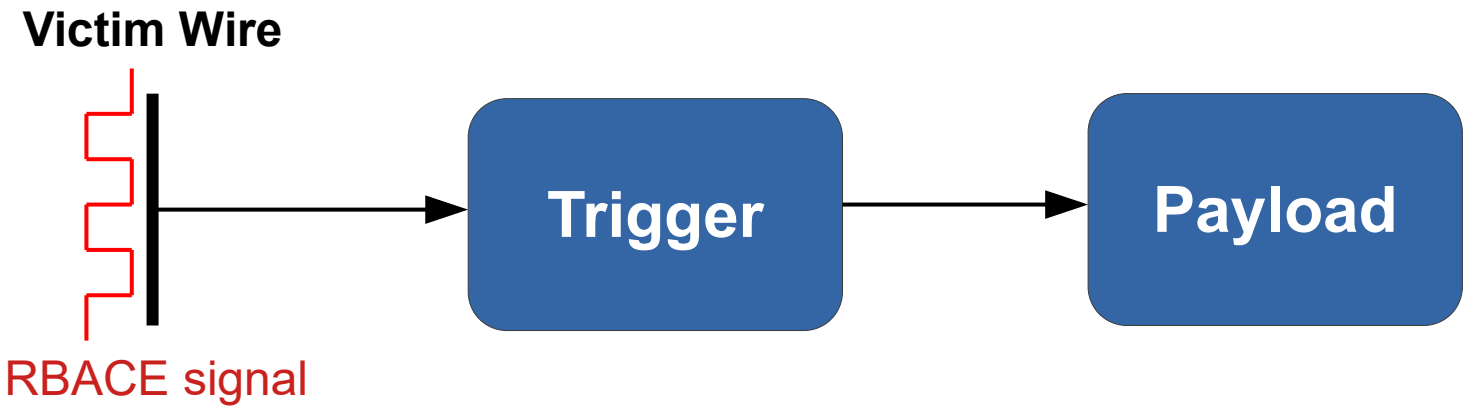

Rare, **B**ut **A**ttacker **C**ontrollable **E**vent

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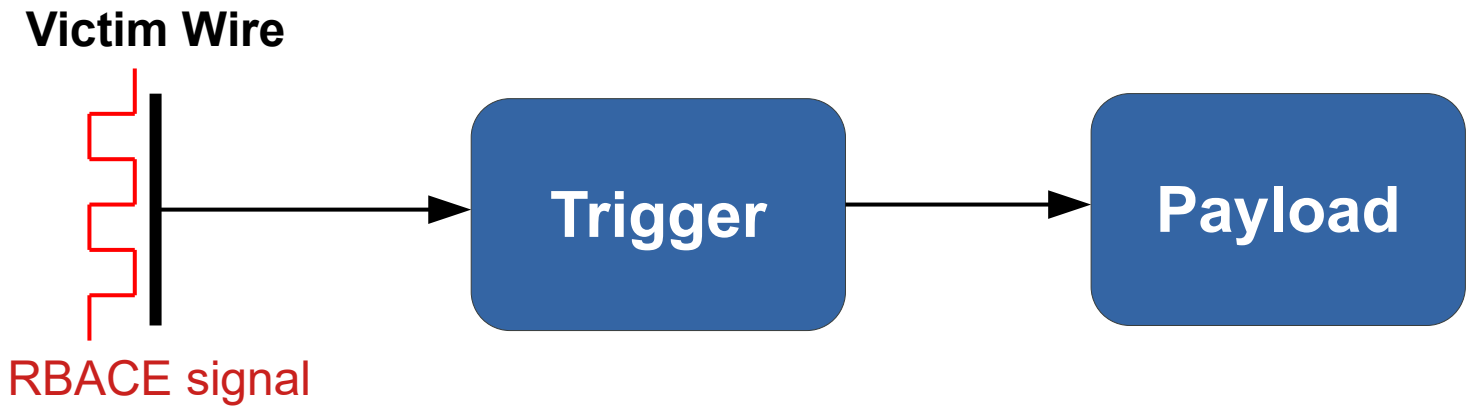

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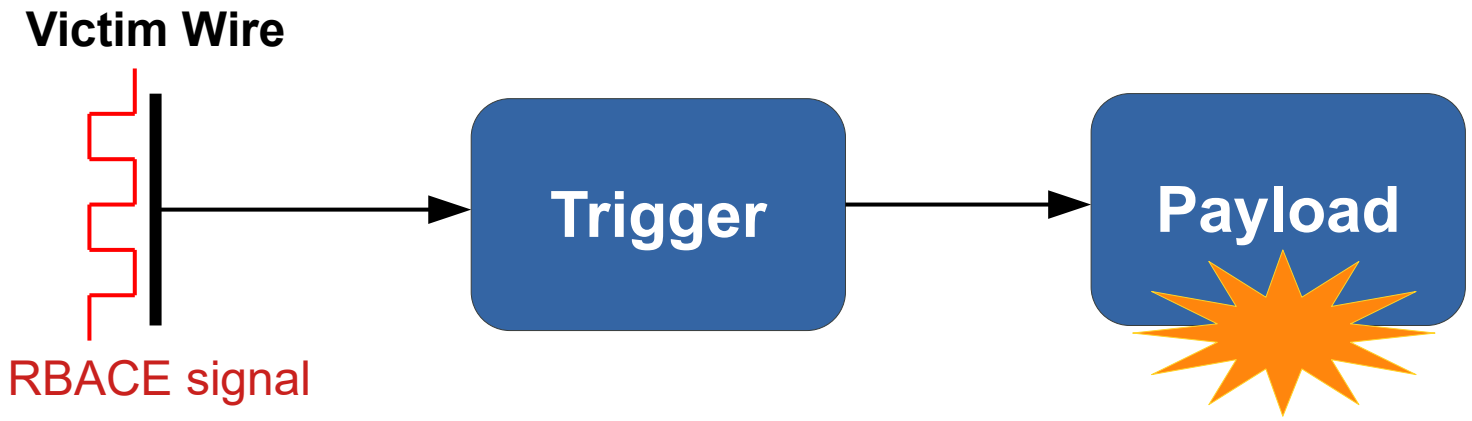

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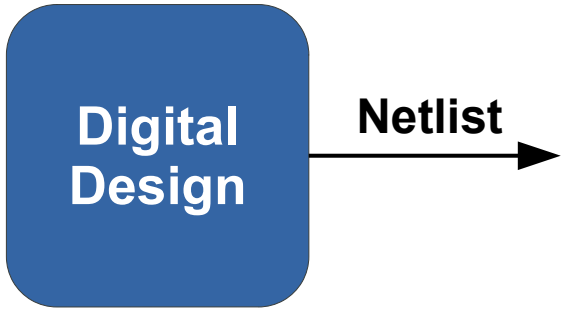

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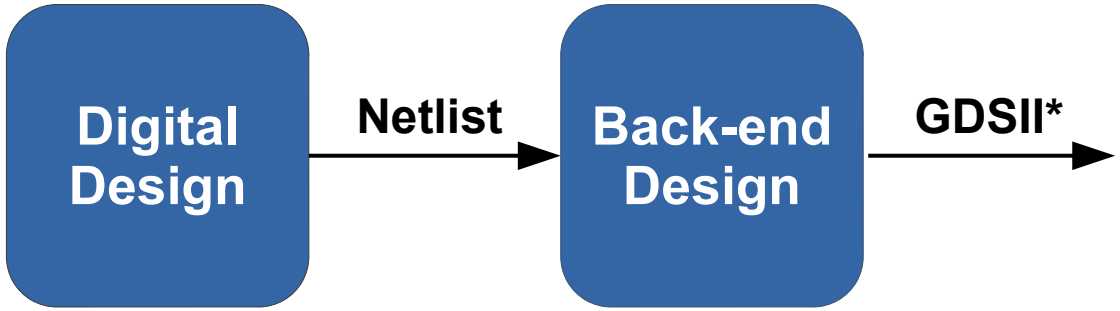

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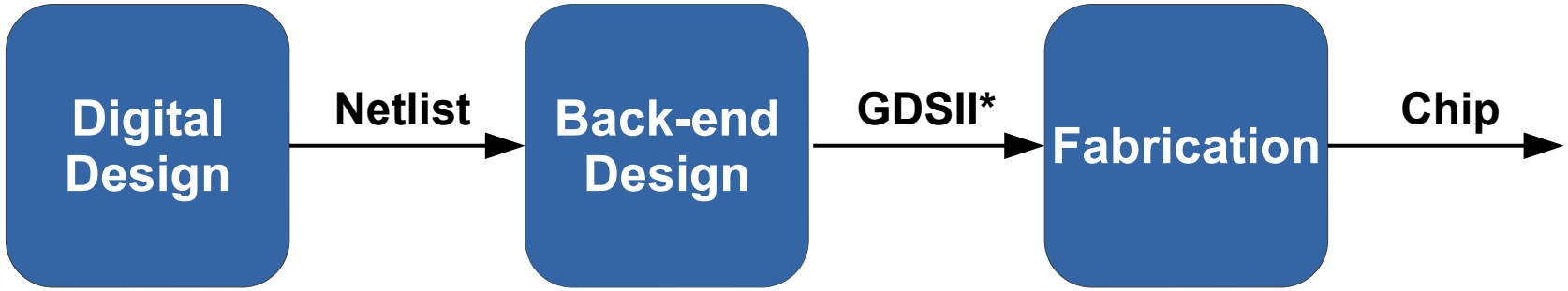

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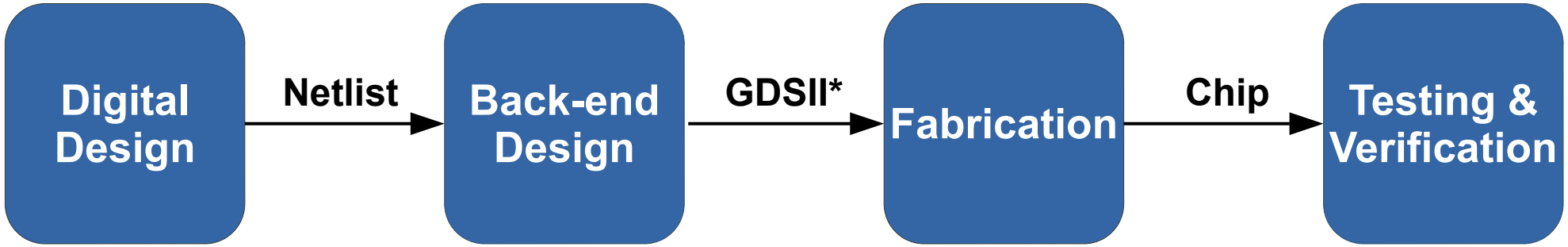

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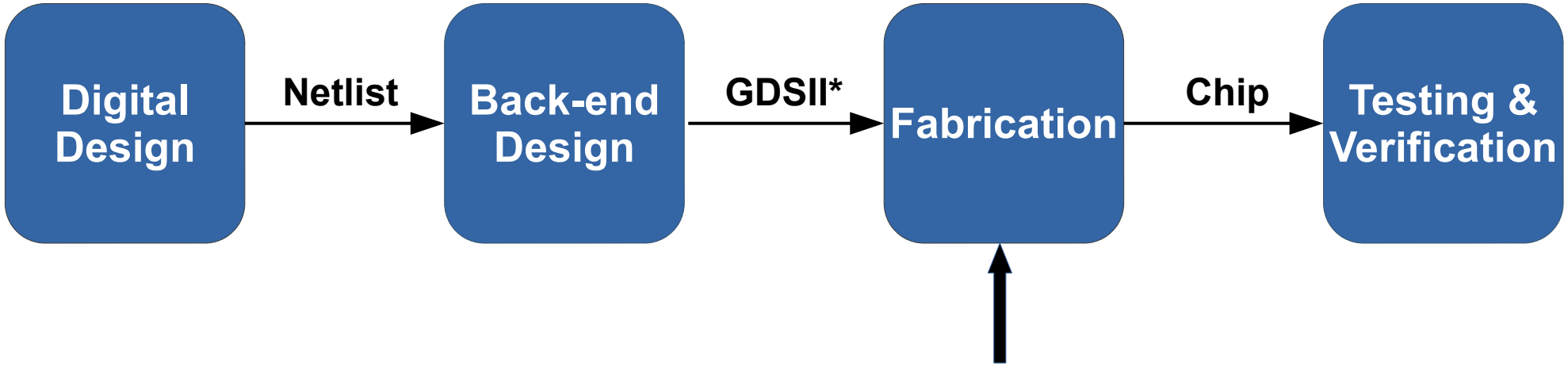

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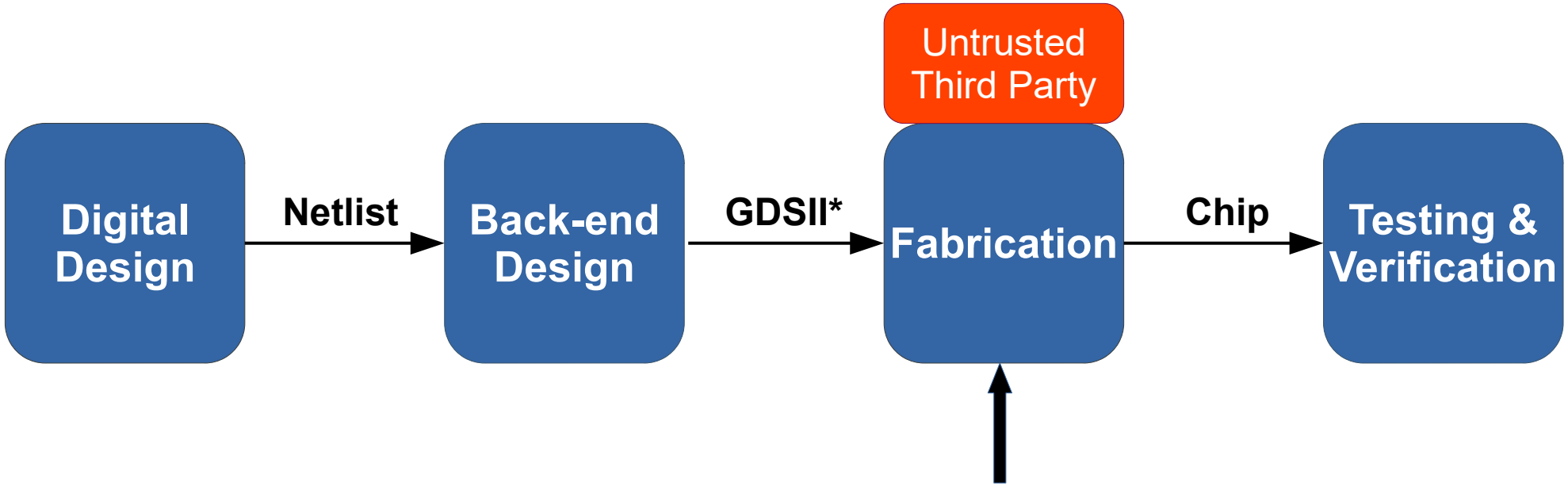

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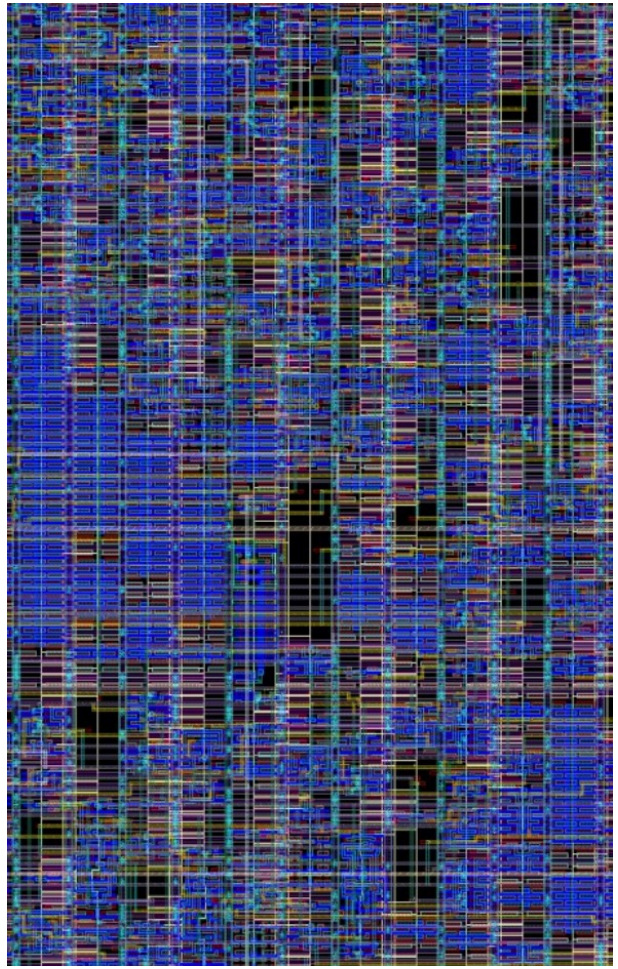

Example GDSII layout with free space

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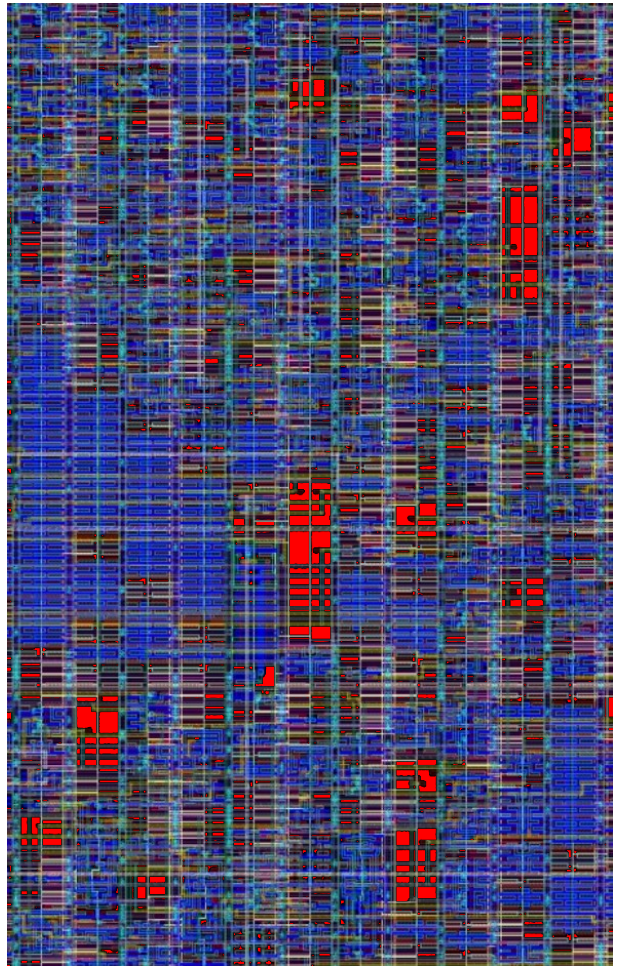

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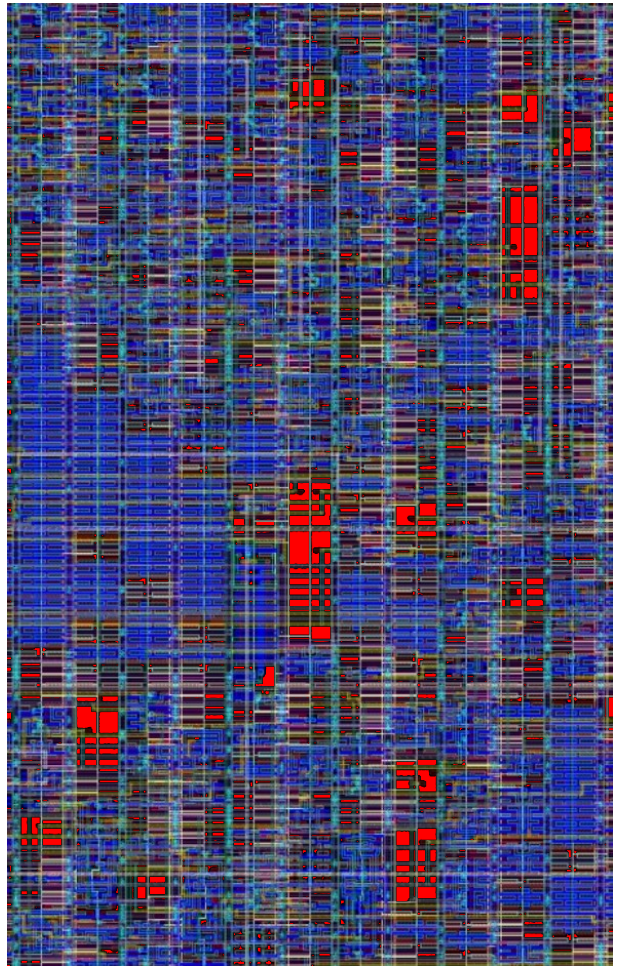

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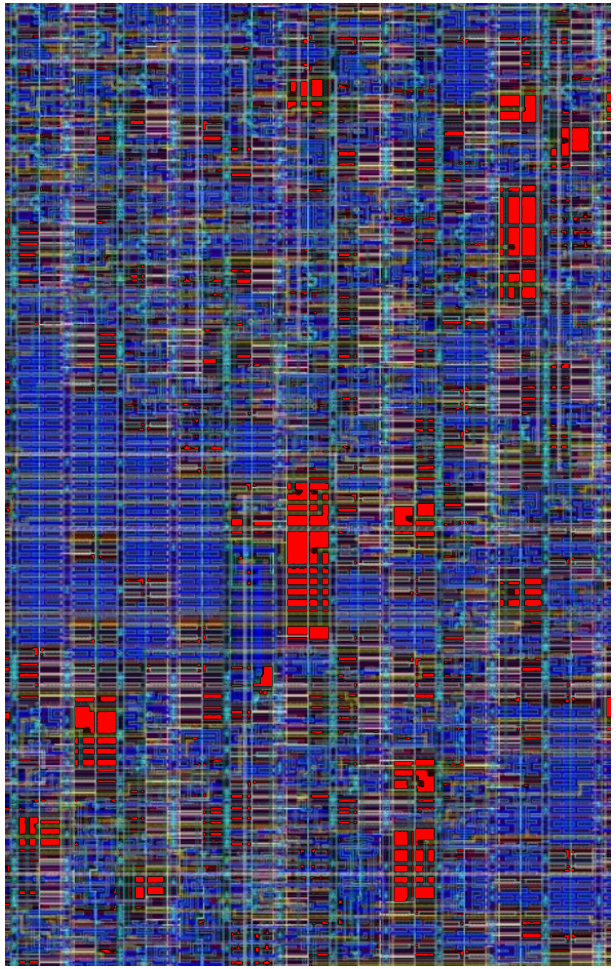
Opens up possibility for attackers to embed malicious hardware



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Issues With Existing Hardware Attacks

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Can We Do Better?

Is there a better hardware attack that does not suffer from these issues?

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How can it work?

Goal

Goal of the Paper

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Stealthy

Threat Model for the Attack

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Threat Model for the Attack

Goal

- Attack implemented at time of **fabrication**
- The attacker has only access to a **correctly implemented GDSII** file
- The attacker **cannot change dimensions** or move stuff around
- The attacker has **no knowledge over tests** conducted on the chip

Novelty

Previous Approaches of Hardware Attacks

Novelty

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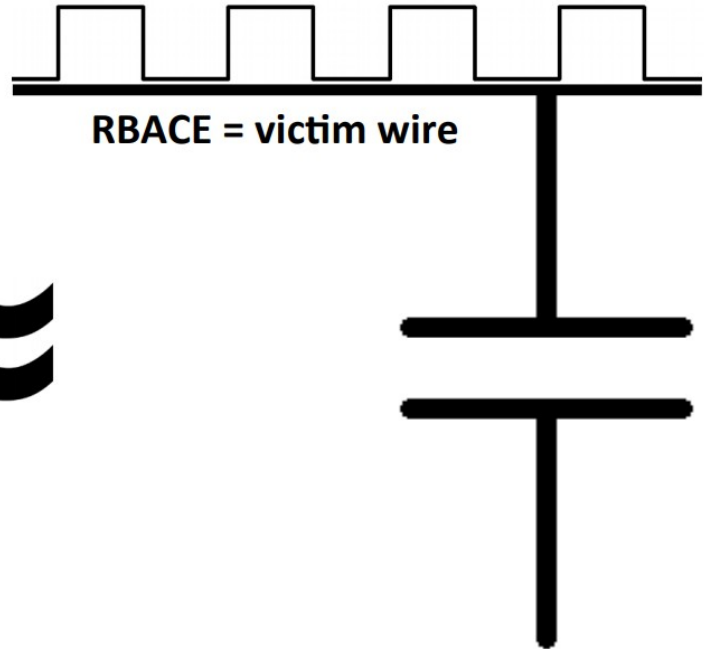

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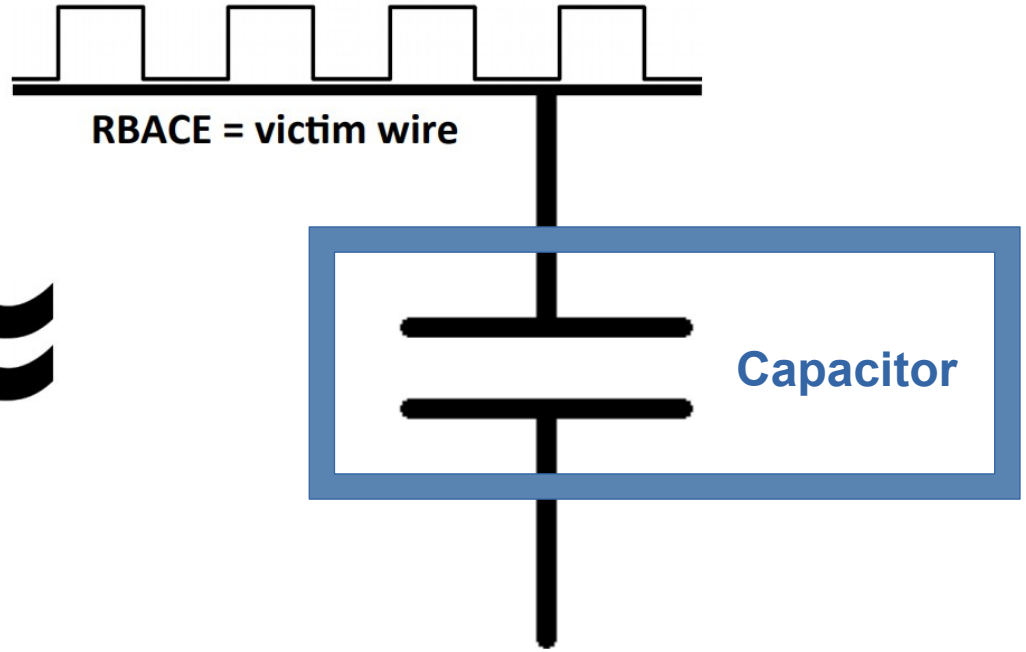

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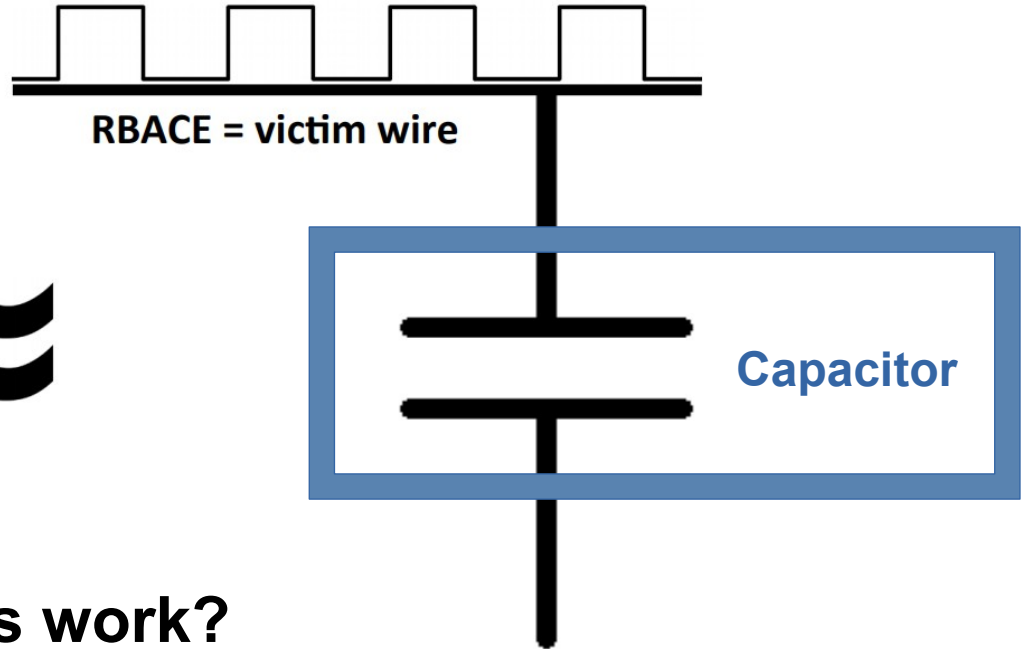
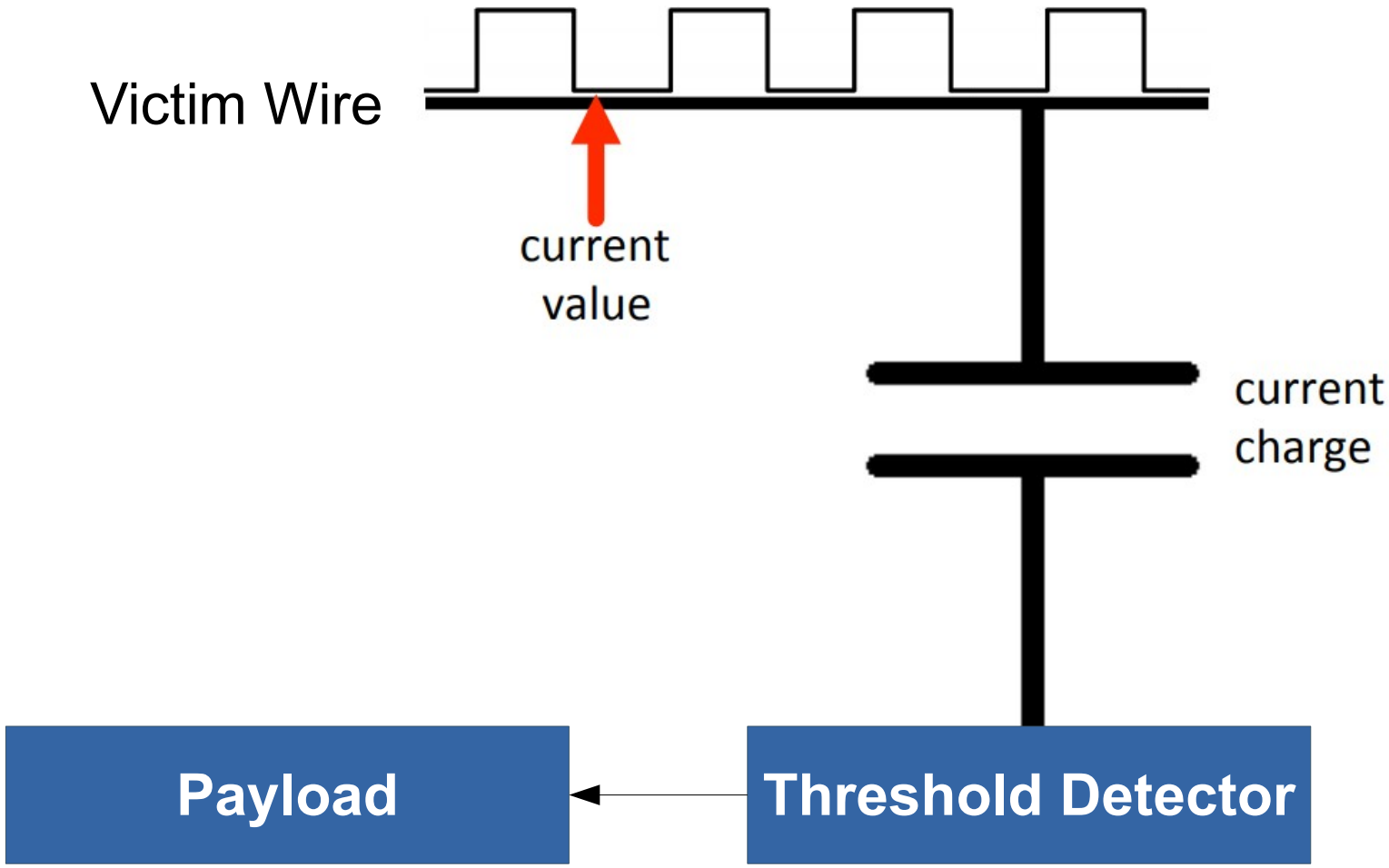


How does this work?

Key Approach & Ideas

How does A2 work?



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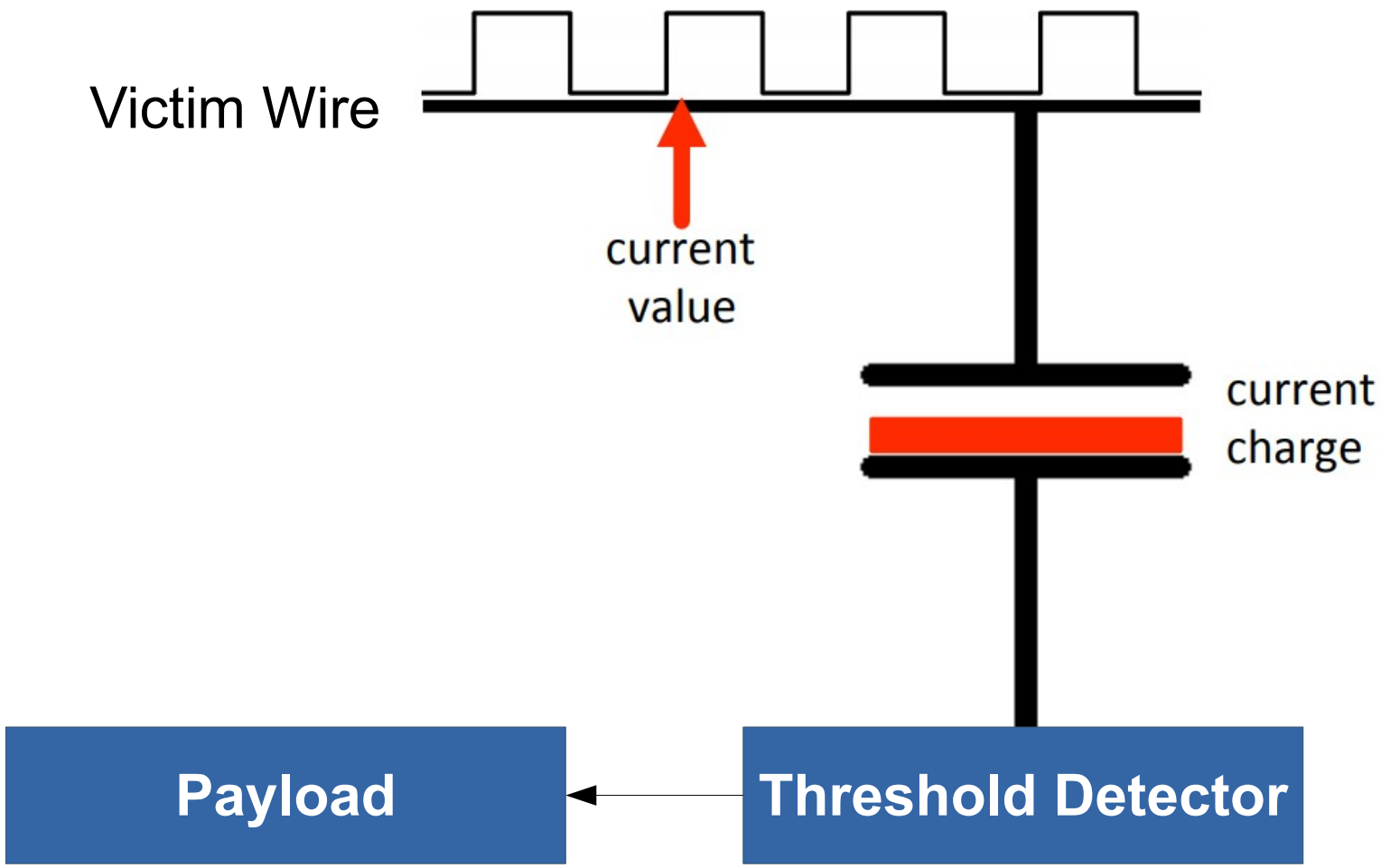

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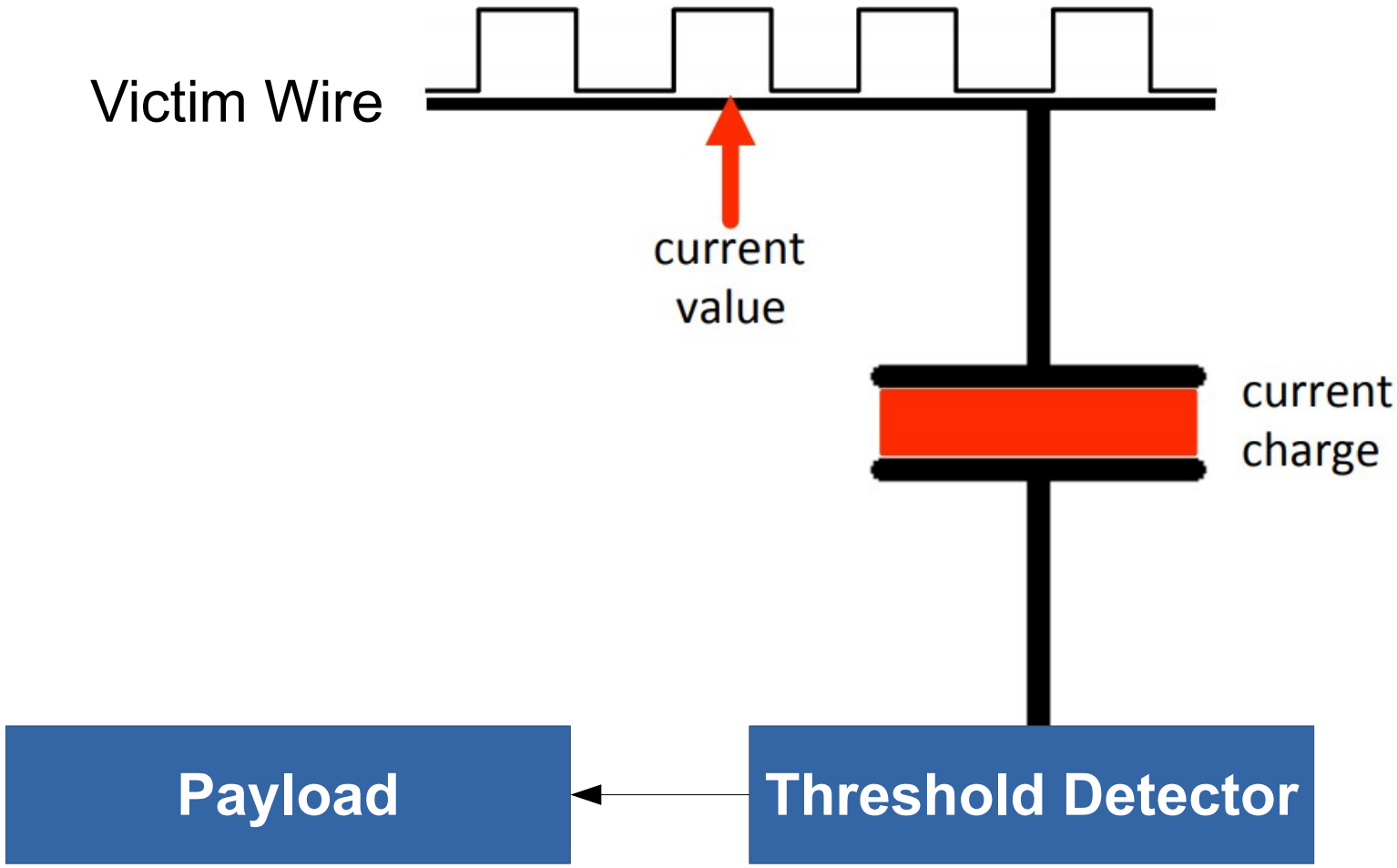

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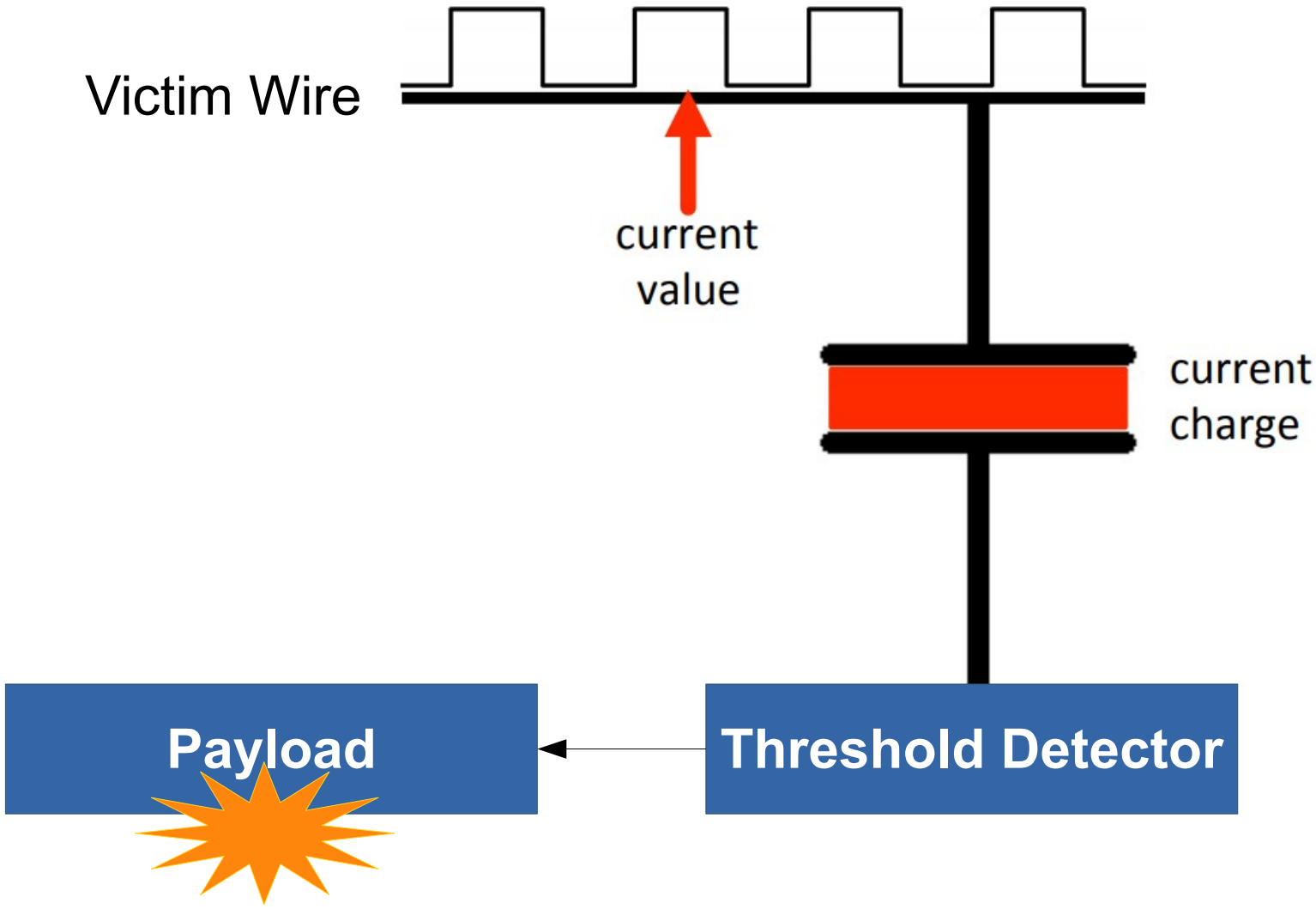
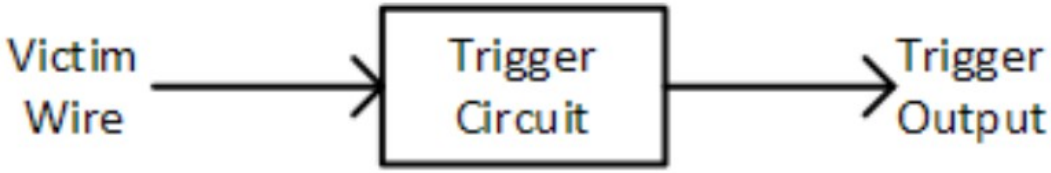
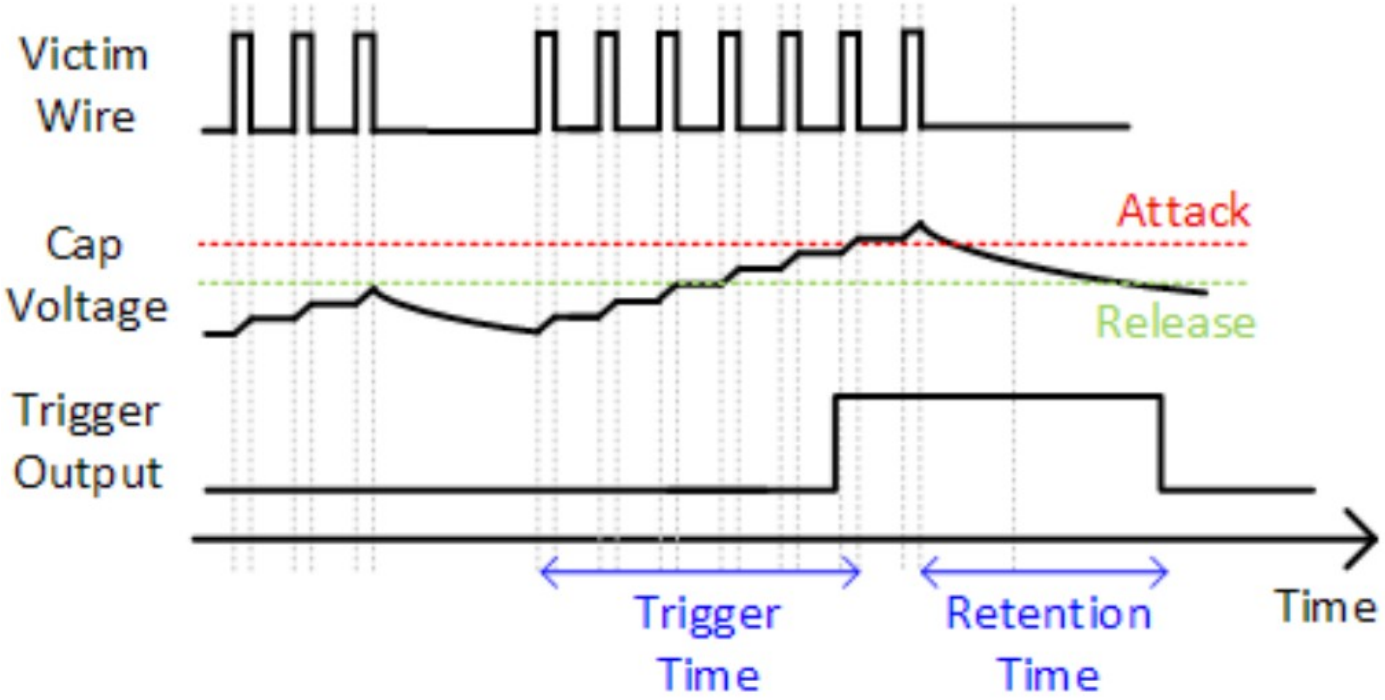


Mechanism in Detail

The Analog Trigger Circuit





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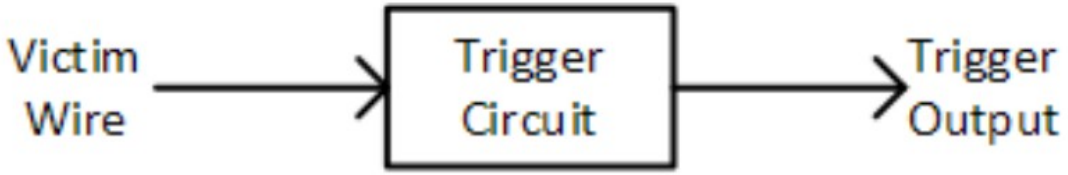

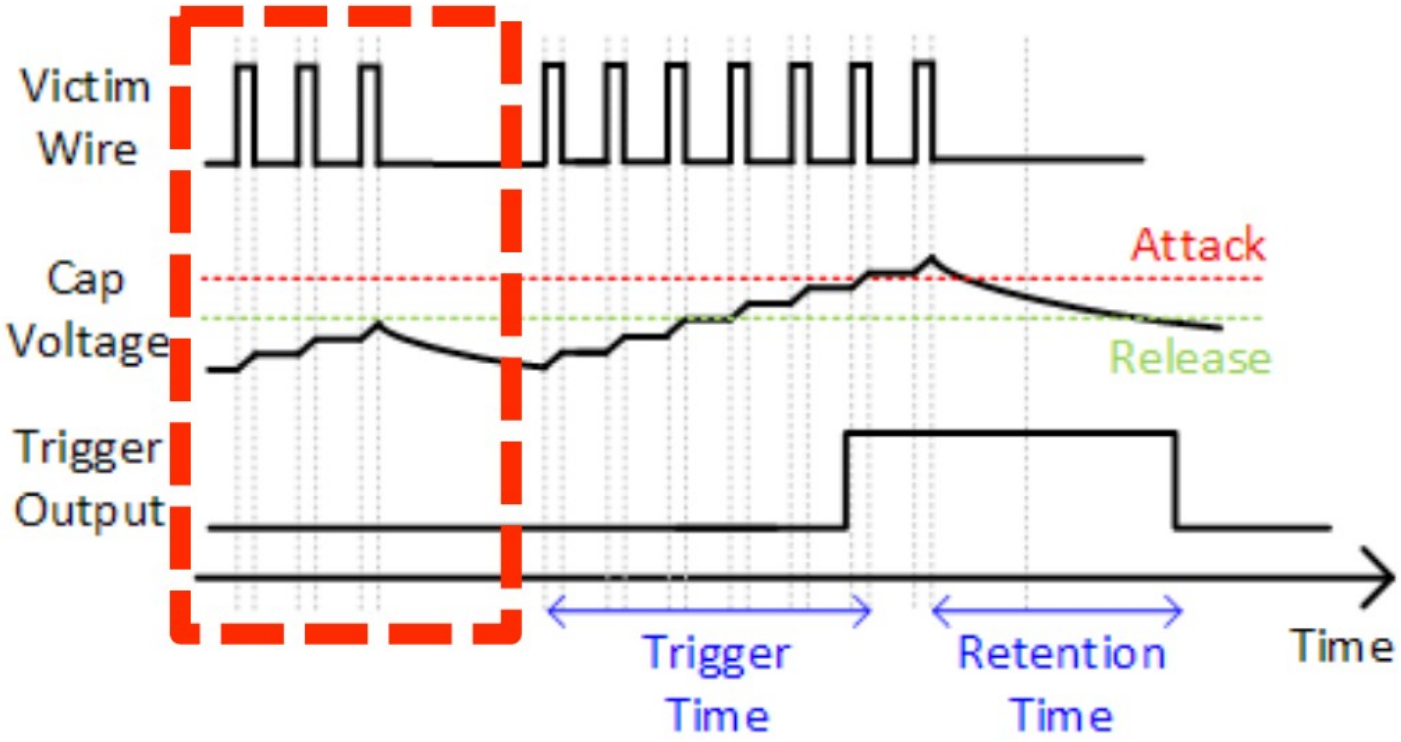

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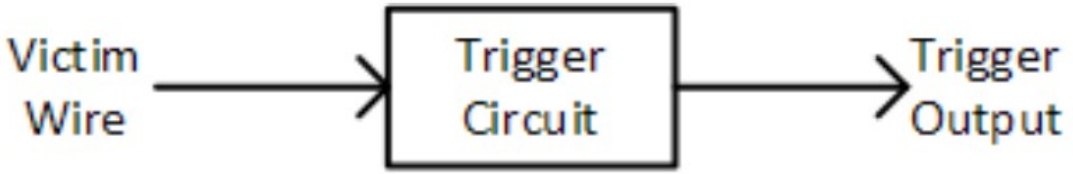

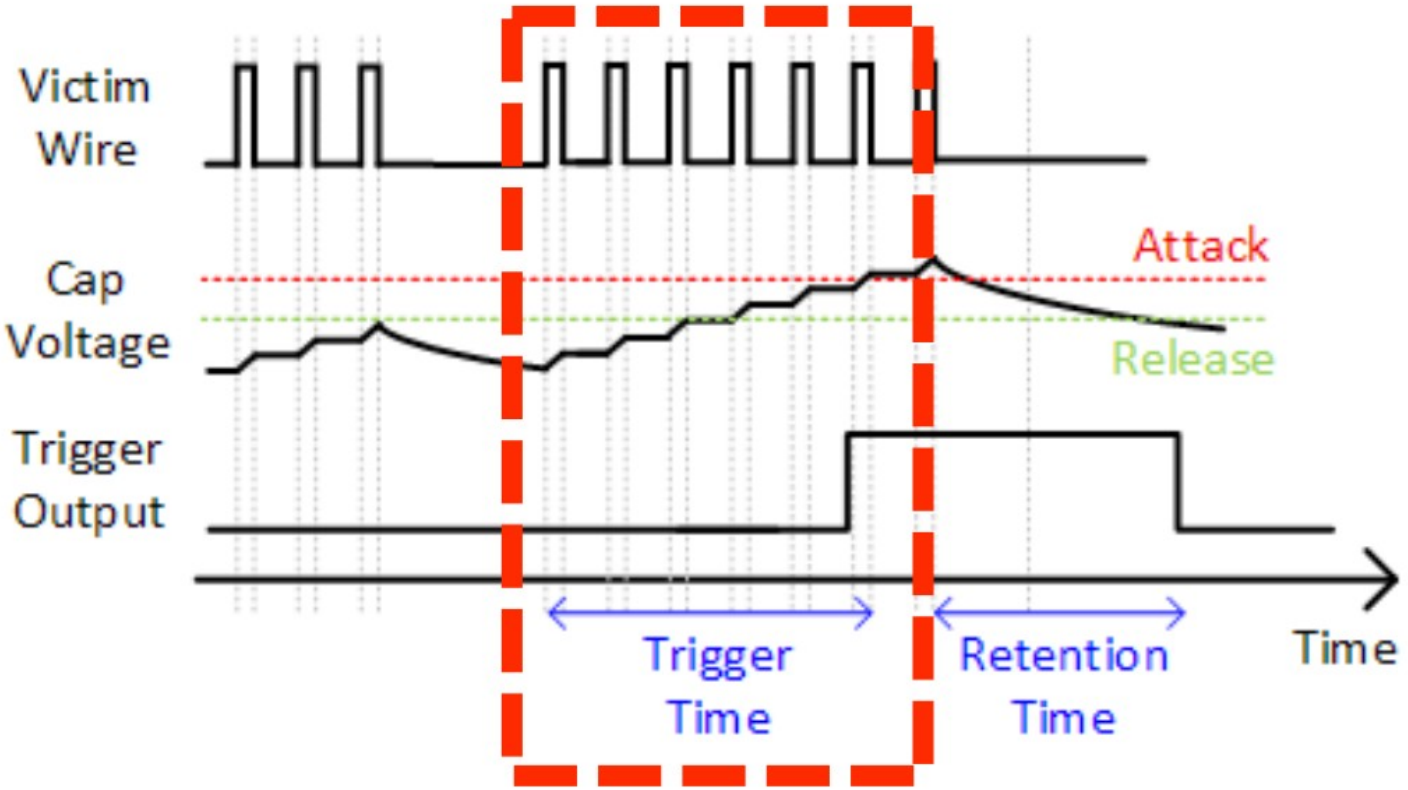

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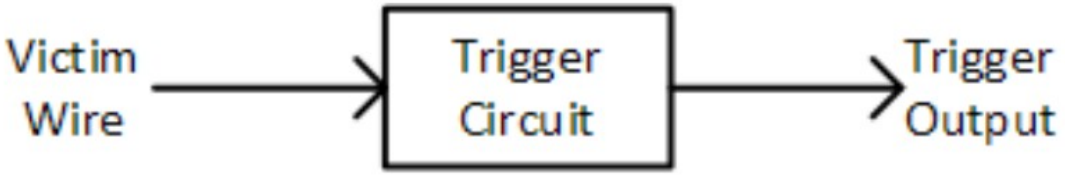

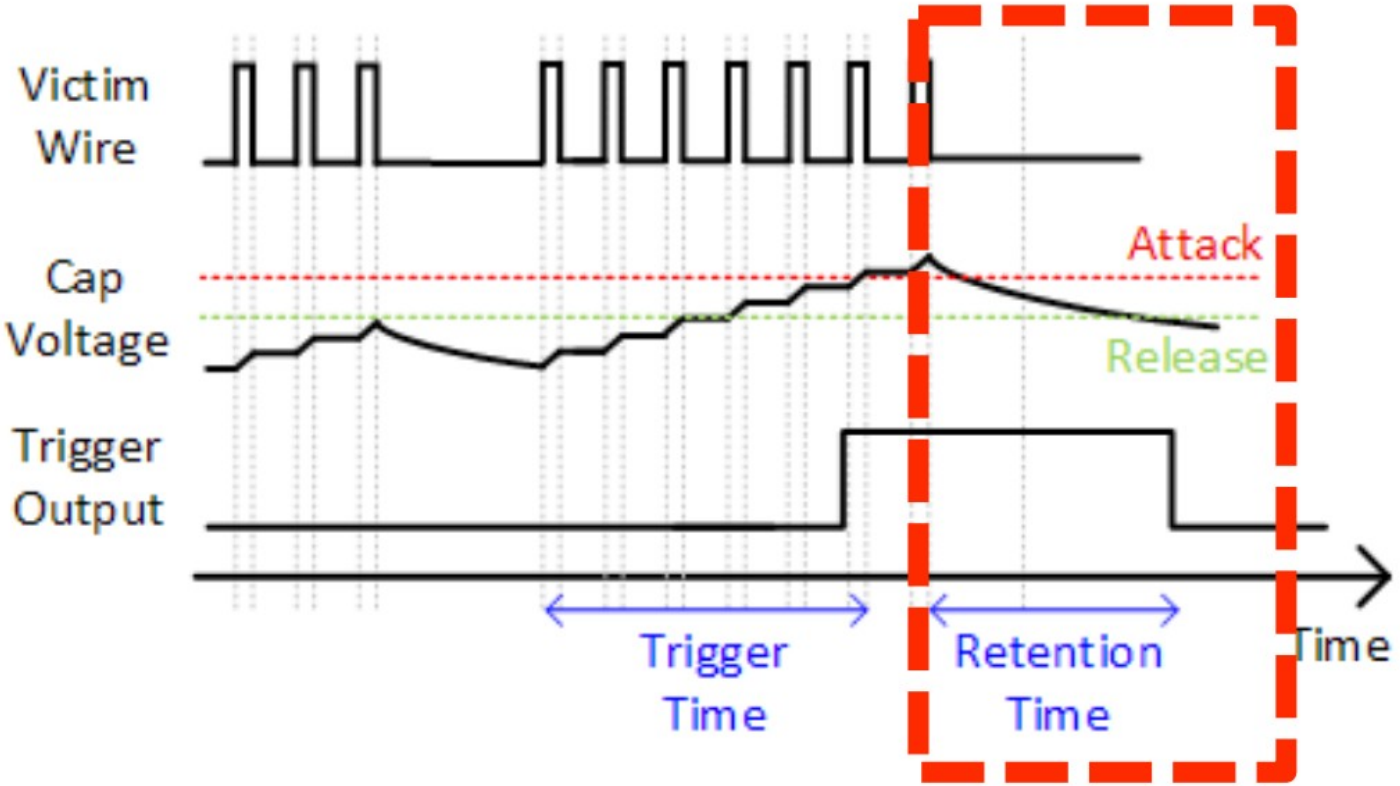

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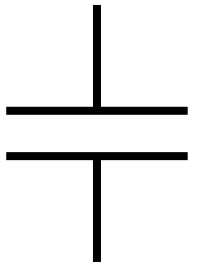

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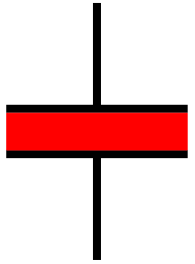

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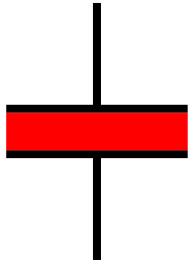

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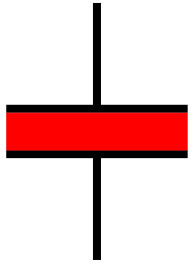
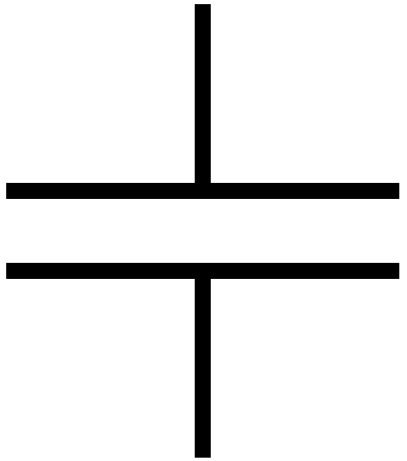
Large capacitors induce current spikes



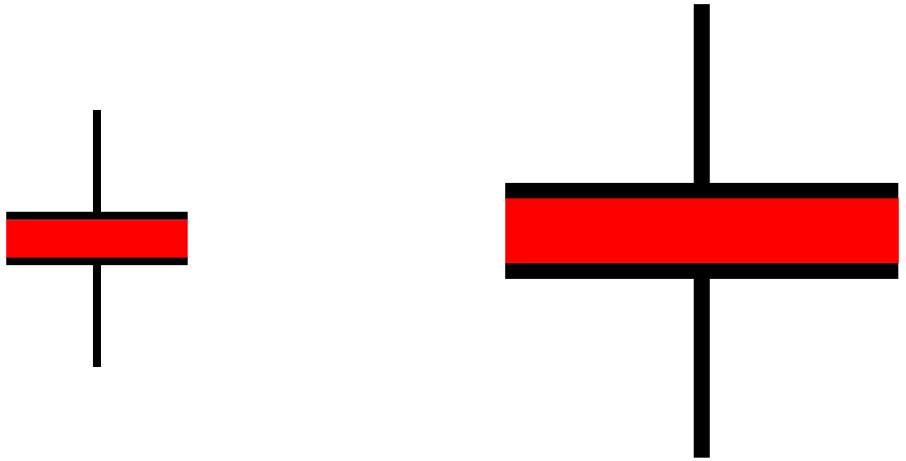


Design Challenge: Single Capacitor

Small capacitors charge up to quickly

- This results in the attack being too easy to trigger

Large capacitors induce current spikes



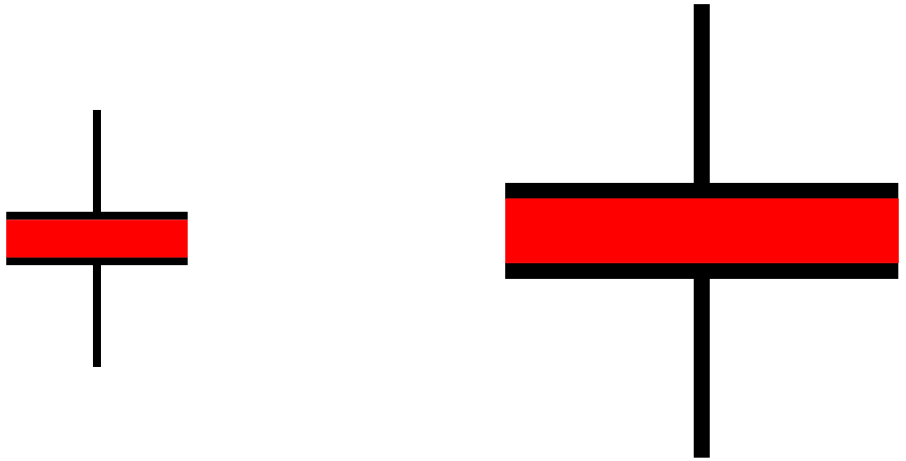
Design Challenge: Single Capacitor

Small capacitors charge up to quickly

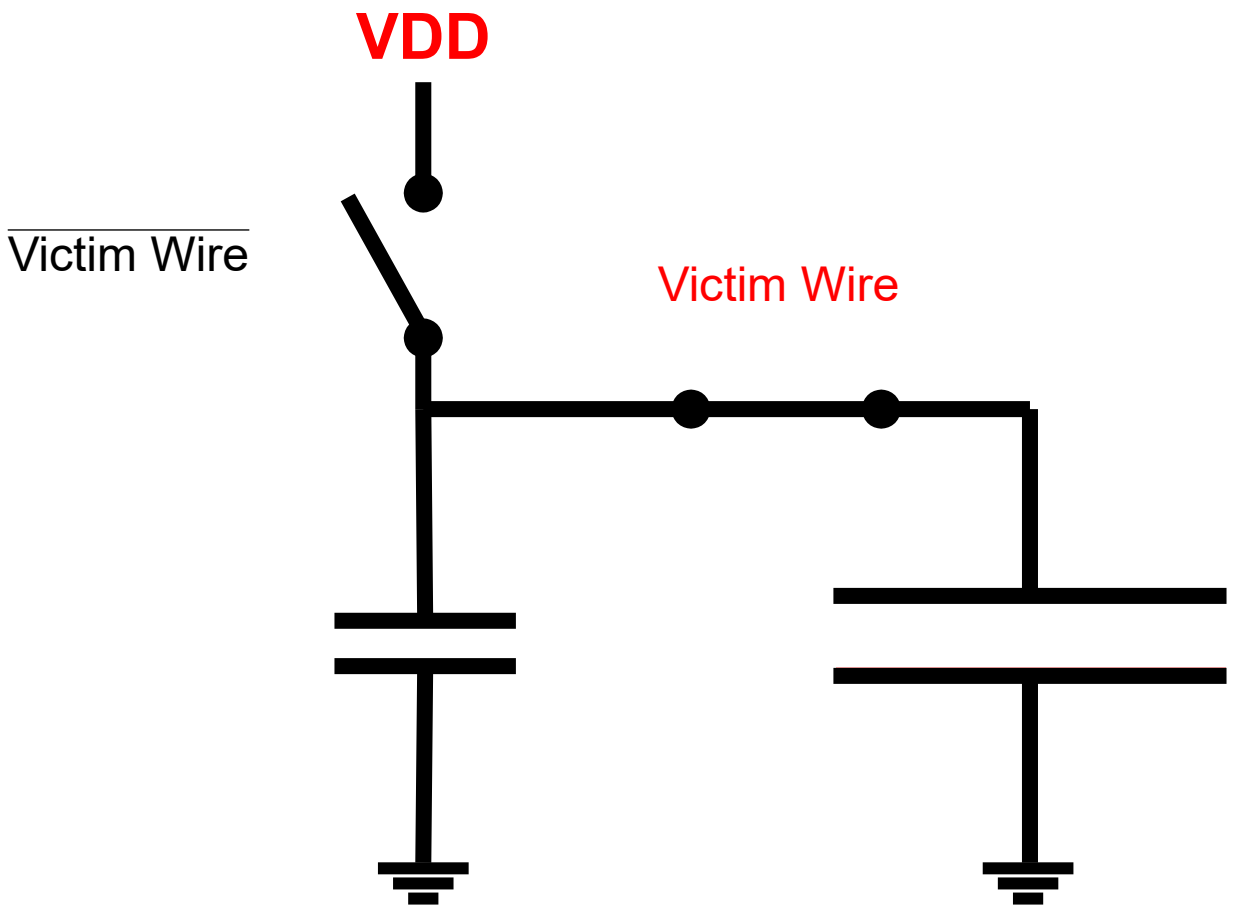
- This results in the attack being too easy to trigger

Large capacitors induce current spikes

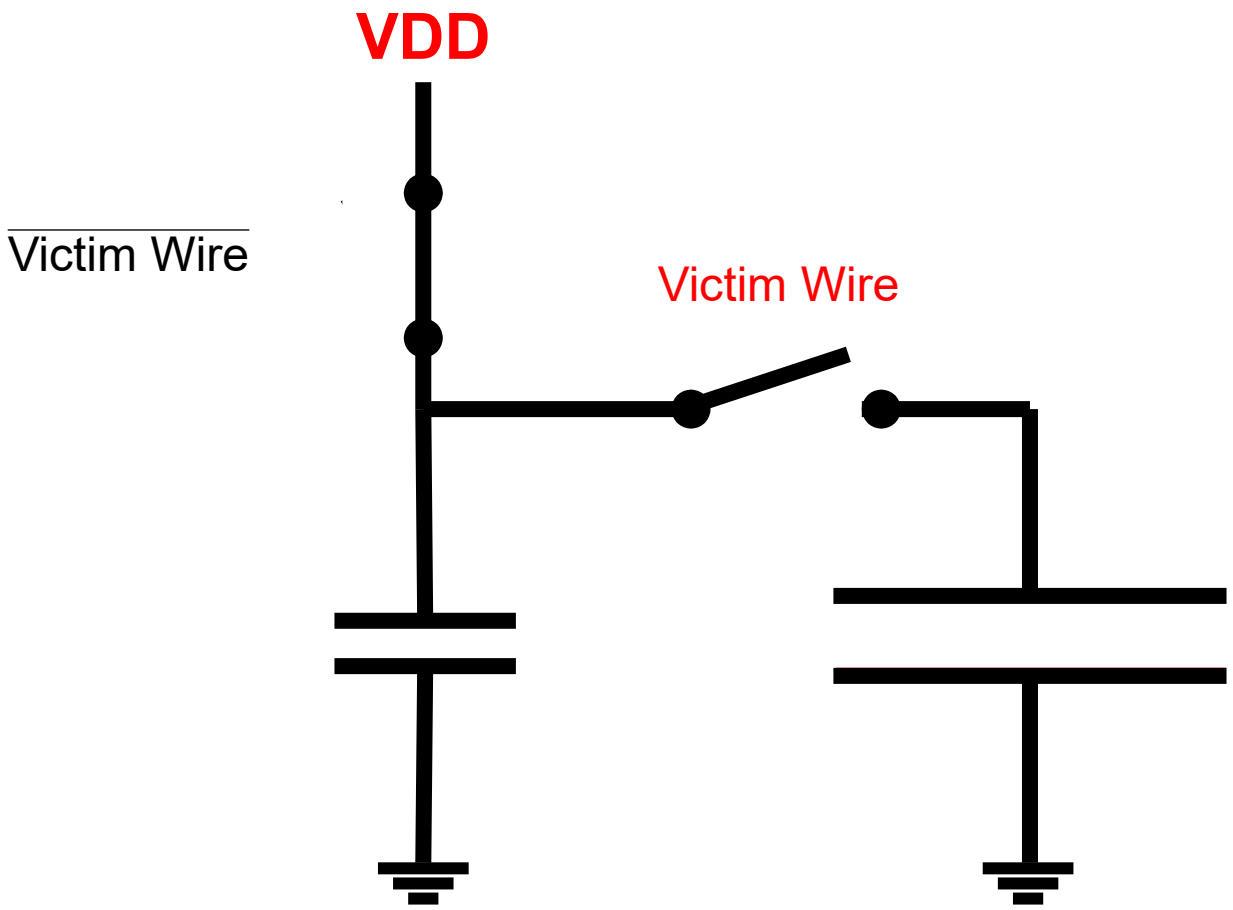
- This makes it also easier to detect



Charge Sharing



Charge Sharing



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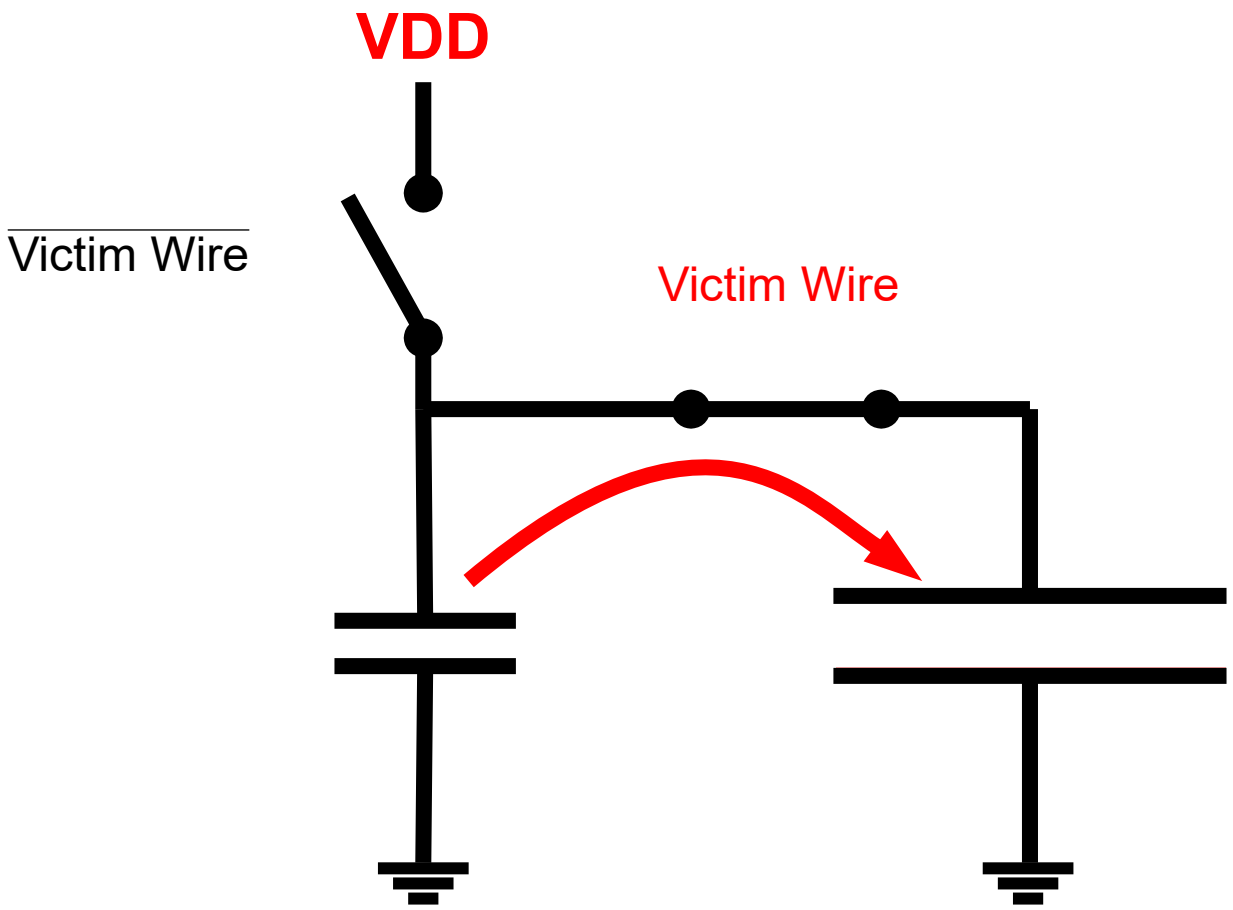

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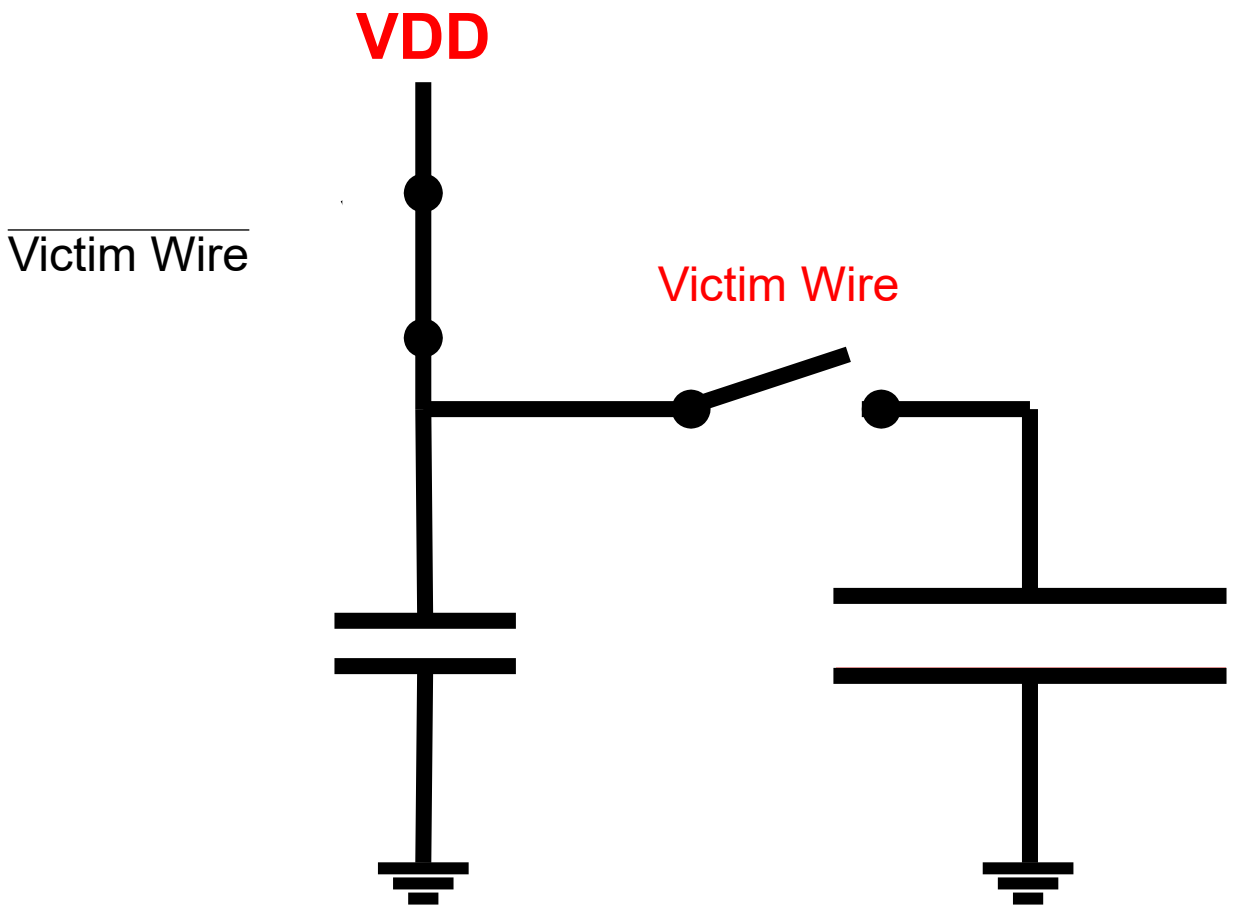

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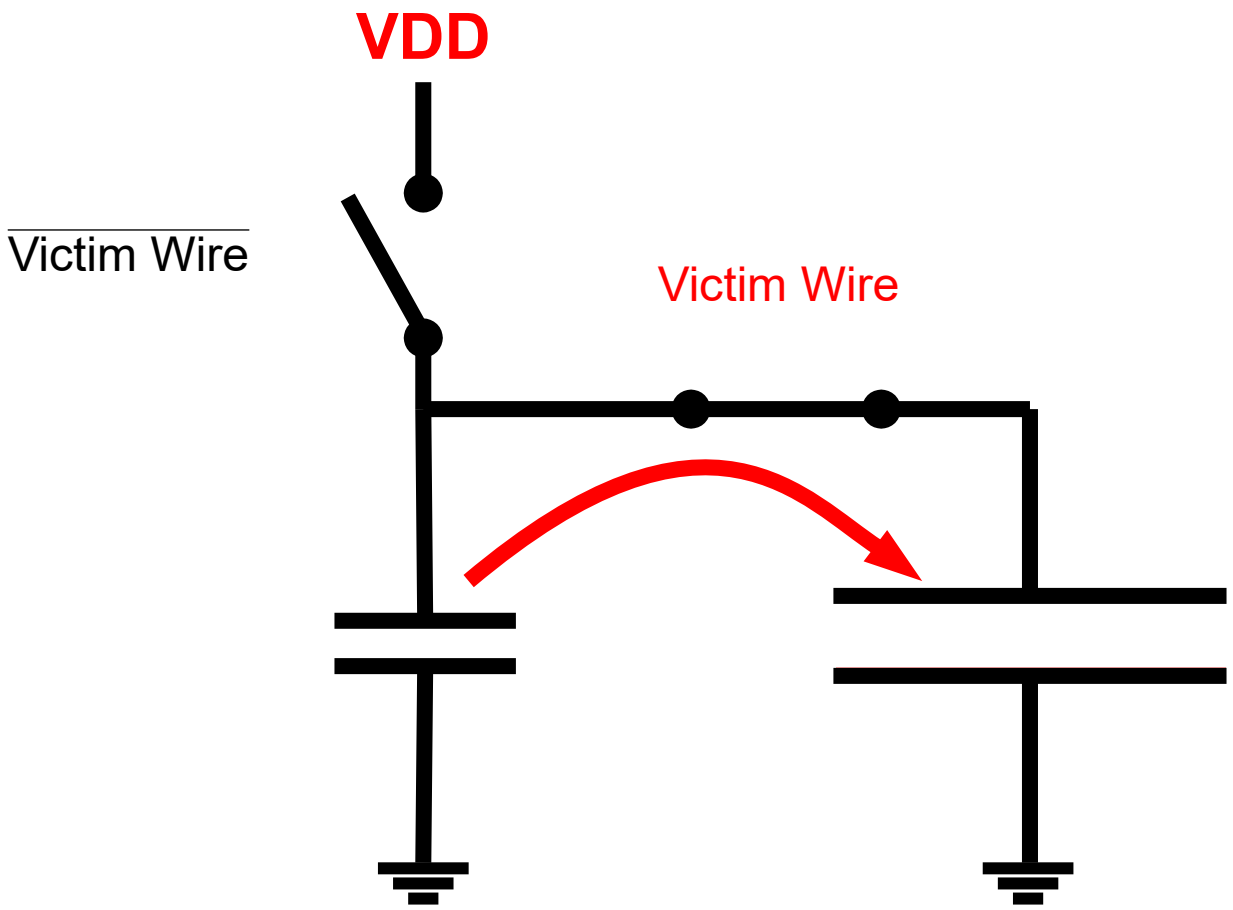
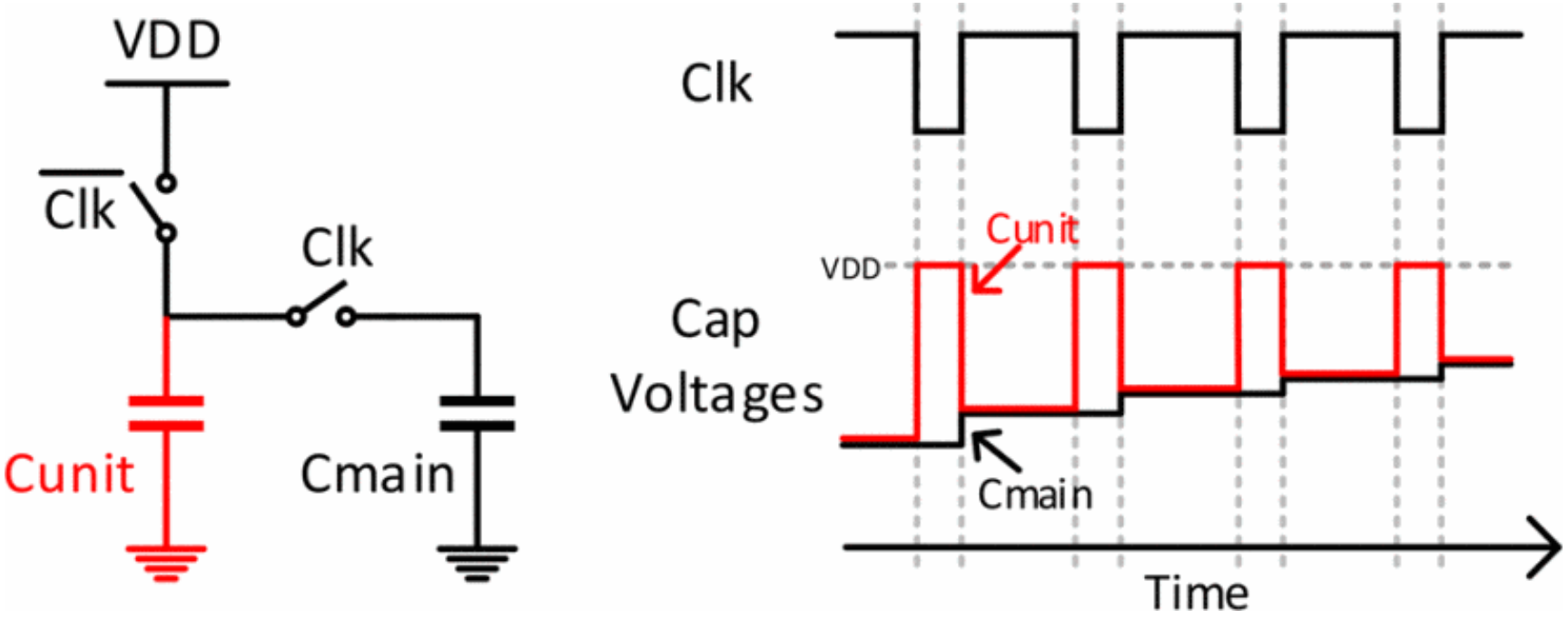


The Analog Trigger Circuit (Revised)



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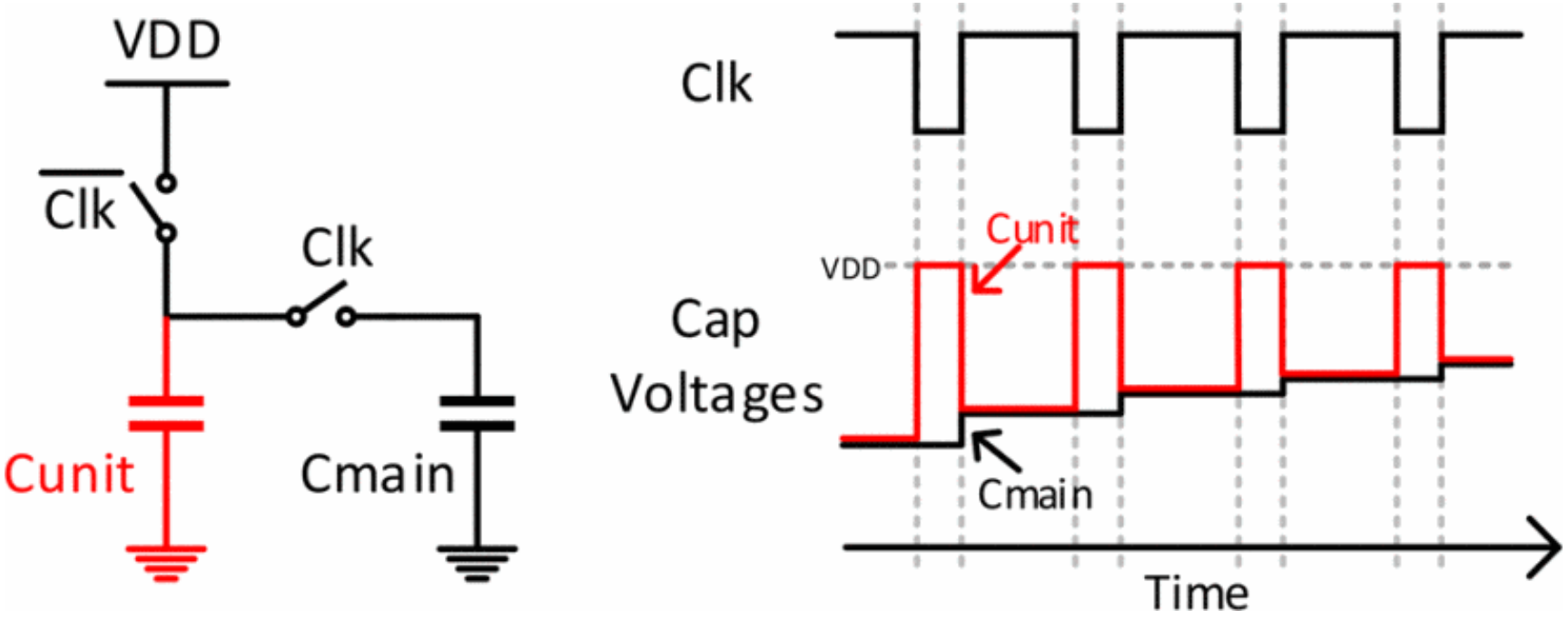
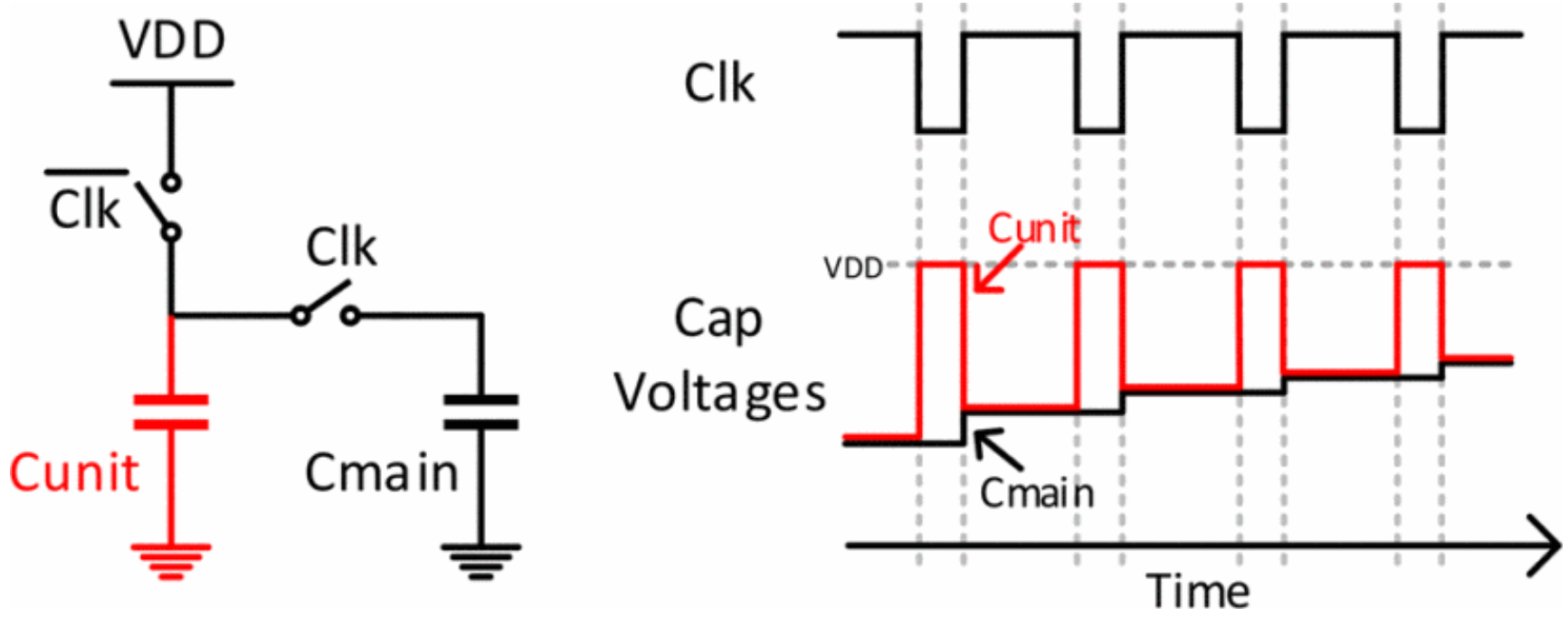


1. What can this trigger be used for?

The Analog Trigger Circuit (Revised)



1. What can this trigger be used for?
2. What do we connect it to?

1. Example Payload Circuit

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Observation:

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Observation:

Many processors de-escalate privilege stepwise after reset

1. Example Payload Circuit

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Many processors de-escalate privilege stepwise after reset

Idea:

1. Example Payload Circuit

Observation:

Many processors de-escalate privilege stepwise after reset

Idea:

Tap into reset wires of supervisor mode register

1. Example Payload Circuit

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Privilege escalation by flipping the supervisor mode bit

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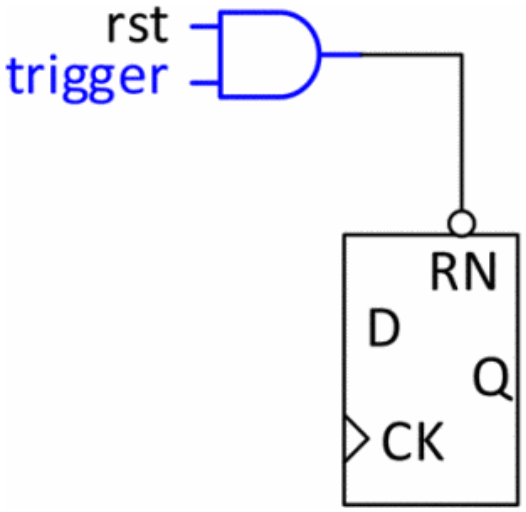
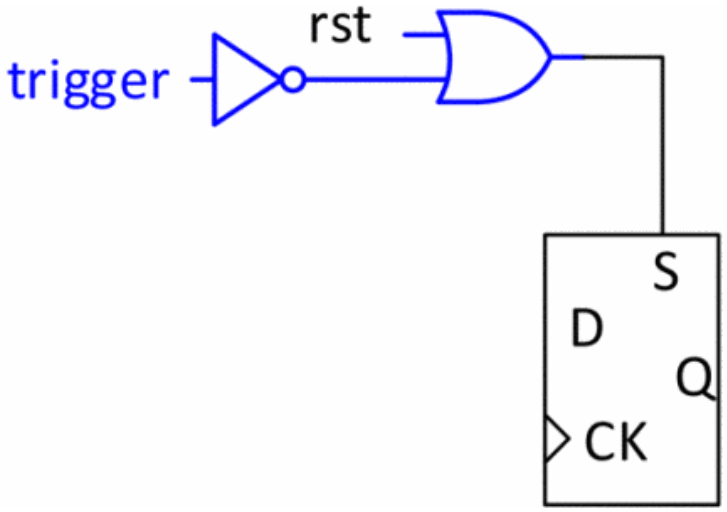
Privilege escalation by flipping the supervisor mode bit



Active-low reset variant



Active-high reset variant

2. How to Find a Victim Wire

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Observation:

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Need to find a software controllable wire with usually very low toggle rate

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Idea:

2. How to Find a Victim Wire

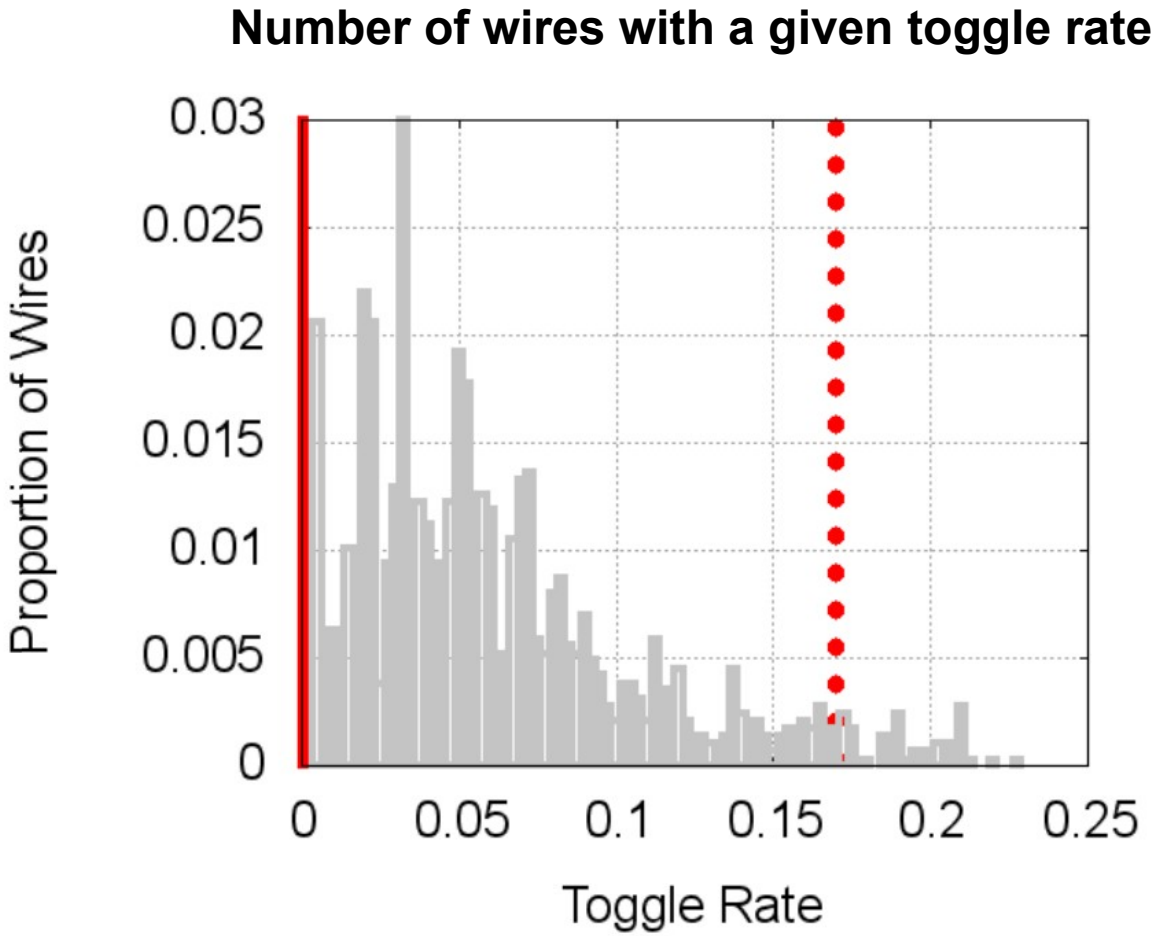
Observation:

Need to find a software controllable wire with usually very low toggle rate

Idea:

Simulate different programs to find wires with low toggle rates

2. How to Find a Victim Wire



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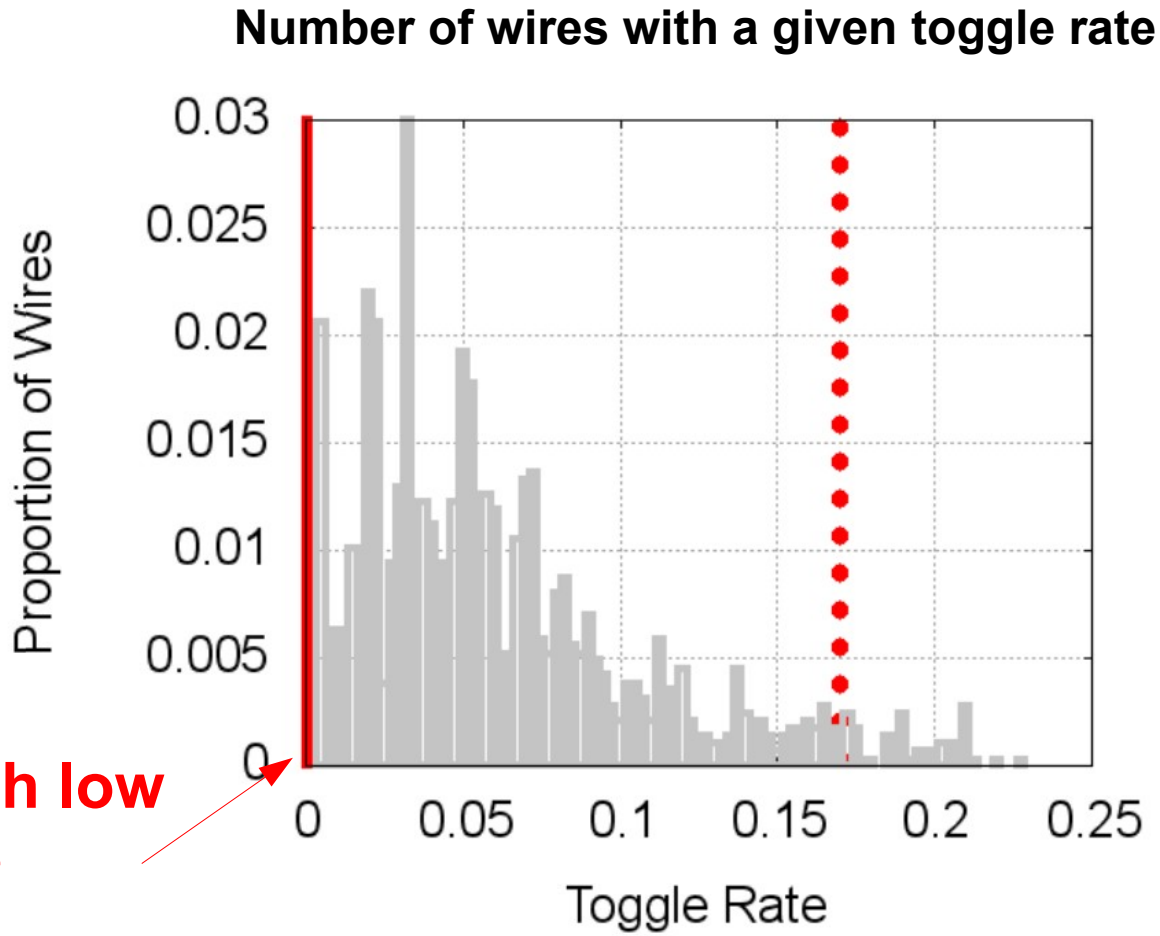
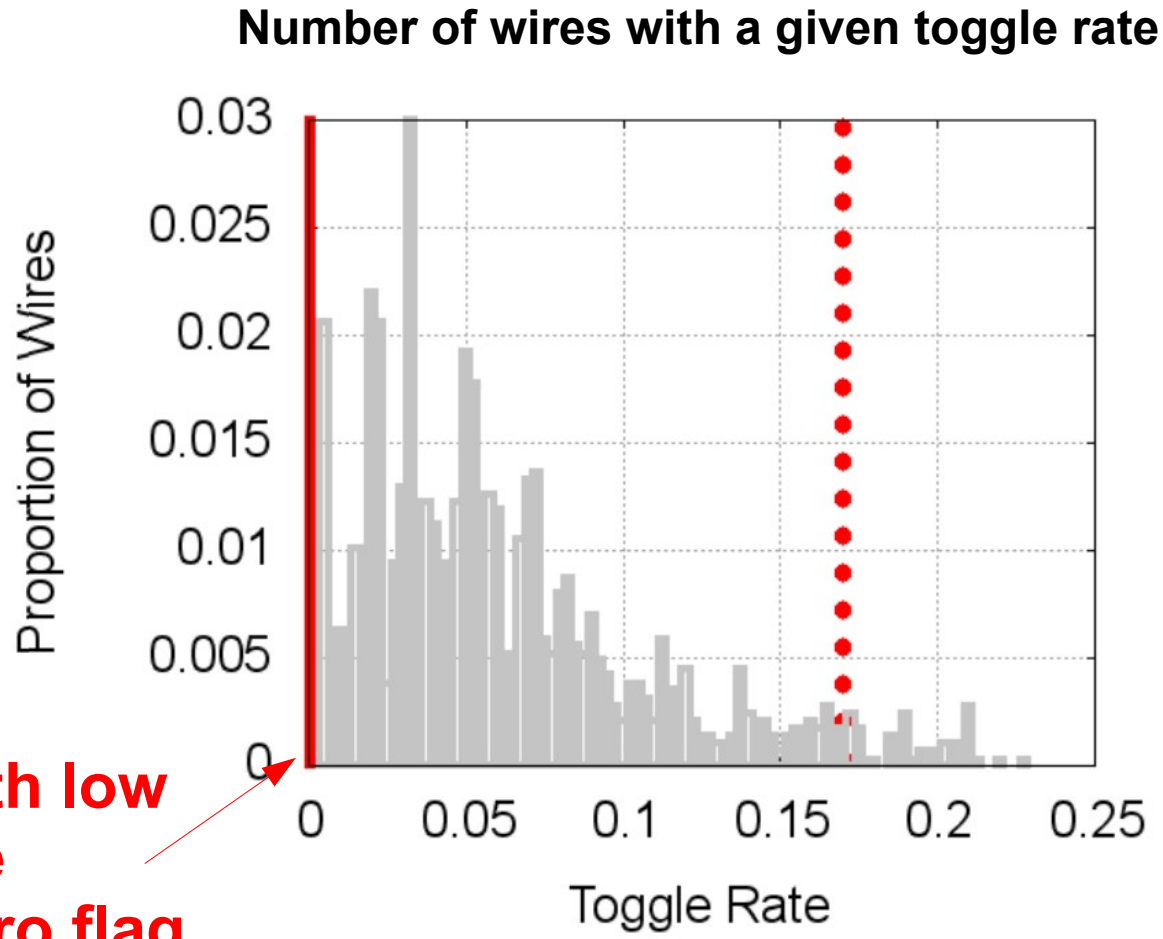


Choose wire with low toggle rate

2. How to Find a Victim Wire



Choose wire with low toggle rate e.g. divide by zero flag

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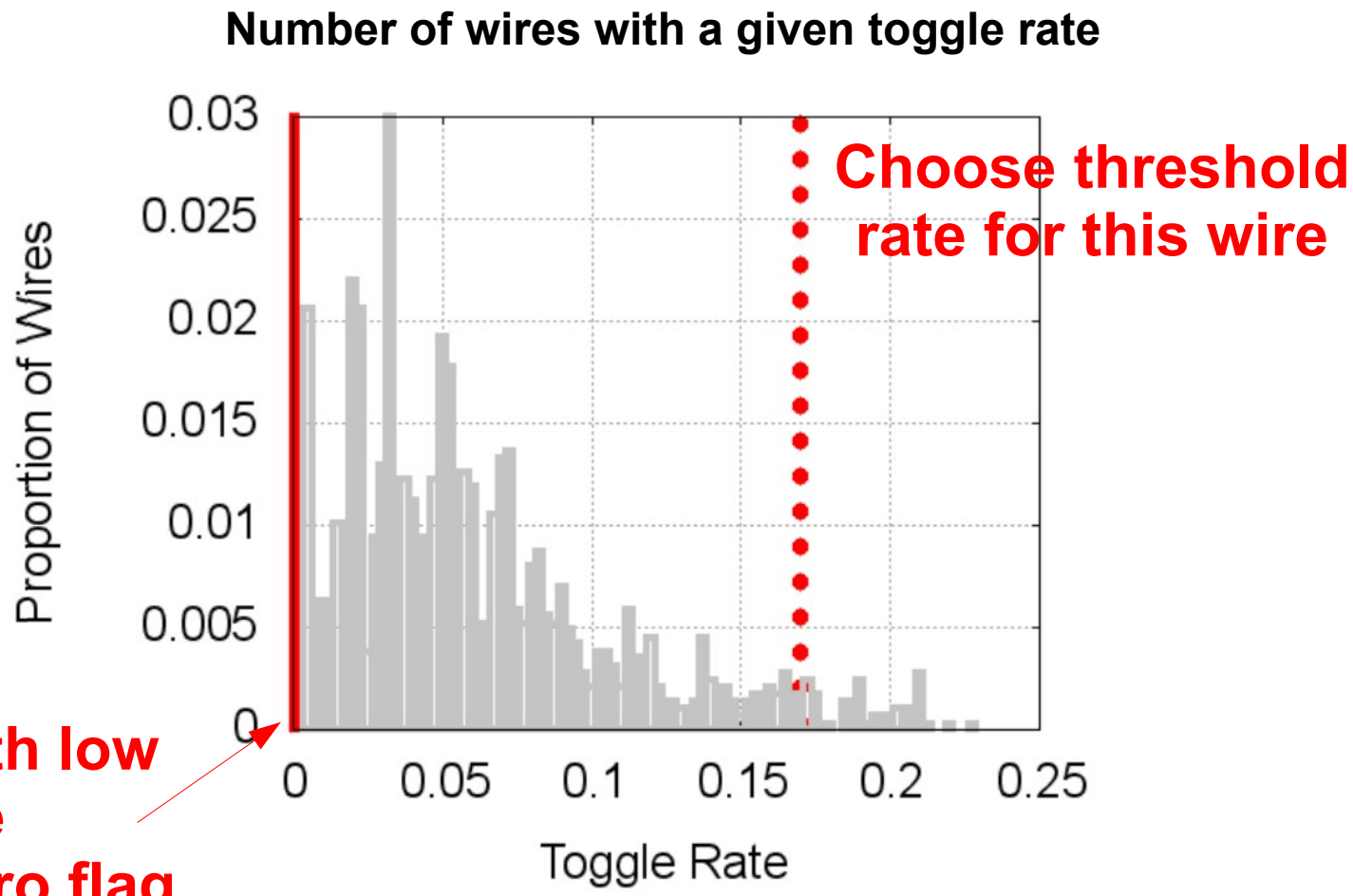

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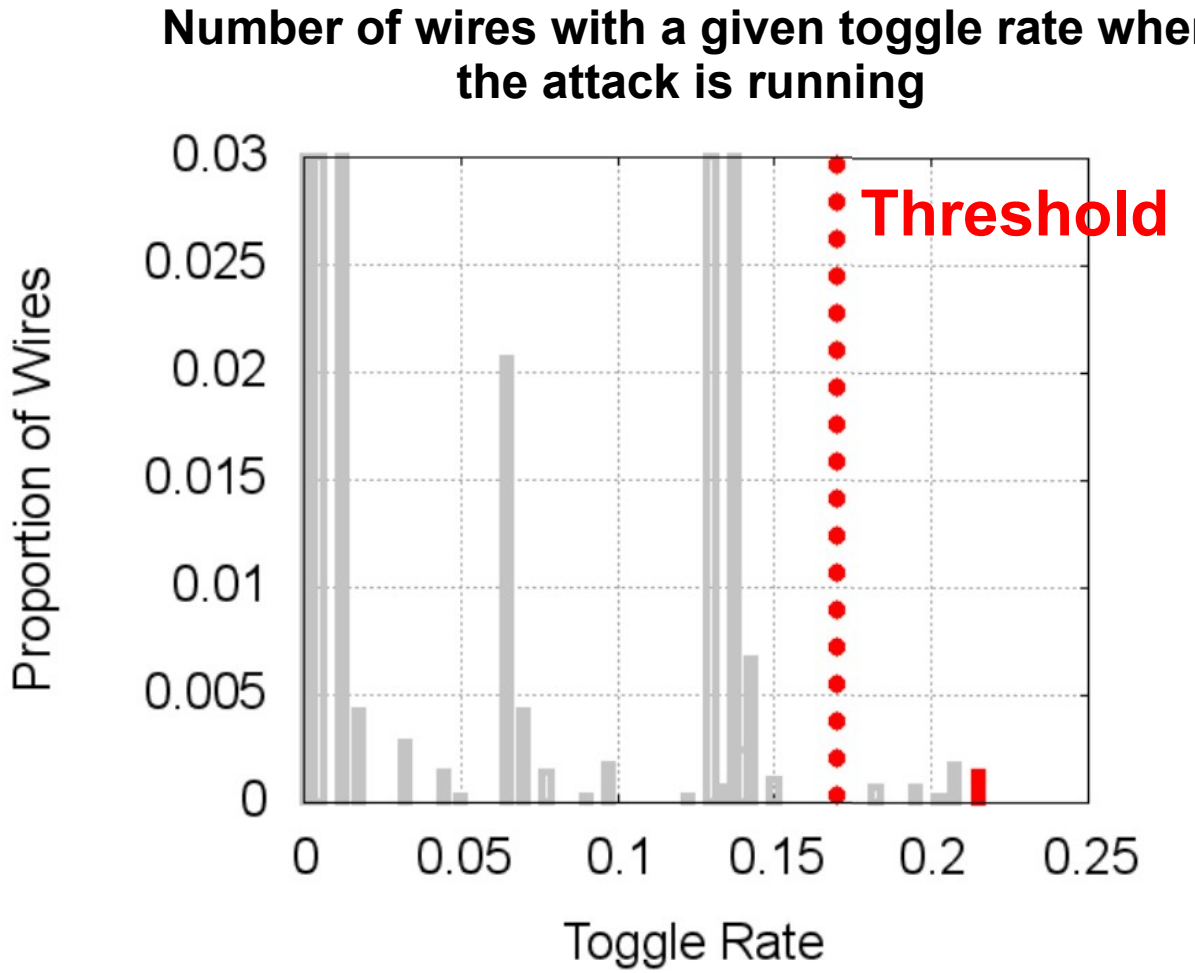

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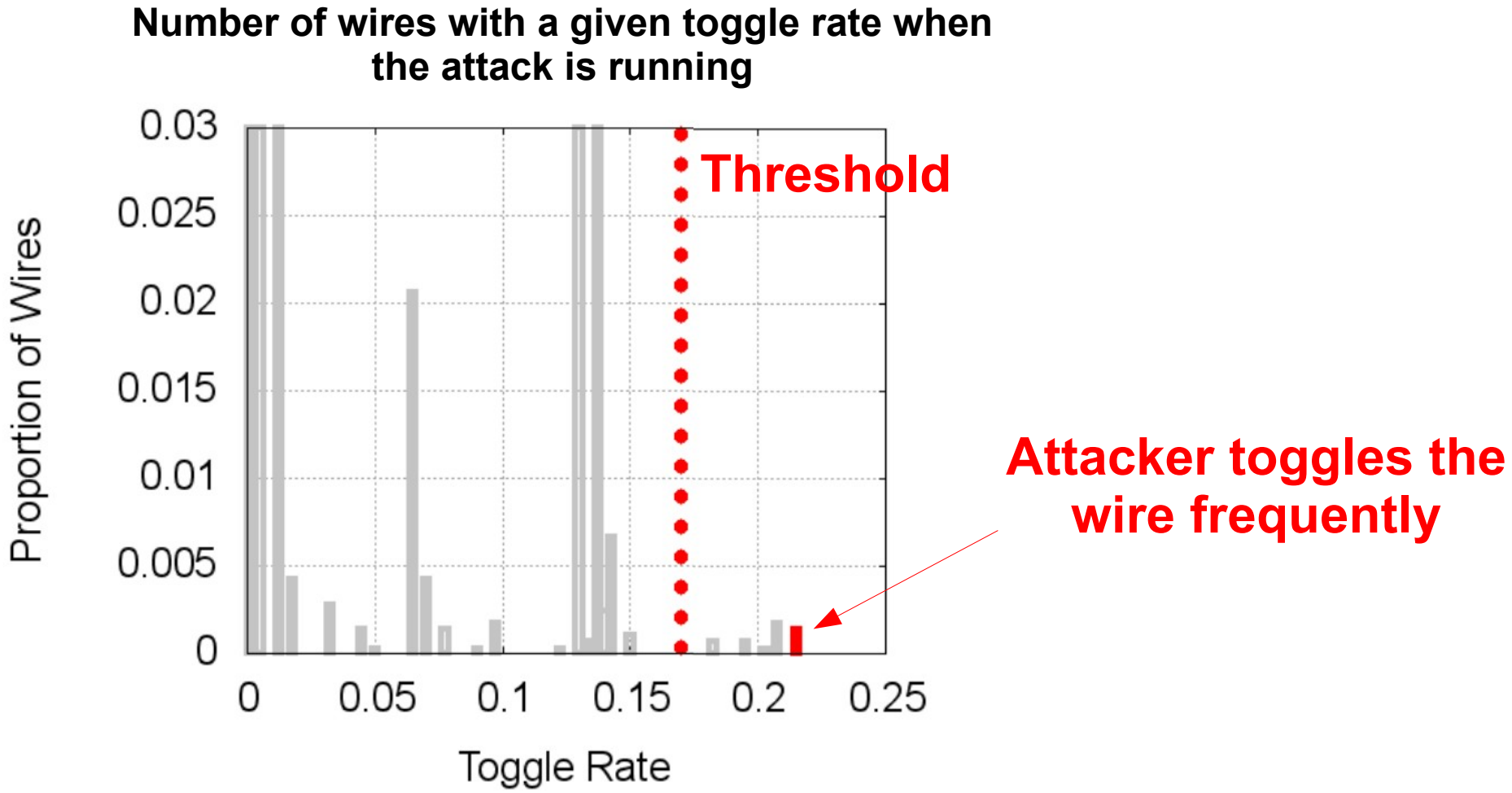

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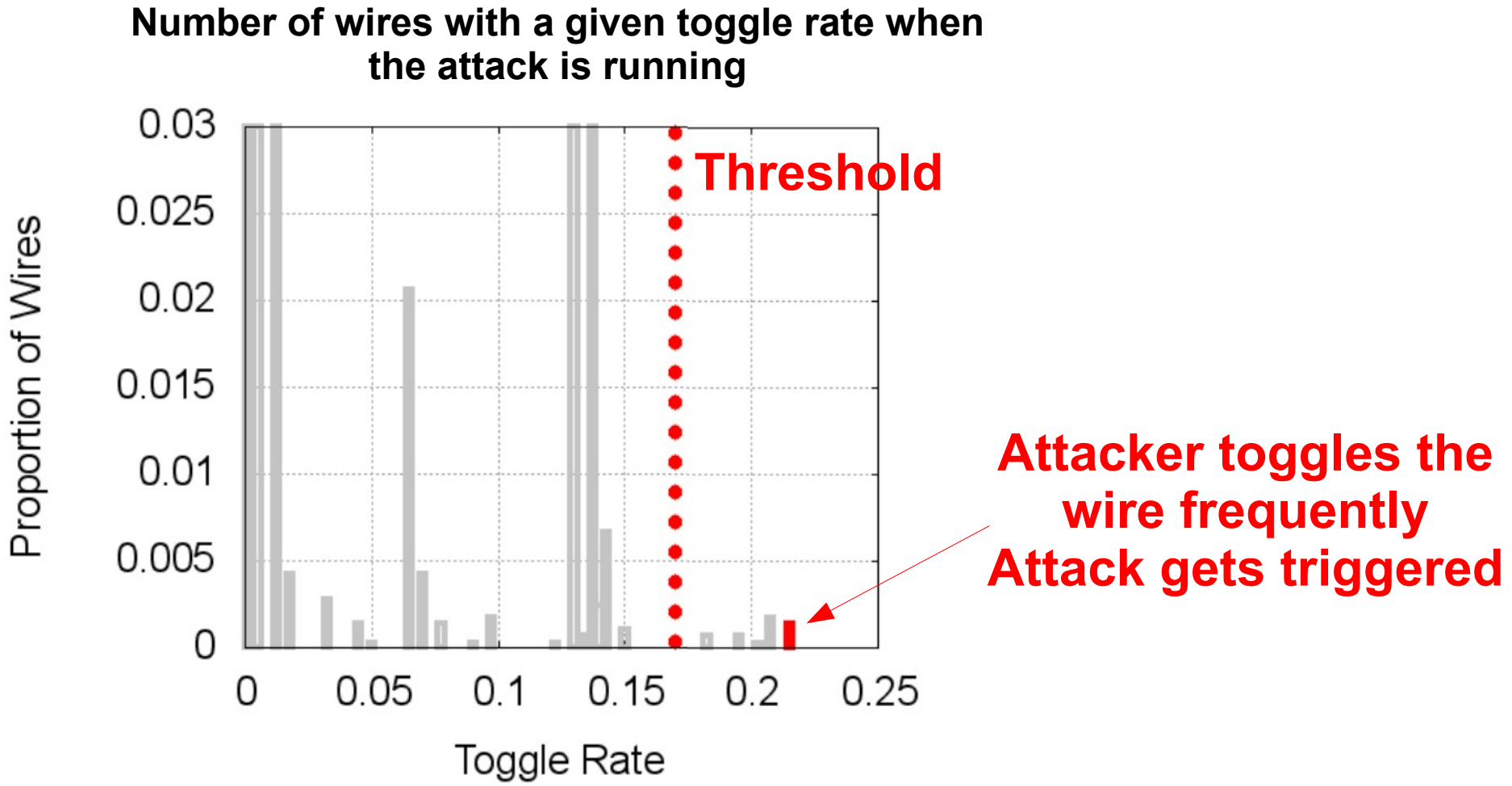
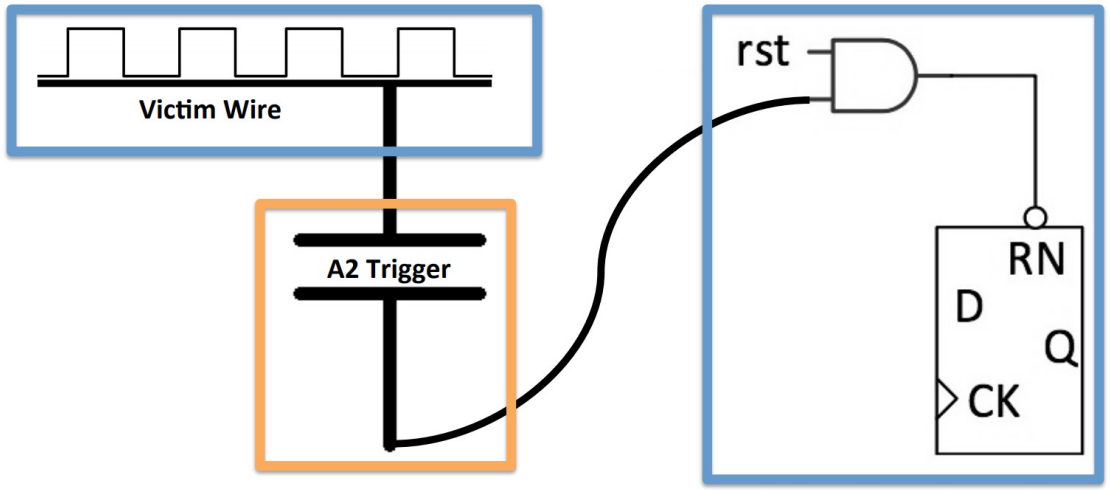


Controlling the Attack From Software

Attack Code Example

```
/* Victim wire is divide by zero
flag */
while attack_success == 0 do
  i ← 0
  while i < 500 do
    z ← 1/0
    i ← i + 1
  end while
  if test_privileges() == 1 then
    attack_success ← 1
  end if
end while
```



Analog domain and digital domain of A2

Key Results

Methodology

Methodology

How the attack was evaluated:

Methodology

How the attack was evaluated:

1. Verification of design in simulation on 65nm CMOS in SPICE

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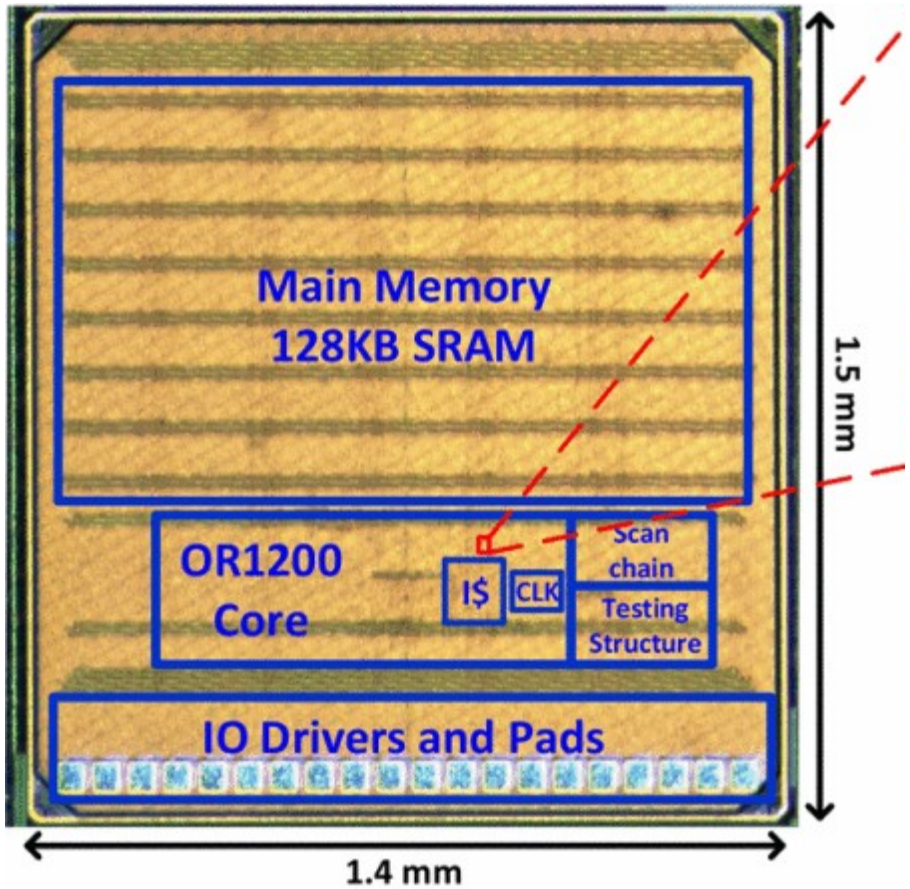
4. Assessing detectability

Implementation in a Real Chip

OpenRISC 1200 Processor



Implementation in a Real Chip

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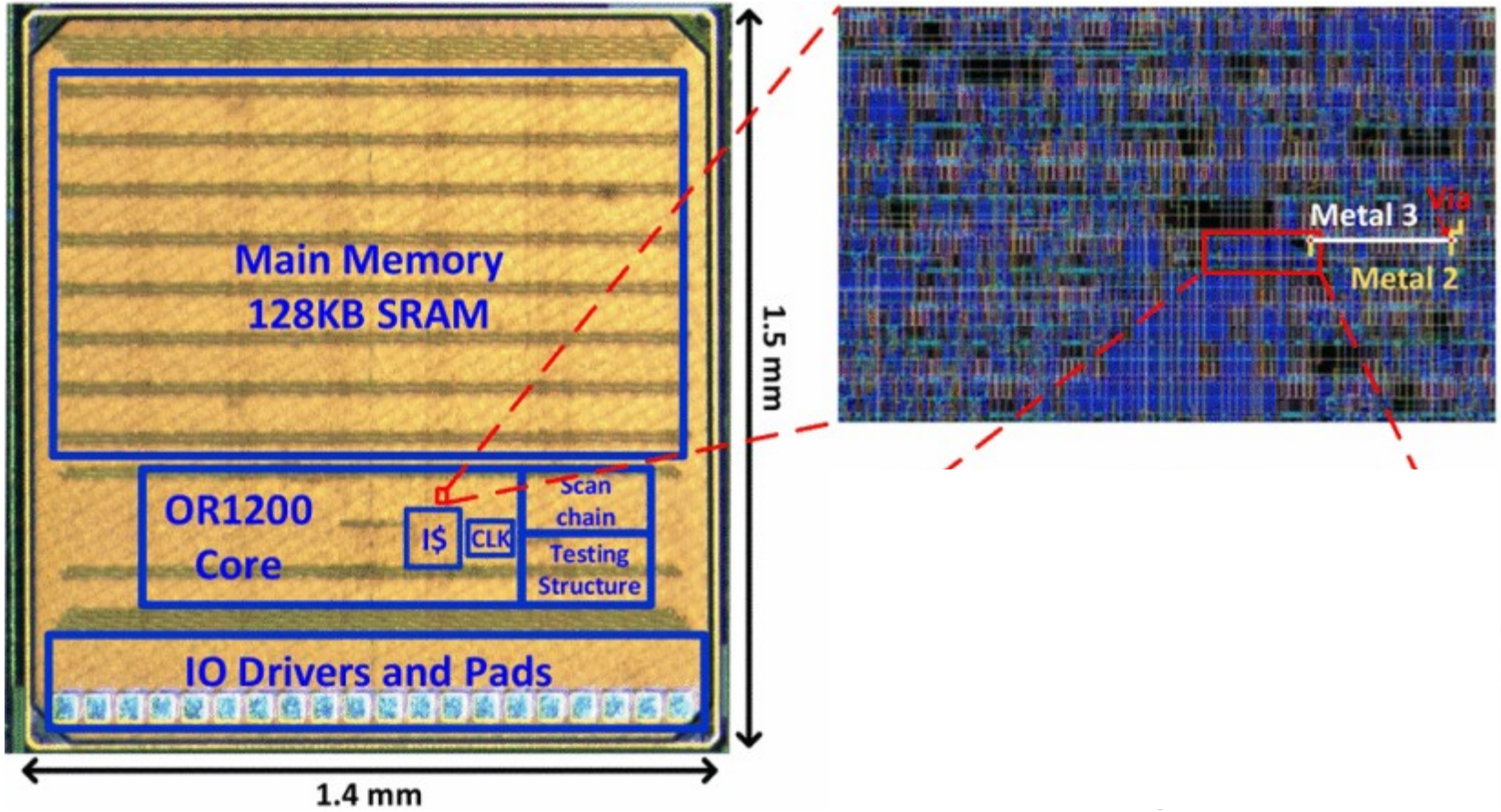

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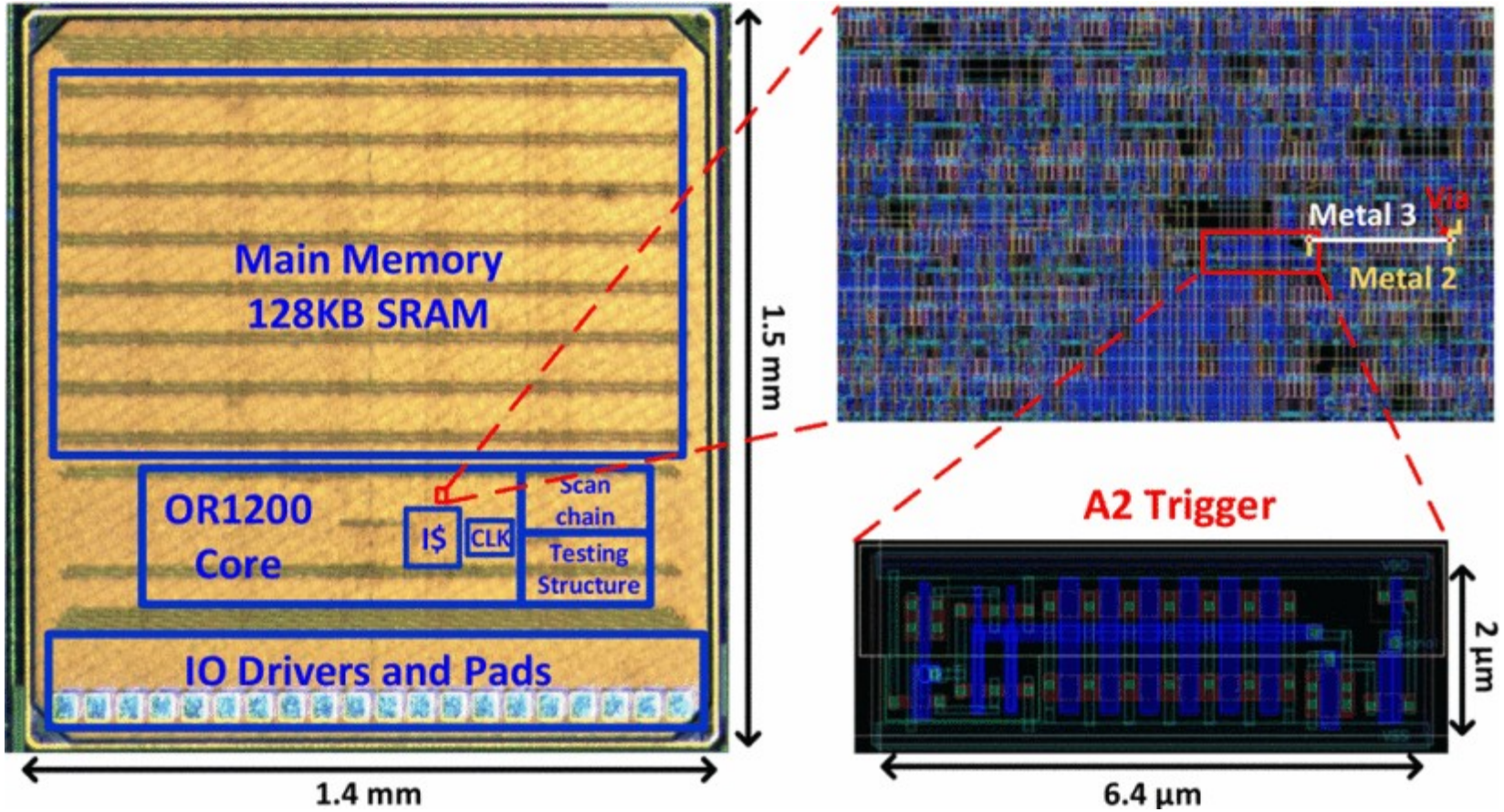
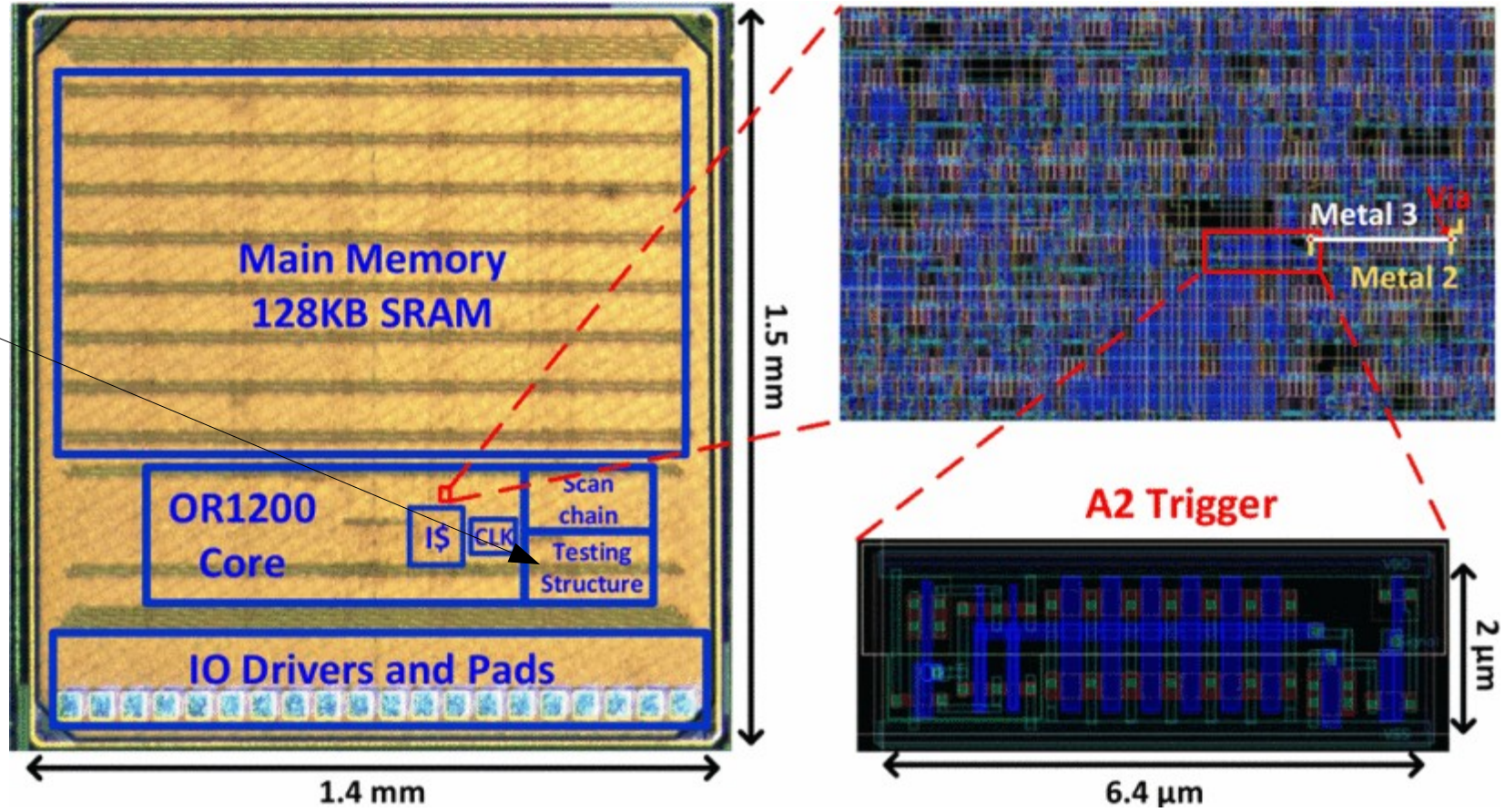


Implementation in a Real Chip

OpenRISC 1200 Processor

Includes stand-alone trigger testing structure



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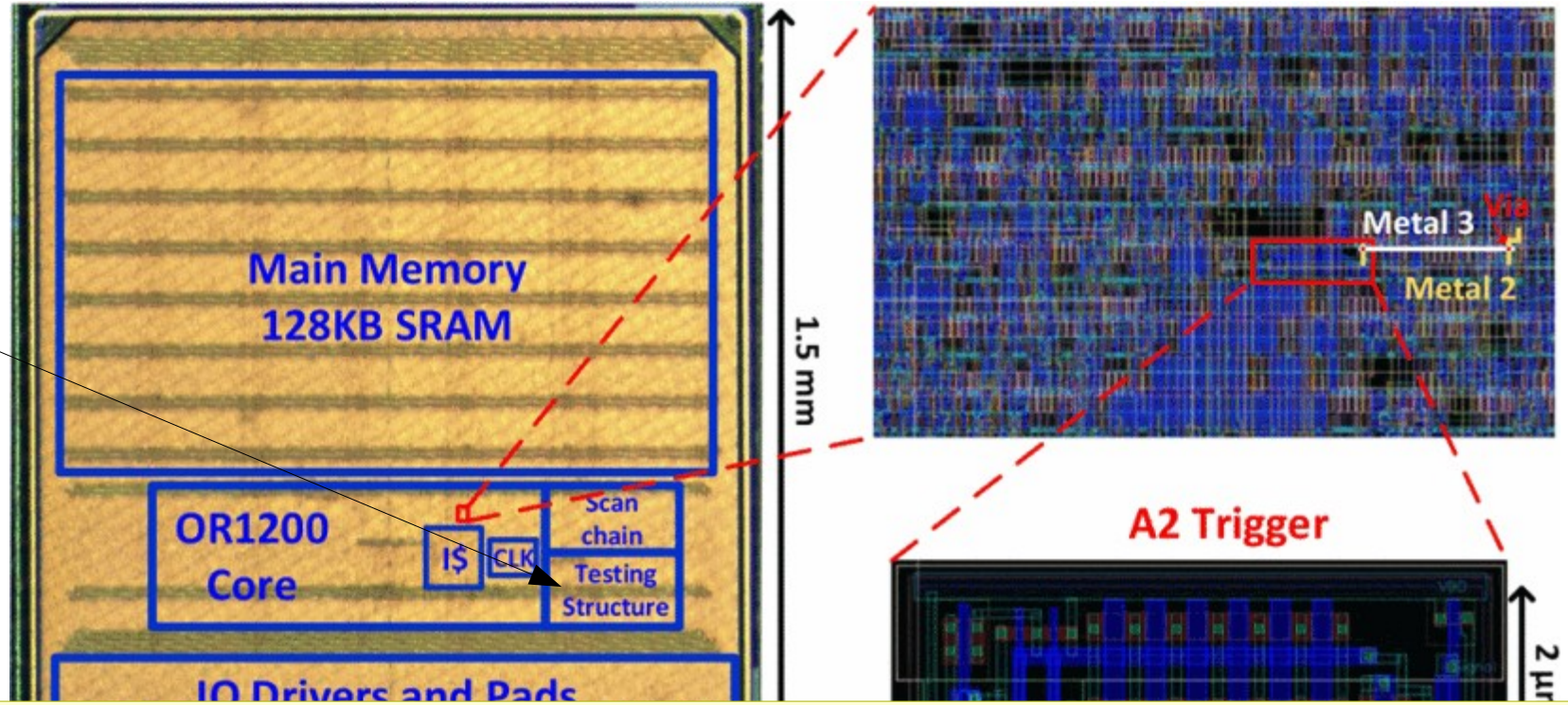

Uses only 0.08% of the total area!

Goal of the Paper

Goal: Design a hardware attack that is

Very small

Controllable

Stealthy

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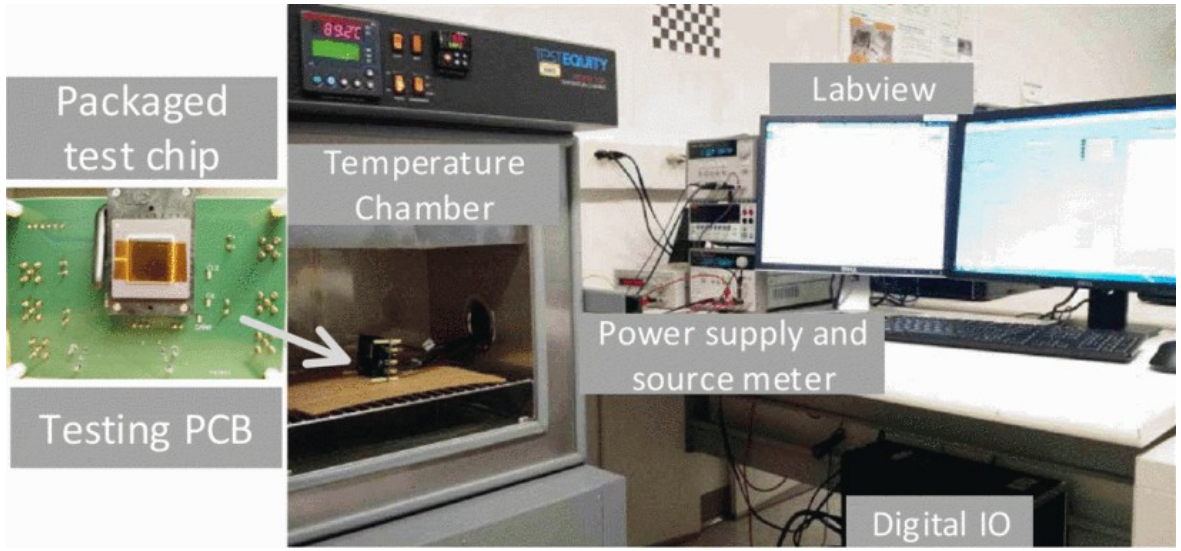
Verification in the OR1200 Processor

Key Results

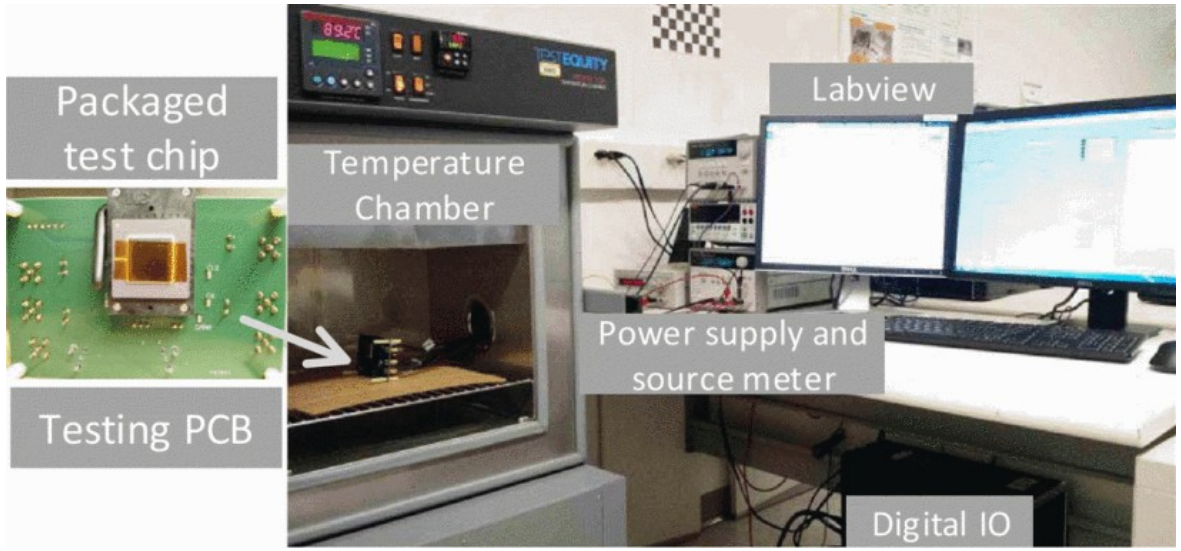


Testing setup

Verification in the OR1200 Processor

Key Results

Circuits tested under temperature, clock frequency and voltage variations



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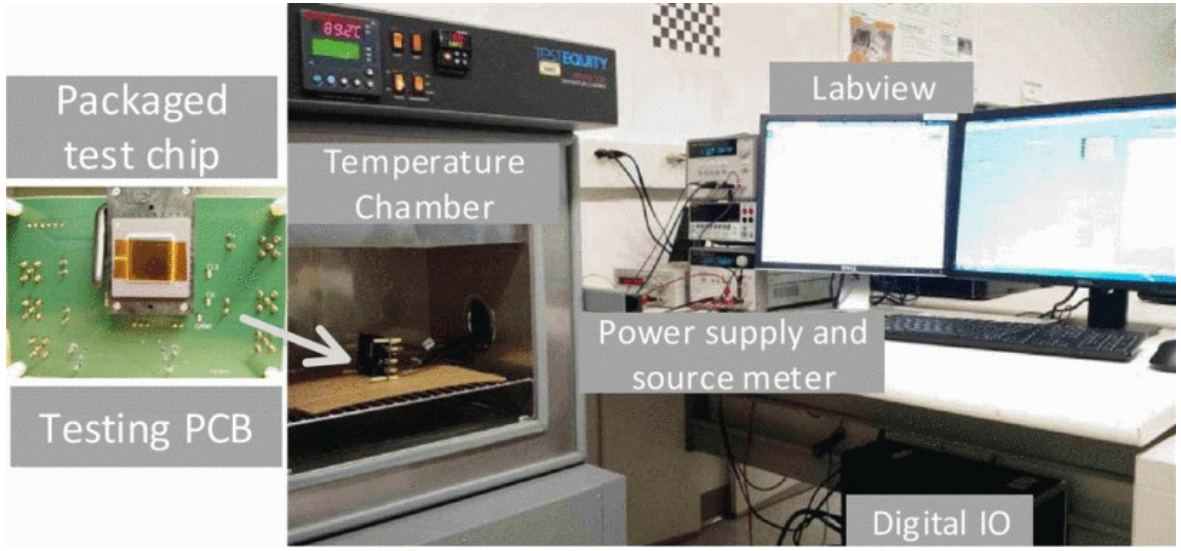

Testing setup

Verification in the OR1200 Processor

Key Results

Circuits tested under temperature, clock frequency and voltage variations

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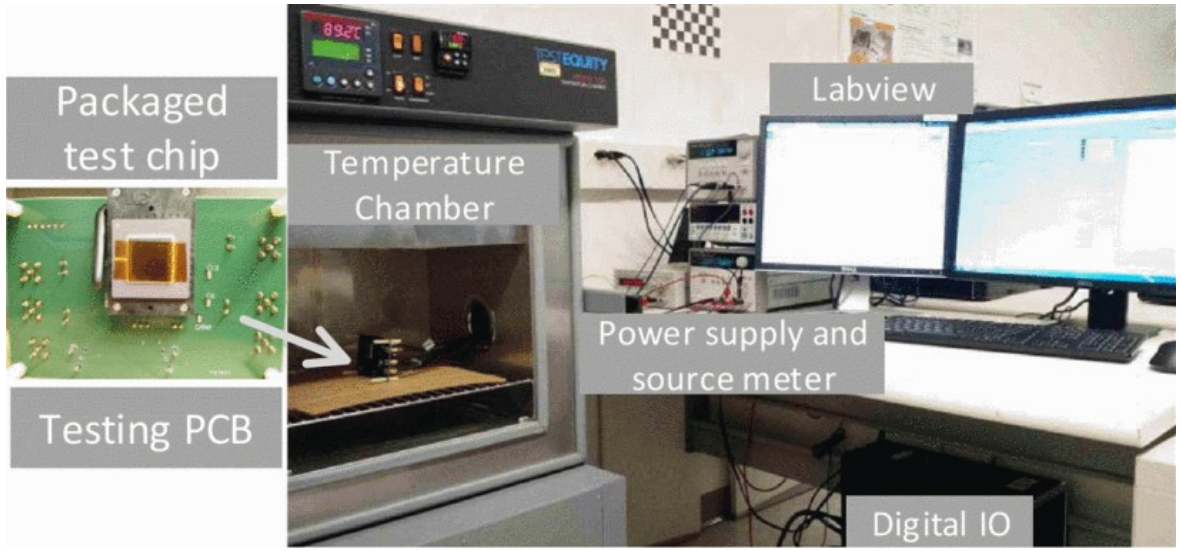
Trigger and retention times measured using the separate testing structure



Testing setup

Test Results of Real Chip Implementation

Key Results

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Attacks in the chips are:

Test Results of Real Chip Implementation

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Robust against manufacturing variations

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Robust against supply voltage fluctuations

Test Results of Real Chip Implementation

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Robust against supply voltage fluctuations

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Comparison to Simulation

Trigger times in cycles

Trigger Circuit	Toggle Rate (MHz)	Measured (10 chip avg)	Simulated (Typical corner)
w/o IO device	120.00	7.4	7
w/o IO device	34.29	8.4	8
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Comparison shows that simulation has good enough accuracy to fabricate precise and controllable attacks!

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How to Detect a Hardware Attack

Key Results

How to Detect a Hardware Attack

Side Channel Information

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Power requirements

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Detects attacks that get hot or use much power

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Measure signal propagation delays

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Detects attacks that add logic to wires

Functional Testing

Test for unexpected behaviour

Detects some attacks that change the circuit behaviour

How Stealthy is the Attack?

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Can the attack be detected by side channels?

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Measuring of chip power consumption

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Simulating theoretical power usage of trigger circuit

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Answer:

How Stealthy is the Attack?

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Simulating theoretical power usage of trigger circuit

Answer:

The power requirements of the attack are well below normal fluctuations

Detection Mechanisms Evaded by A2

Side Channel Information

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Measure signal propagation delays

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Maybe With On-Chip Sensors?

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Can the attack be detected by measuring propagation delays?

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Can the attack be detected by measuring propagation delays?

High accuracy simulation of trigger wire delays

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Reset wires are typically asynchronous

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Answer:

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Answer:

For a **4ns** clock period the delay change is **only 0.33%** and well below process variation and noise

Detection Mechanisms Evaded by A2

Side Channel Information ✓

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Test for unexpected behaviour

And Visual Inspection?

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Can the attack be found by looking at the chip?

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And Visual Inspection?

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A2 is as small as **one gate** and is almost identical to the other gates in a design

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Requires delayering to very low layers

Answer:

A2 is unlikely to be found by visual inspection

Detection Mechanisms Evaded by A2

Key Results

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Adding Sensors ✓

Measure signal propagation delays

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Test for unexpected behaviour

What About Functional Testing?

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Is the attack triggered during normal execution?

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Testing with five selected benchmark programs

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Testing over 6 different temperatures from -25°C to 100°C

Answer:

The attack was not activated across all programs and temperatures

Detection Mechanisms Evaded by A2

Side Channel Information ✓

Temperature

Power requirements

Electromagnetic measurements

Adding Sensors ✓

Measure signal propagation delays

Visual Inspection ✓

Delayering the chip

Inspection via scanning electron microscope

Functional Testing

Test for unexpected behaviour

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A2 is not easily detectable!

Goal of the Paper

Goal: Design a hardware attack that is

Very small 

Controllable 

Stealthy

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Needs a new type of defense!

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-When the capacitors are fully charged, deploy an attack that forces a victim flip-flop to the desired value.

Key Results: 1) Implemented this attack in an OR1200 processor and fabricated a chip; 2) Experimental results show that the attack works efficiently; 3) The attack eludes activation by a diverse set of benchmarks; 4) the attack evades known defenses

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+ Gives a history on previous work done in the field

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- Contains a few typos

Thoughts & Ideas

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  - i.e. avoiding complicated state machines where precision is not as important
  - As was mentioned last week, maybe to prevent Rowhammer attacks?

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  - I have not found any evidence that this attack is being used yet (please prove me wrong)
  - I have found cases for other hardware trojans though, e.g. [1]
  - Can you think of other cases of hardware attacks being used?

[1] S. Skorobogatov, C. Woods, "**Breakthrough silicon scanning discovers backdoor in military chip**", Proc. 14th Int. Conf. Cryptograph. Hardw. Embedded Syst., pp. 23-40, 2012.

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- **What has to be considered when applying this attack to other (smaller) technology nodes?**

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Some Interesting Follow-Up Papers

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- Mohammad-Mahdi Bidmeshki, Angelos Antonopoulos, Yiorgos Makris, "**Information flow tracking in analog/mixed-signal designs through proof-carrying hardware IP**", Design Automation & Test in Europe Conference & Exhibition (DATE) 2017, pp. 1703-1708, 2017.

Open Discussion

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Moodle Discussion

https://moodle-app2.let.ethz.ch/mod/forum/discuss.php?d=38995

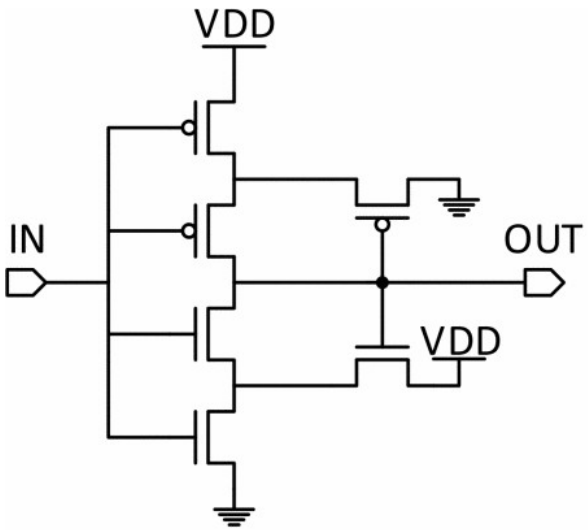
Thank You For Your Attention!

Backup Slides

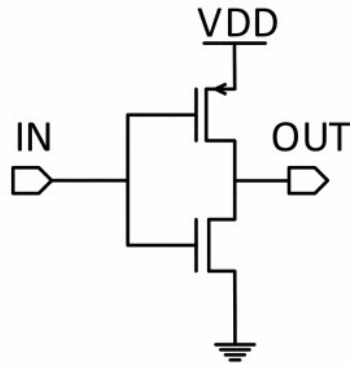
Threshold Detector

Threshold Detector

Two possibilities for threshold detectors



Schmitt Trigger

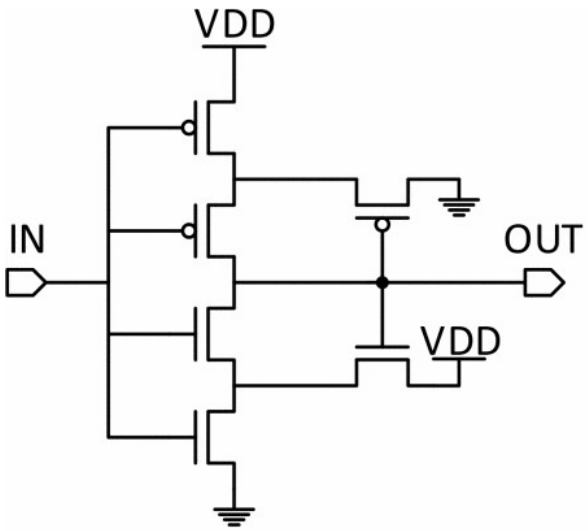


Skewed Inverter

Threshold Detector

Two possibilities for threshold detectors

- Skewed inverter with fixed switching voltage



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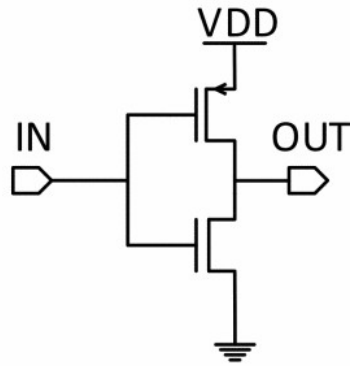

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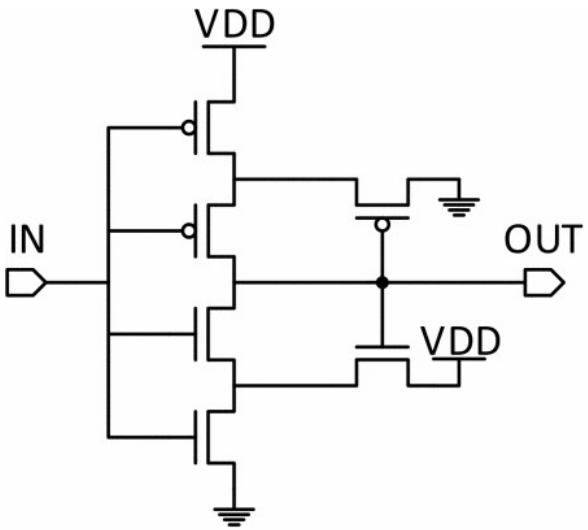
- Skewed inverter with fixed switching voltage
- Schmitt trigger with hysteresis, i.e. high threshold on rising edge and low threshold on falling edge



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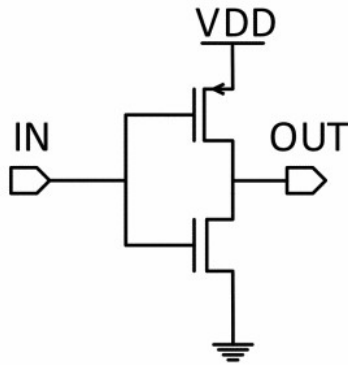

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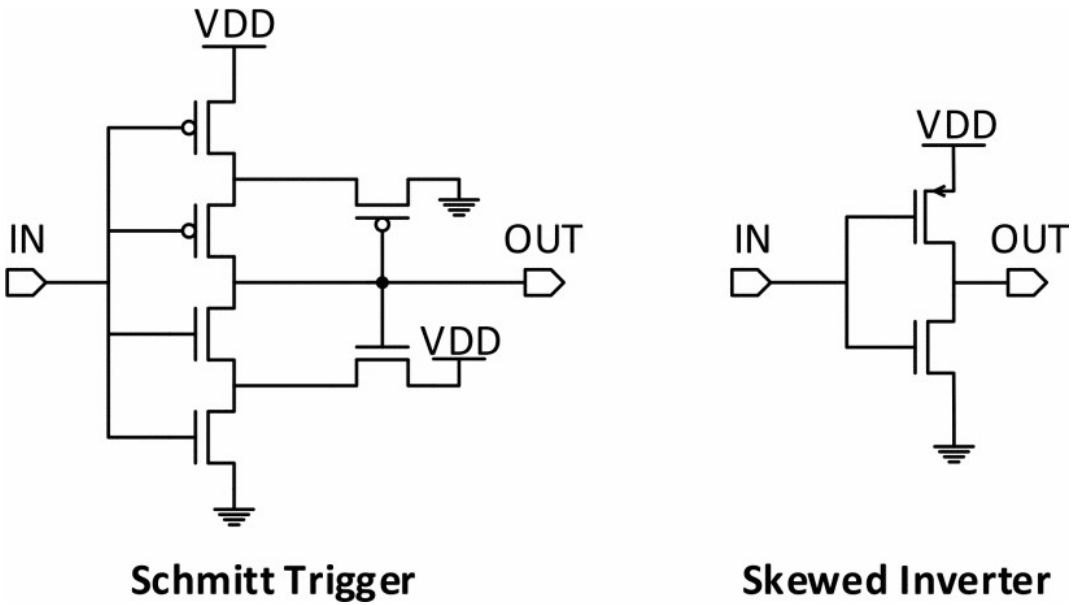
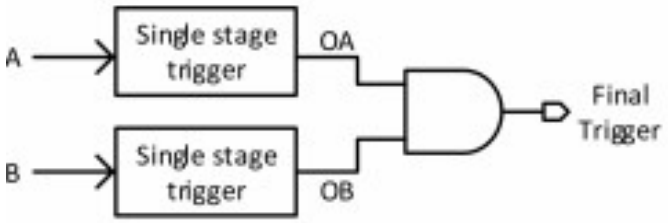
  Paper chooses Schmitt trigger as it extends trigger and retention time



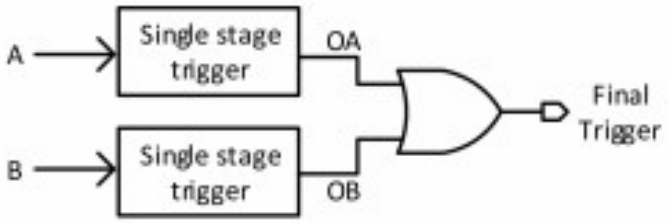
Schmitt Trigger

Skewed Inverter

Possibility: Chaining Triggers Together



Final Trigger = OA & OB
Either A or B triggers



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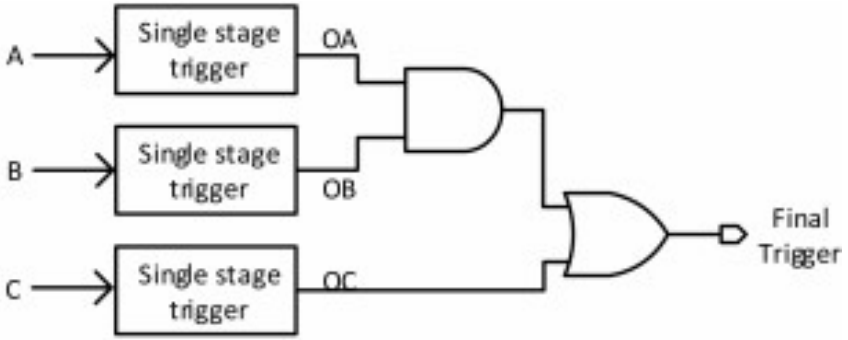

Final Trigger = (OA & OB) | OC
One of A and B trigger, C trigger

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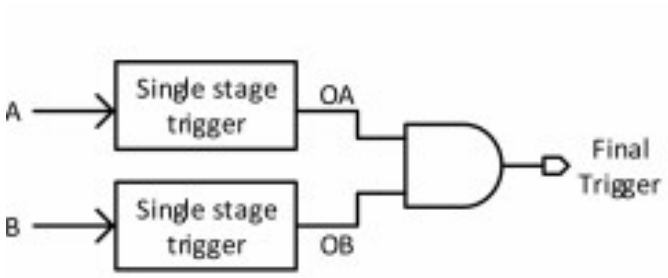

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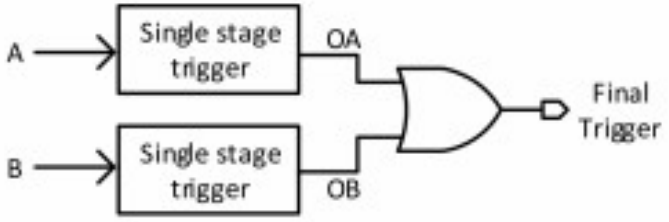

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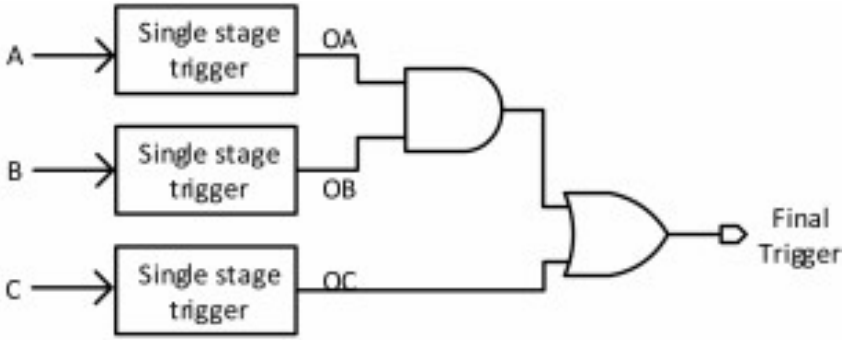

Final Trigger = (OA & OB) | OC
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- Triggers can be combined to form more complex trigger mechanisms

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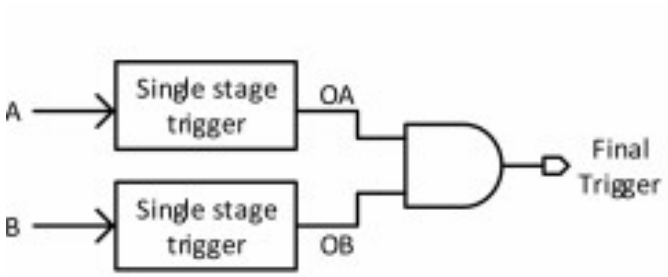

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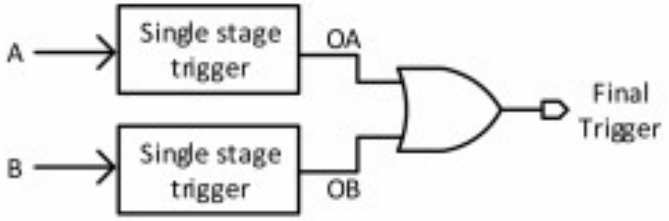

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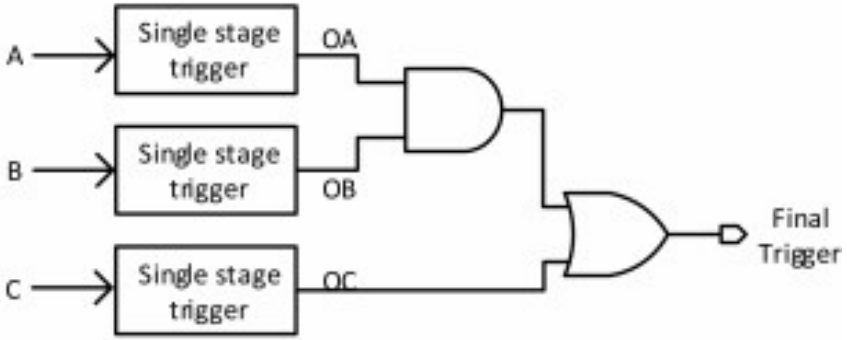

Final Trigger = (OA & OB) | OC
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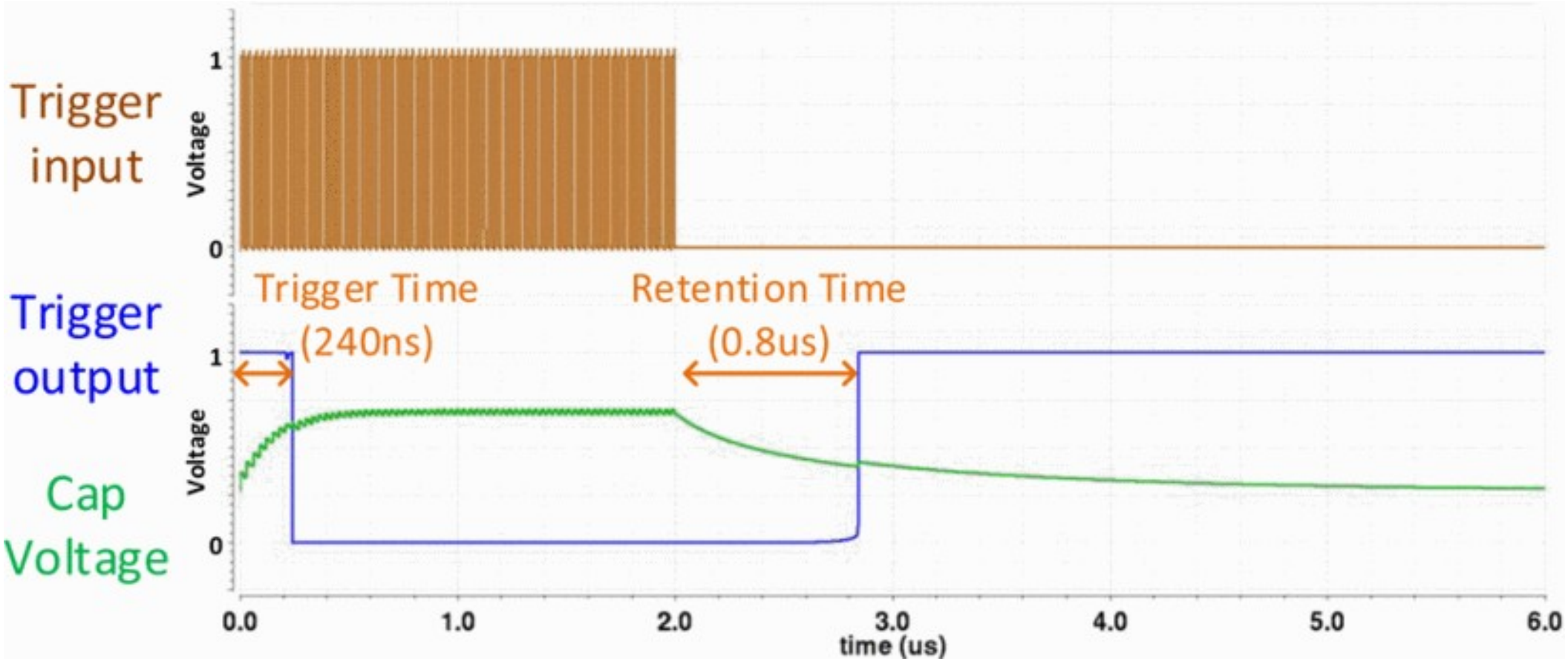
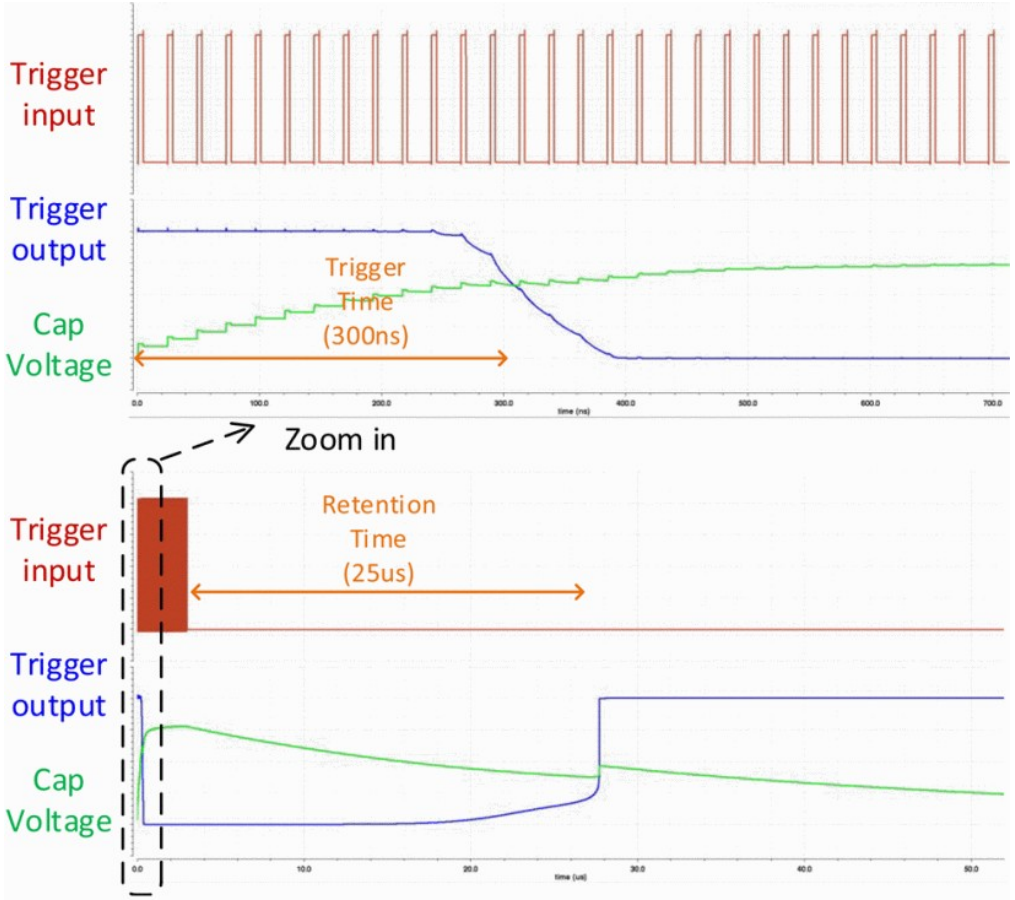
- Triggers can be combined to form more complex trigger mechanisms
- Can be used to construct well hidden multi-stage triggers

SPICE Simulation Results

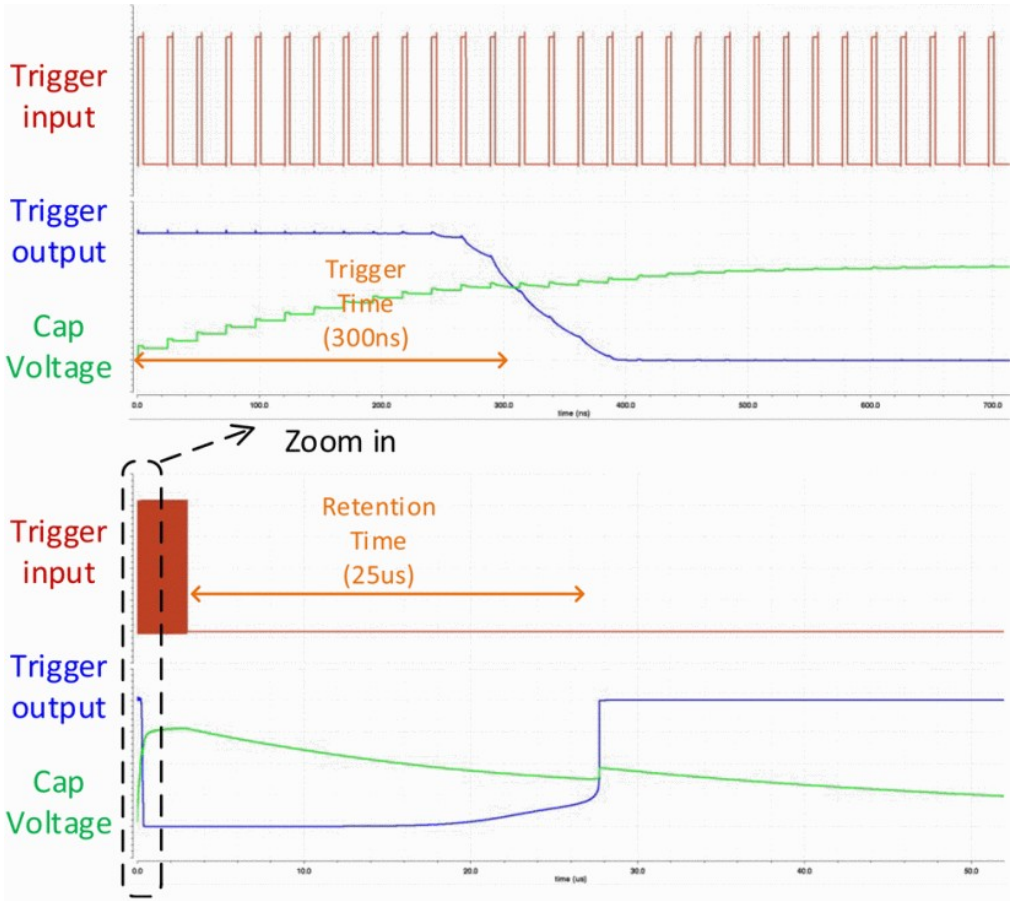


SPICE Using I/O Devices in 65nm CMOS



SPICE Using I/O Devices in 65nm CMOS

- To mitigate gate leakage, I/O Device Cells can be used instead of normal standard cells



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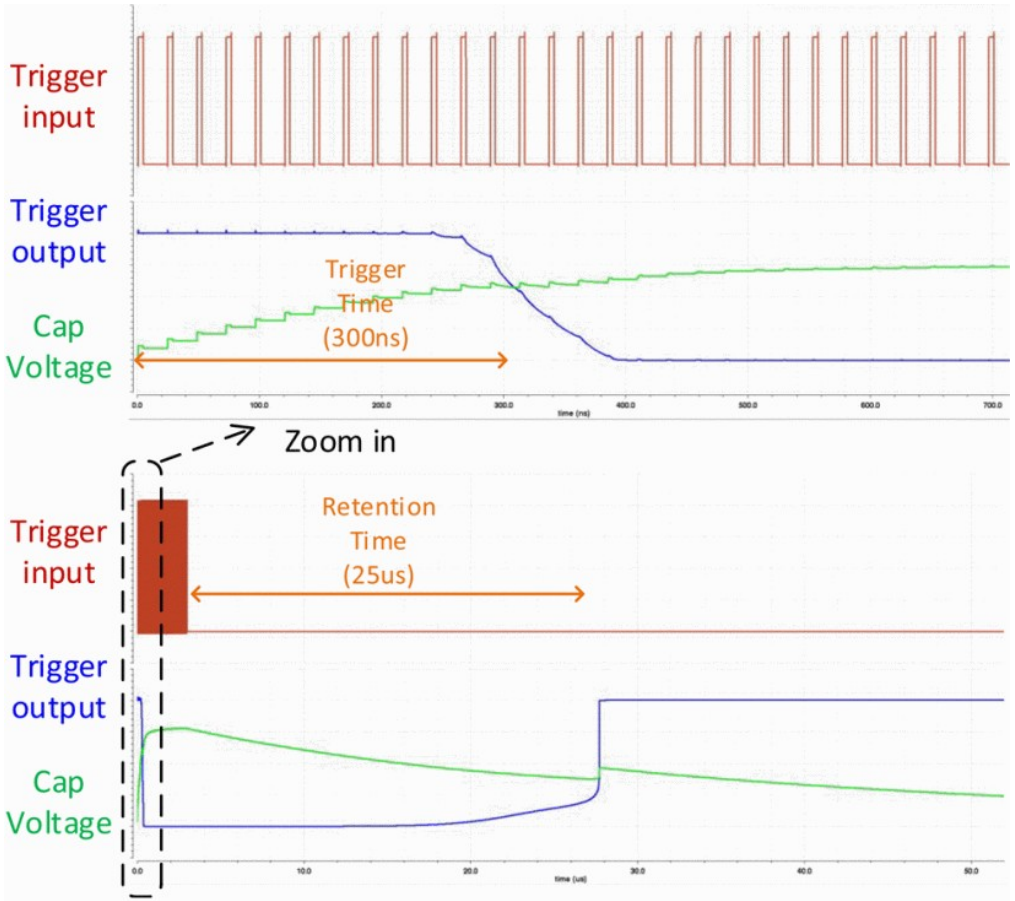

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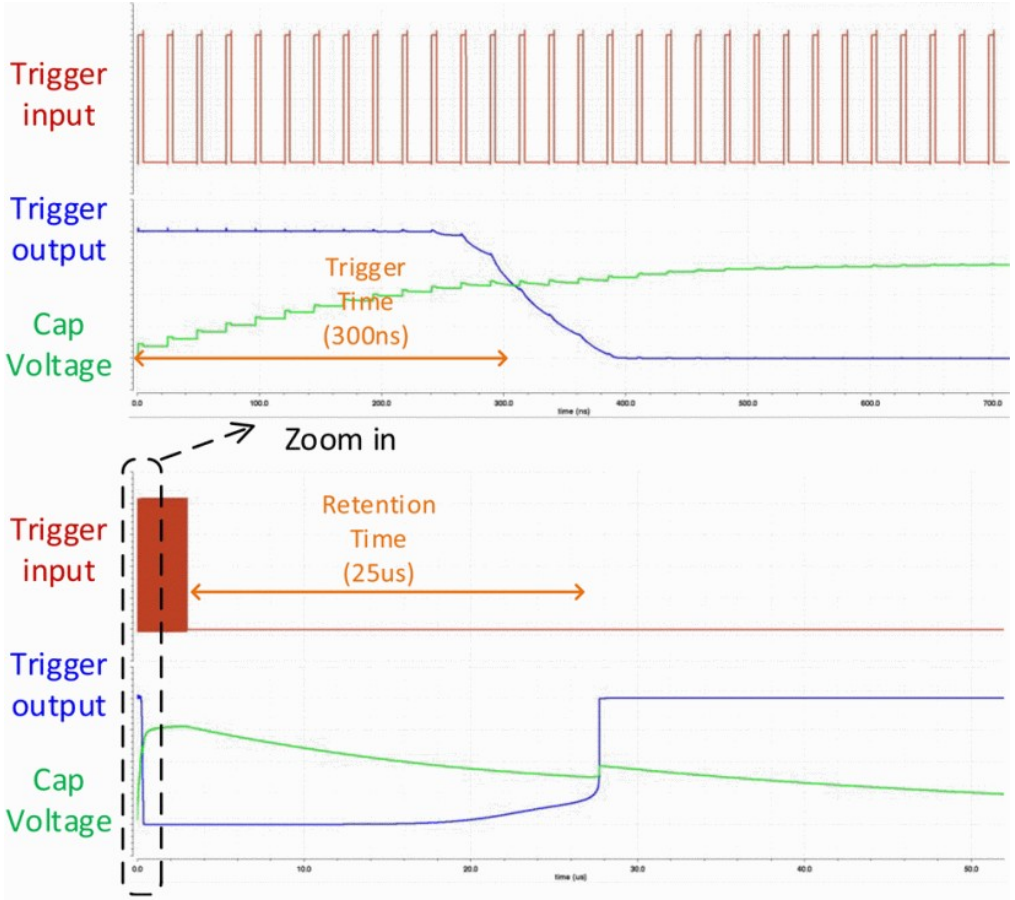

SPICE Using I/O Devices in 65nm CMOS

- To mitigate gate leakage, I/O Device Cells can be used instead of normal standard cells
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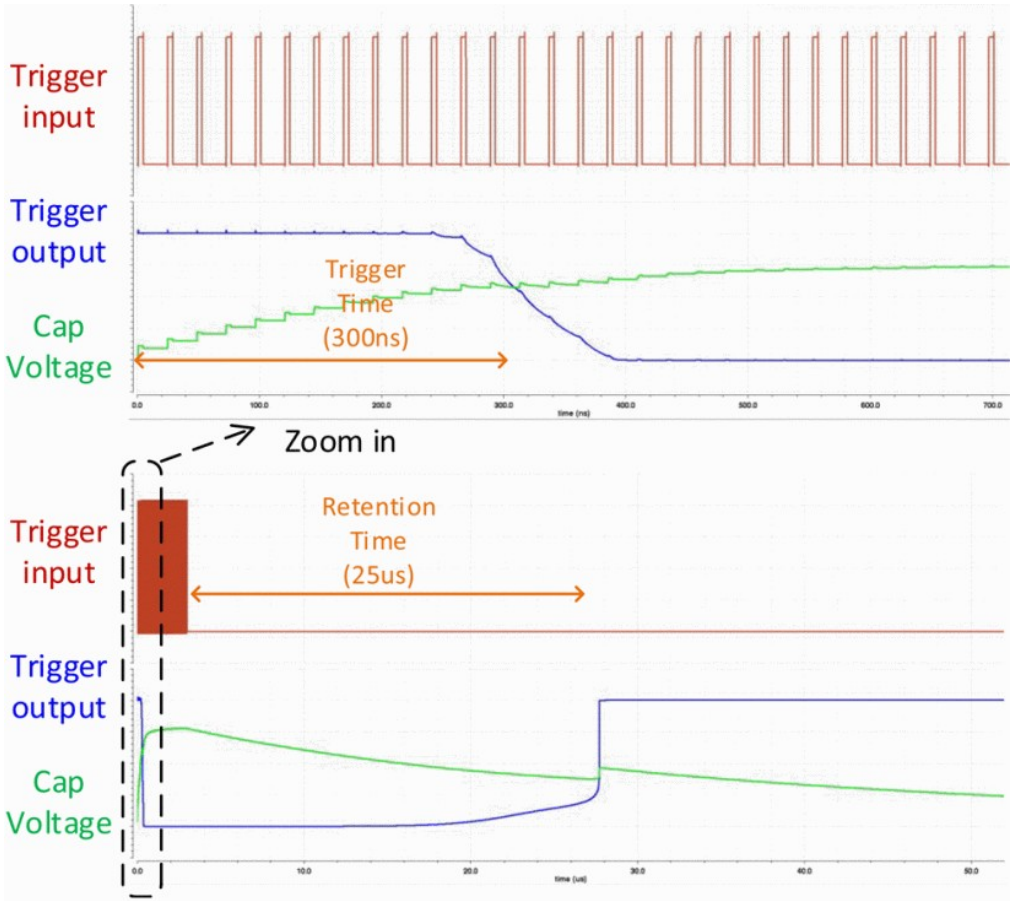
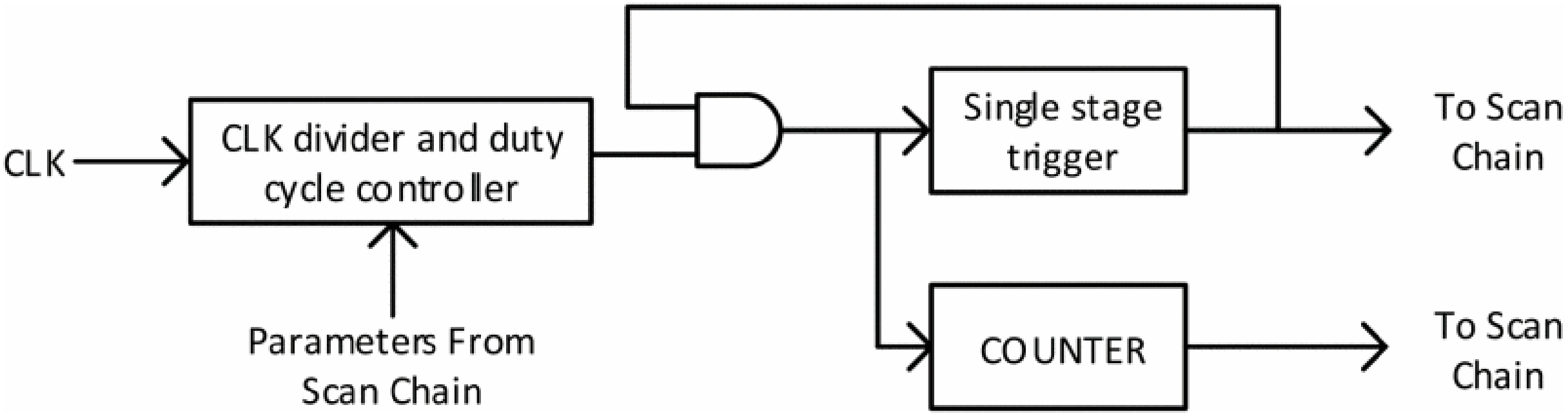
- Uses slightly more chip area
- Also simulated in 65nm low power CMOS



Stand-alone Testing Structure



Results Across 10 Chips (1V, 25°C)

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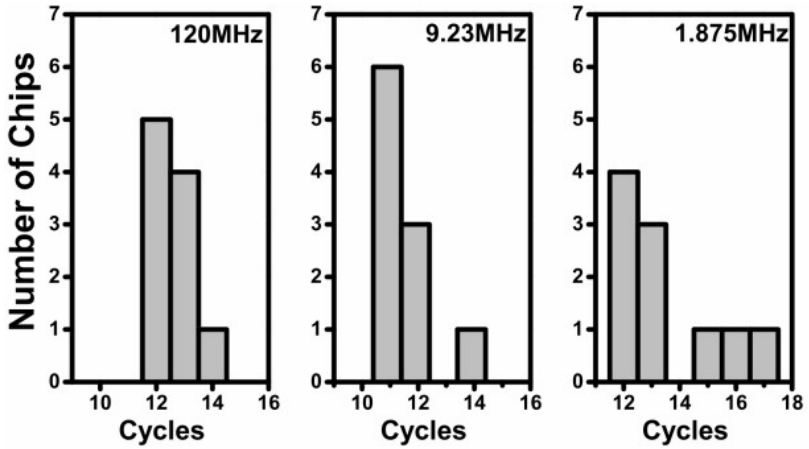
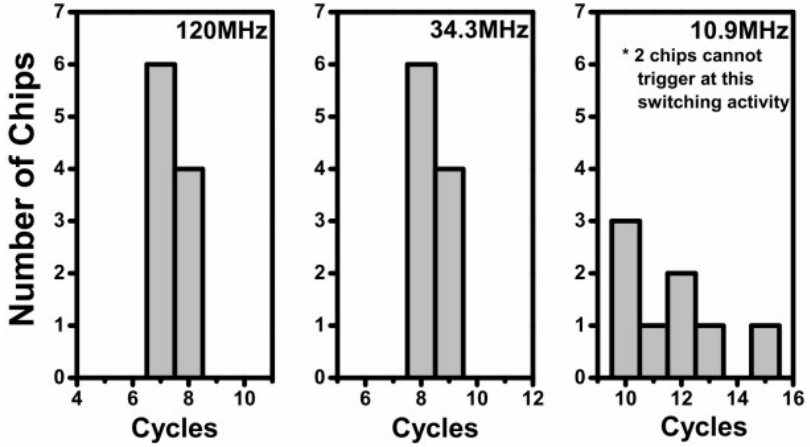


(a) Distribution of analog trigger circuit using IO device



(b) Distribution of analog trigger circuit using only core device

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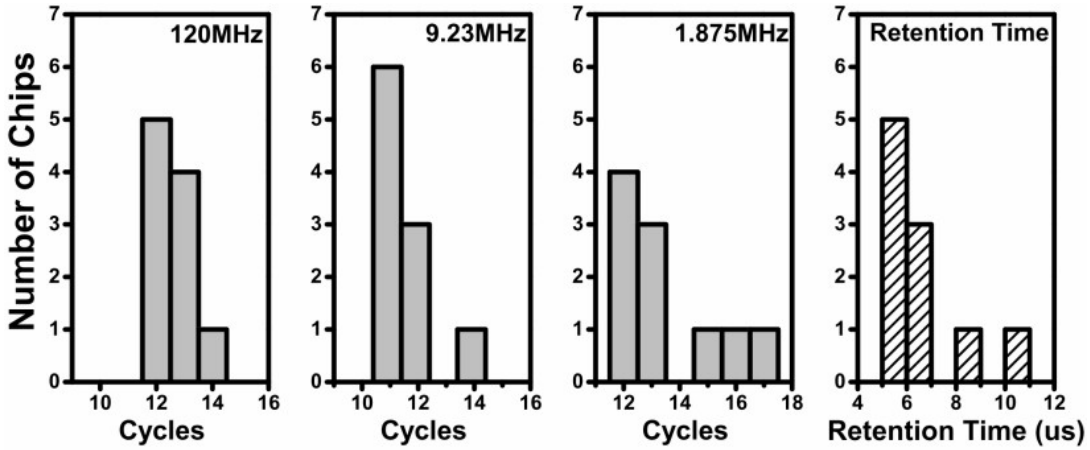
- Also shows number of chips which show a certain retention time in µs



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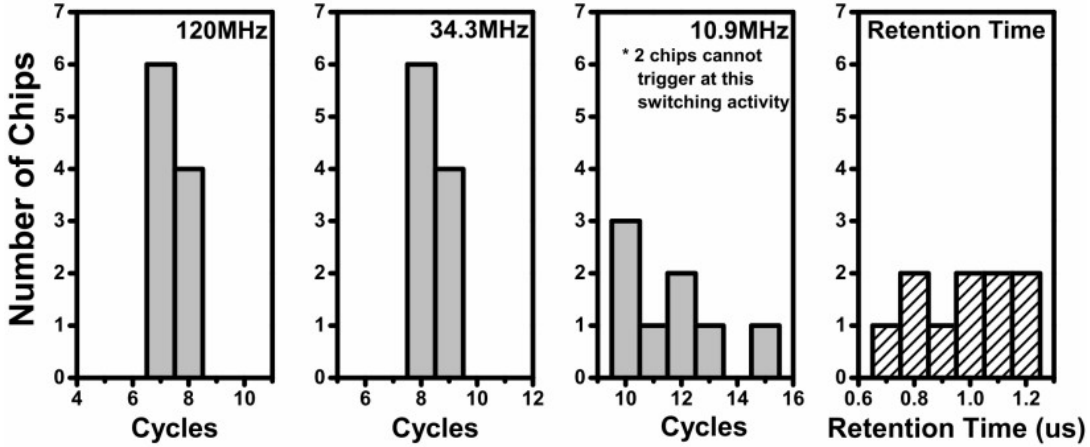

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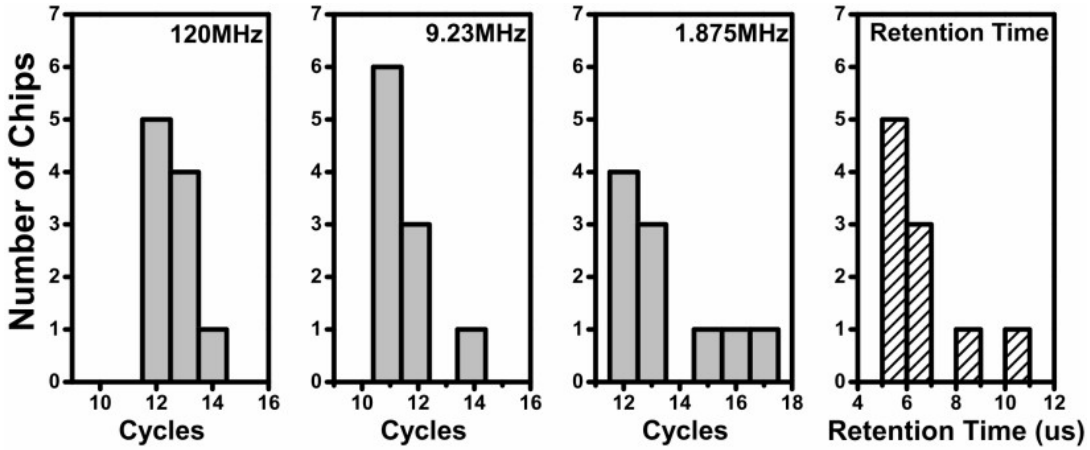
- Shows number of chips which show a certain trigger time in cycles at different switching frequencies
- Also shows number of chips which show a certain retention time in µs
- Shows robustness against manufacturing variations



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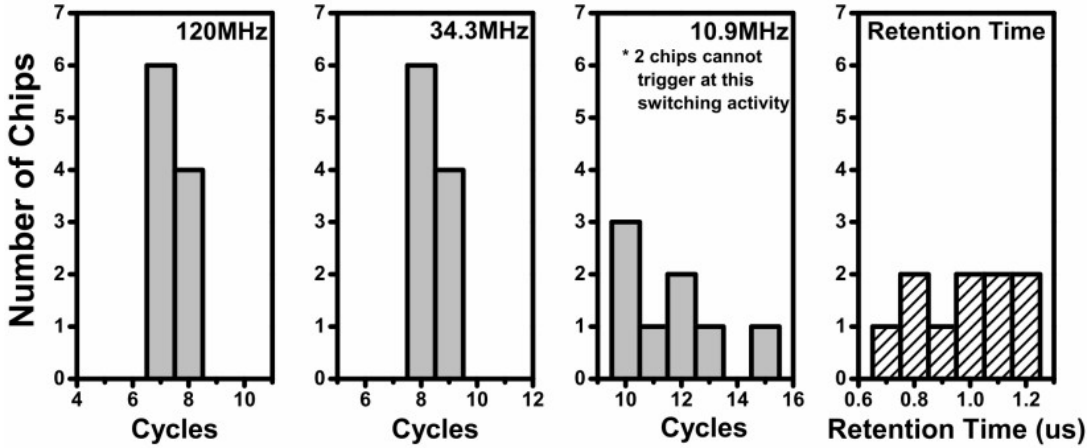
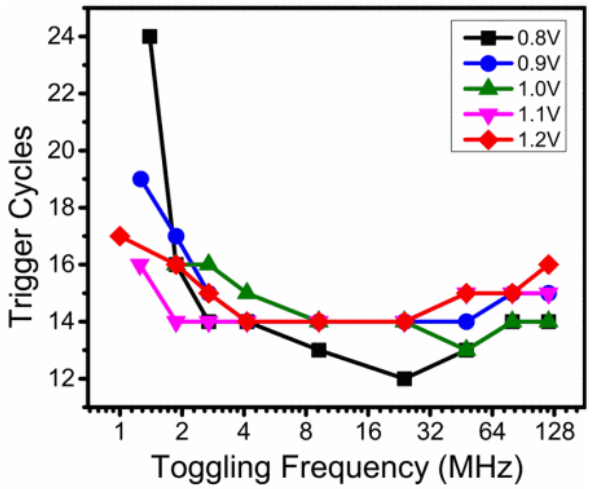


(b) Distribution of analog trigger circuit using only core device

Varying the Voltage

Varying the Voltage

- Shows the trigger time in cycles for a given voltage and frequency



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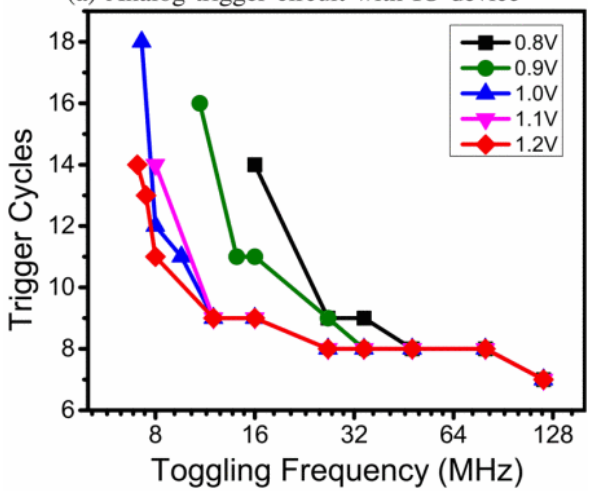
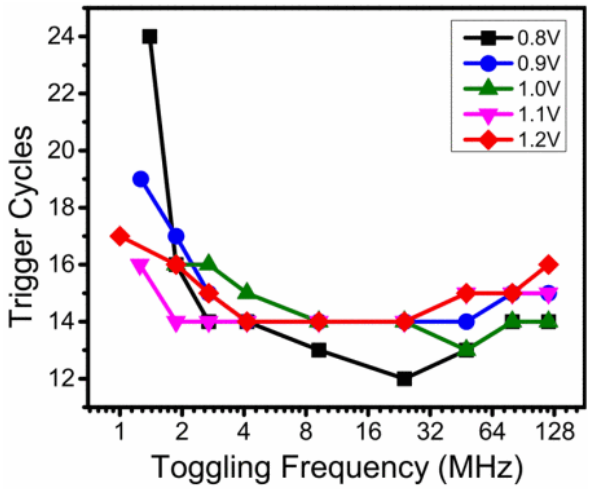


(b) Analog trigger circuit with only core device

Varying the Voltage

- Shows the trigger time in cycles for a given voltage and frequency
- Shows robustness across variations in the supply voltage



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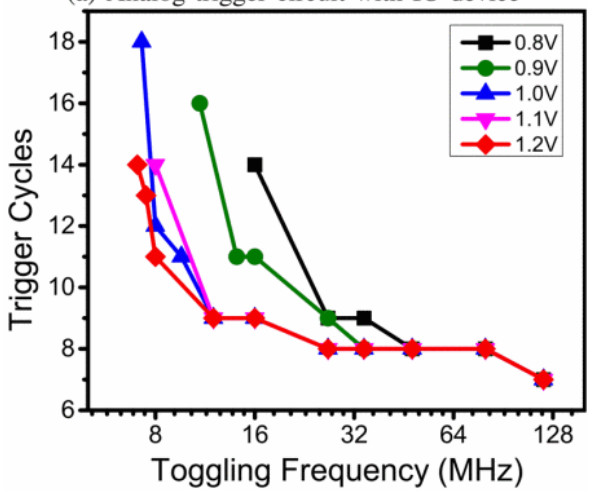

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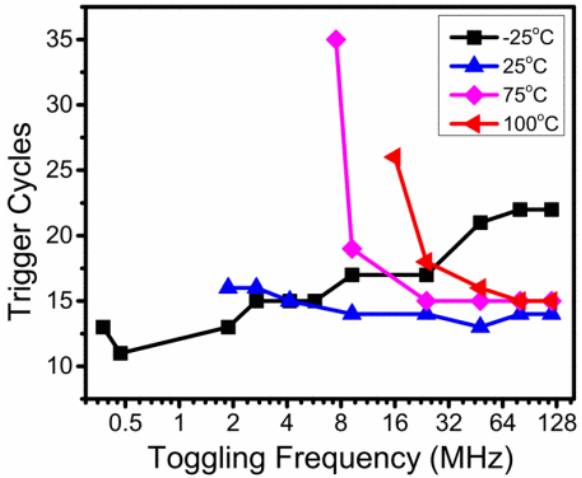

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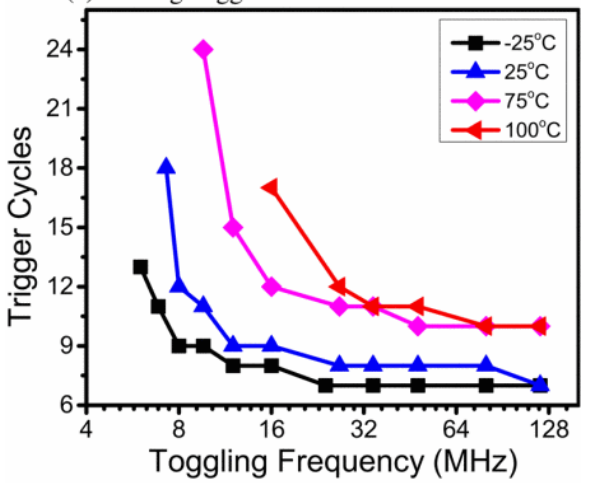

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Varying the Temperature

- Shows the trigger time in cycles for a given temperature and frequency
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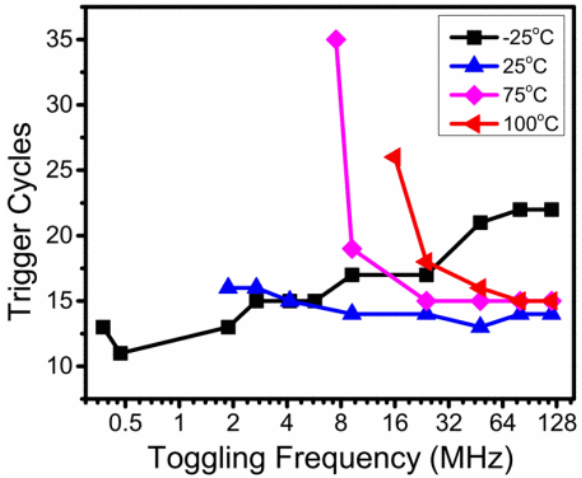

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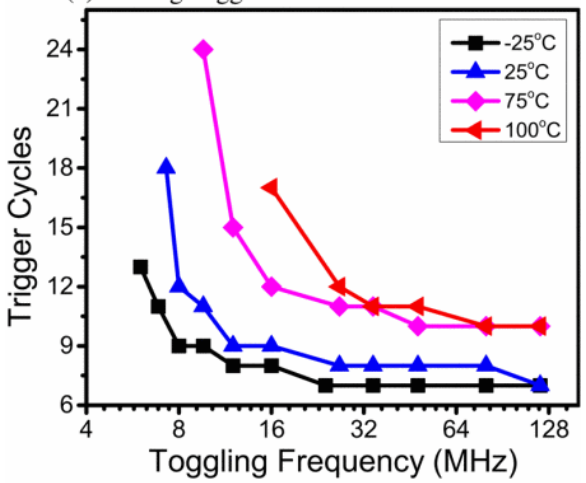
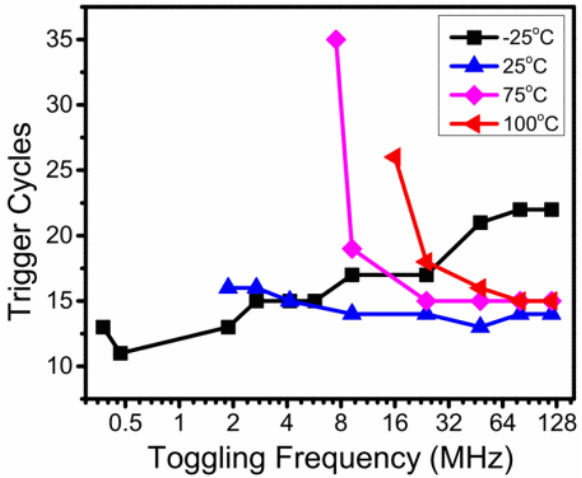


(b) Analog trigger circuit with only core device

Varying the Temperature

- Shows the trigger time in cycles for a given temperature and frequency
- Shows robustness across variations in the ambient temperature
- The paper states that both single and two-stage attacks trigger in all 10 chips over 6 tested temperatures



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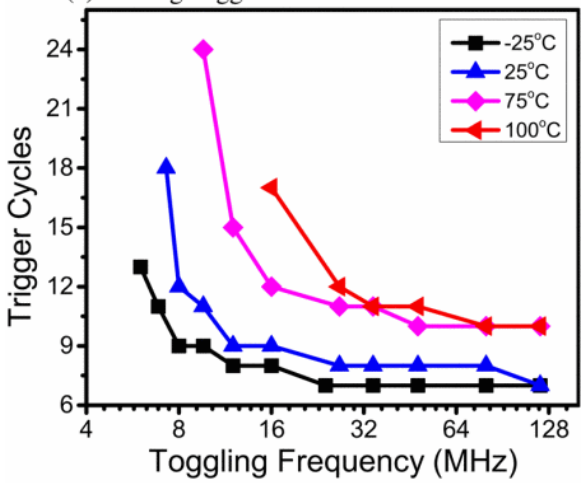

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Evaluation of Side Channel Information

Backup Slides

Evaluation of Side Channel Information

- Power consumption of the chip measured down to 1 µA at 1V and 25°C

Program	Power (mW)
Standby	6.210
Basic math	23.703
Dijkstra	16.550
FFT	18.120
SHA	18.032
Search	21.960
Single-stage Attack	19.505
Two-stage Attack	22.575
Unsigned Division	23.206

Table III: Power consumption of our test Chip running a variety of benchmark programs.

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- Well below normal power fluctuations
- Temperature and propagation delays are nearly unaffected by A2 as it is as small as one gate

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- X86 has also likely more viable victim wires
- Due to the complexity of X86, A2 should also be more difficult to detect
- The only expected challenge is maintaining controllability over the many redundant functional units in X86