Ambit: In-Memory Accelerator for Bulk Bitwise Operations Using Commodity DRAM Technology

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Moritz Knüsel

Seminar on Computer Architecture

Executive Summary

- **Problem: Bulk bitwise operations**
  - Problematic when used on large in-memory bitvectors
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  - AND, OR and NOT are sufficient to compute all bitwise operations (NAND,XOR,...)
  - **less than 1%** area overhead
- Results compared to state-of-the-art:
  - **32x** performance improvement, **35x** energy reduction averaged across 7 bulk bitwise operations
  - **3x-7x** performance improvement for real-world data intensive workloads

Background, Problem & Goal

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  - Set operations
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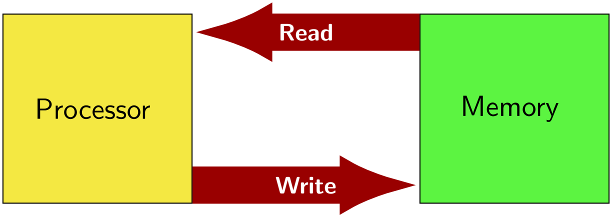
- Bulk bitwise operations become problematic if
  - The bitvectors involved are very large
  - They cannot be combined with other processing

Problem

Memory bandwidth is a bottleneck



Problem

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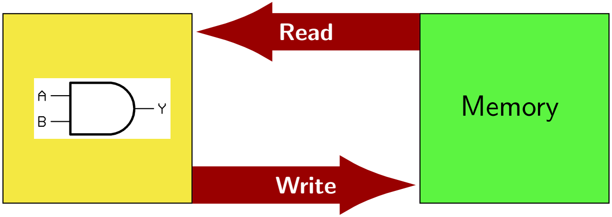
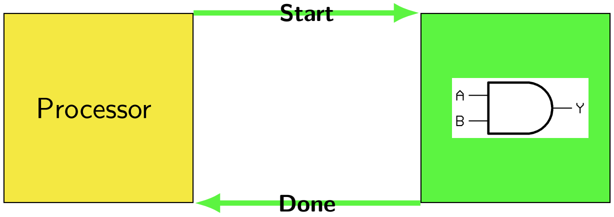


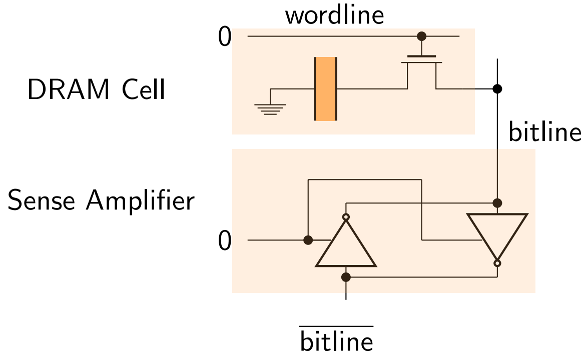
Goal

Idea: Perform bitwise operations directly in DRAM

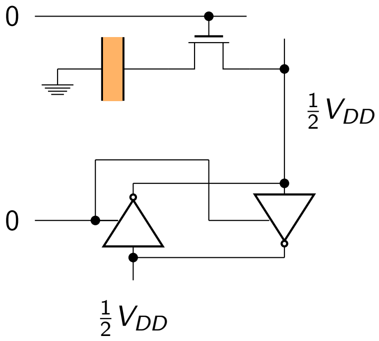


Mechanism

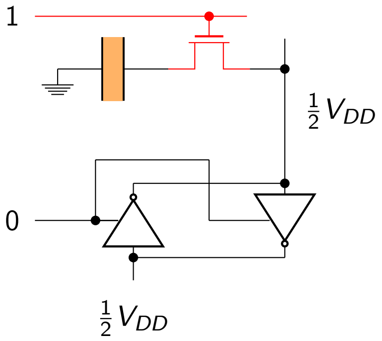
Background on DRAM



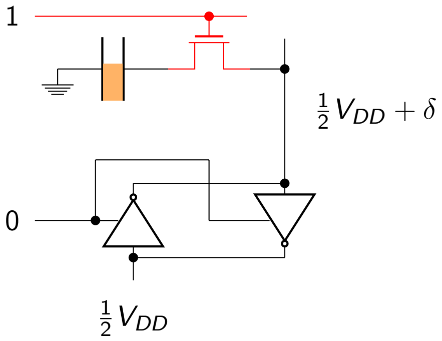
Precharged State



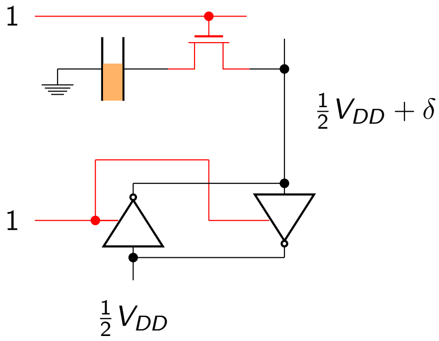
Wordline Enable



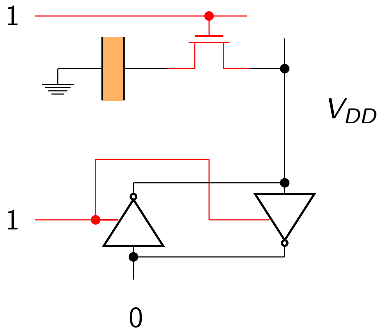
Charge Sharing Phase



Sense Amplifier Enable



Activated State



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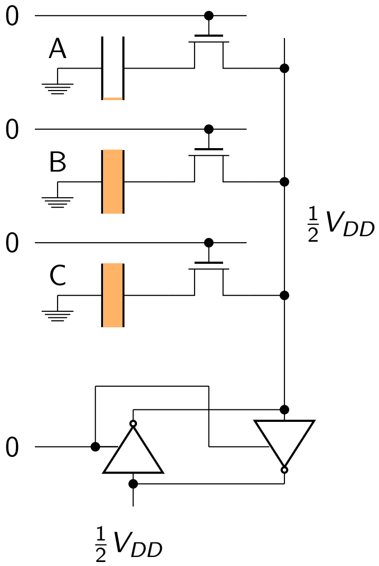
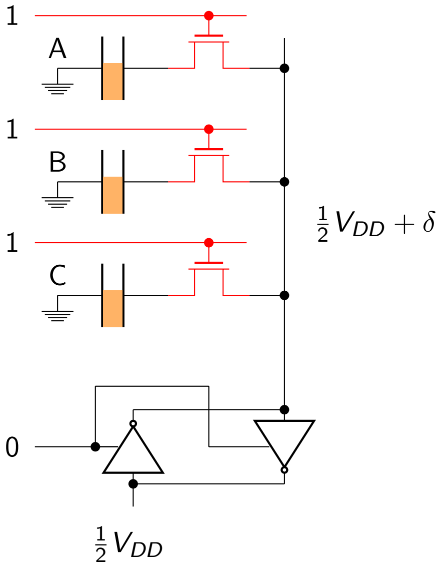
- The final state of the bitline depends mostly on the deviation of the bitline after charge sharing
- **Key observation**: By activating three rows at once, the bitwise majority of the three rows is computed

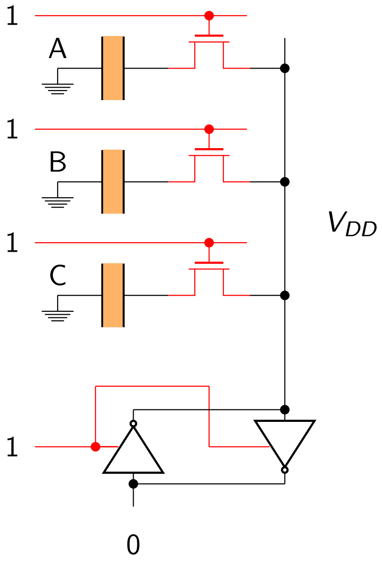
Initial State



Triple Row Activation (**TRA**)



After Sense Amplification



Ambit-AND-OR

C	A	B	Bitwise Majority
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
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1	0	0		0
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1	1	0		1
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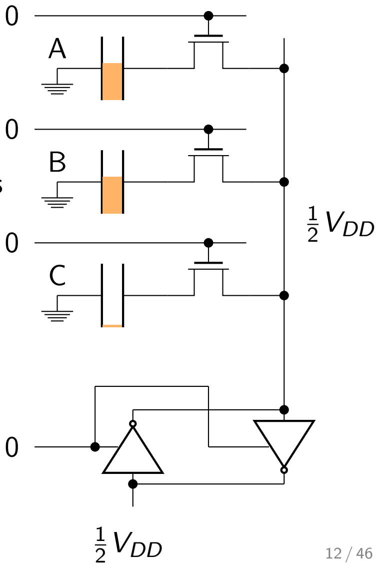

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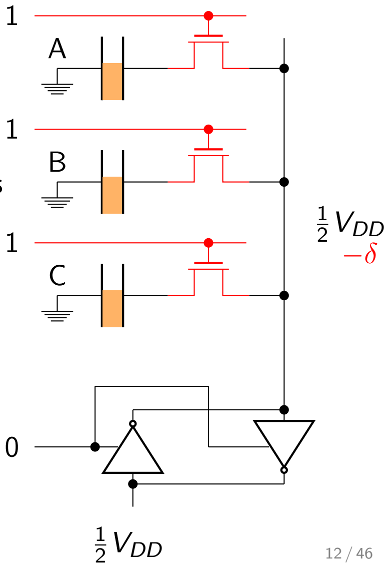

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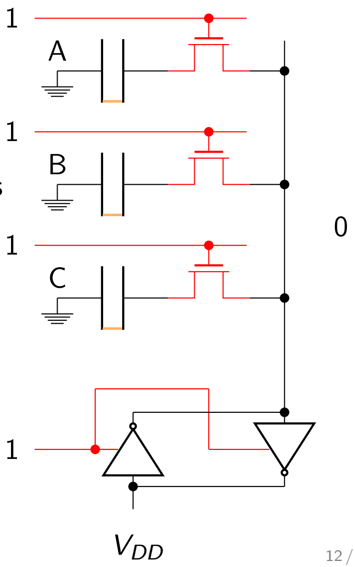

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- All rows in a TRA have been refreshed recently

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- Ambit relies on **RowClone** for copying data and initializing rows

  Vivek Seshadri, Yoongu Kim, Chris Fallin, Donghyuk Lee, Rachata Ausavarungnirun, Gennady Pekhimenko, Yixin Luo, Onur Mutlu, Michael A. Kozuch, Phillip B. Gibbons, and Todd C. Mowry

  RowClone: Fast and Energy-Efficient In-DRAM Bulk Data Copy and Initialization

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- How can we transmit a command to activate three rows without sending and decoding 3 addresses?
- The solution: We use a **reserved address** to communicate a TRA on the designated rows
- Also, we can split up the row decoder into two parts, which leads to a simpler design and better performance

Mechanism

Ambit-NOT

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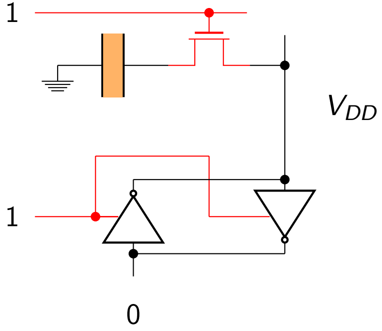
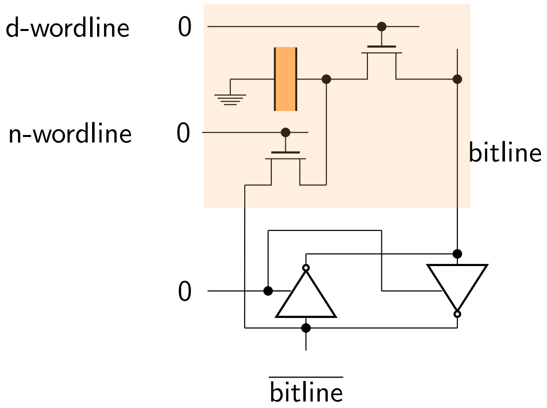
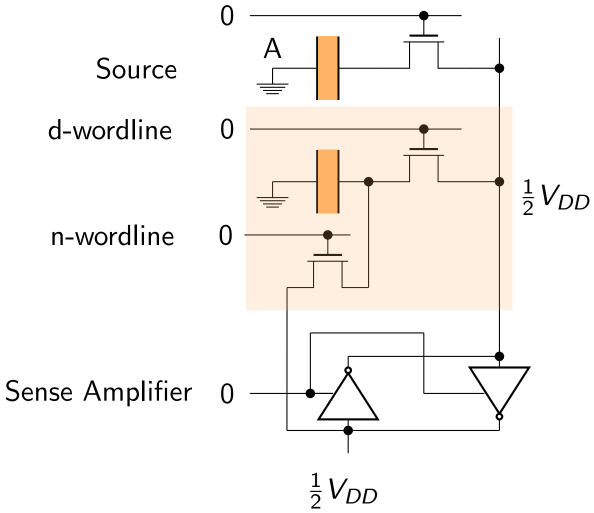
Notice that, during normal DRAM operation, the voltage level of $\overline{\text{bitline}}$ is the negation of the value in the cell.



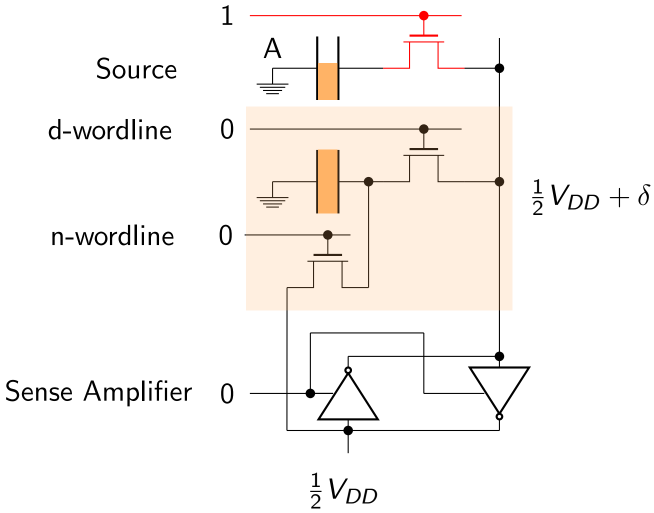
Dual Contact Cell (DCC)



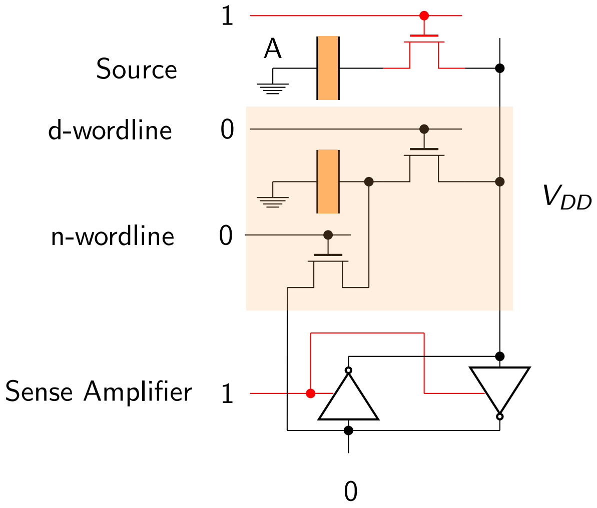
Initial State



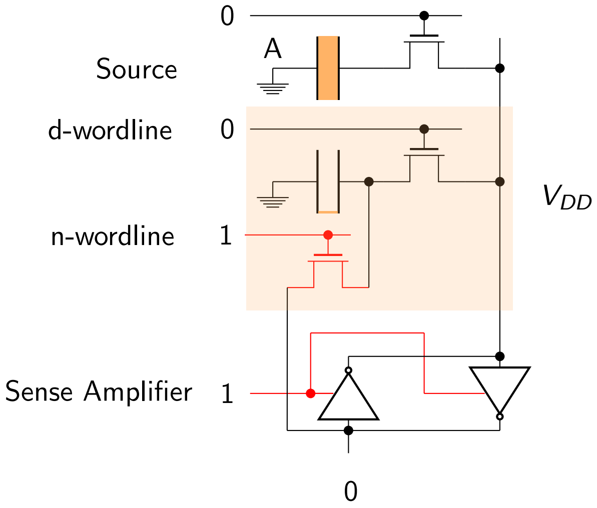
After Charge Sharing



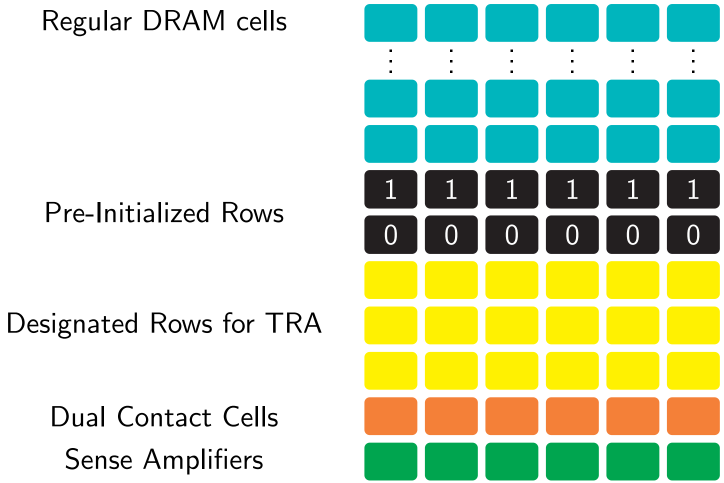
Activated Source Row



Activated n-Wordline



Implementation



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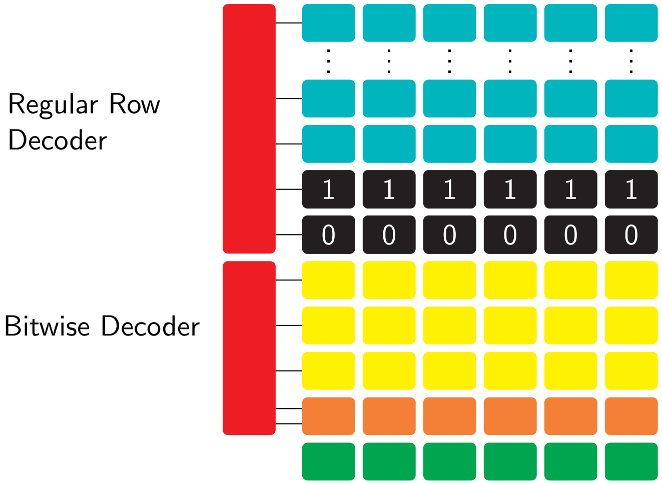
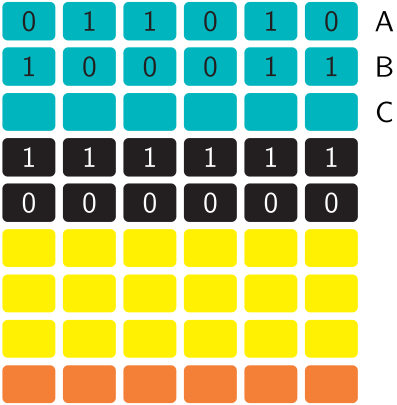


Computing C = A XOR B

- A XOR B = (A OR B) AND NOT (A AND B)



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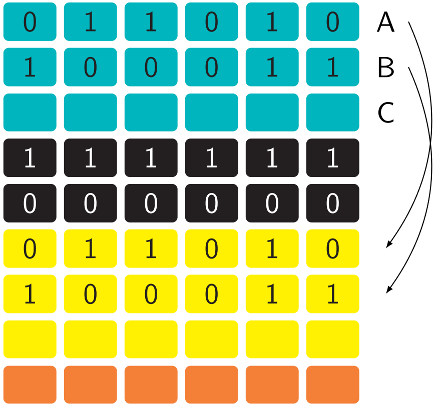

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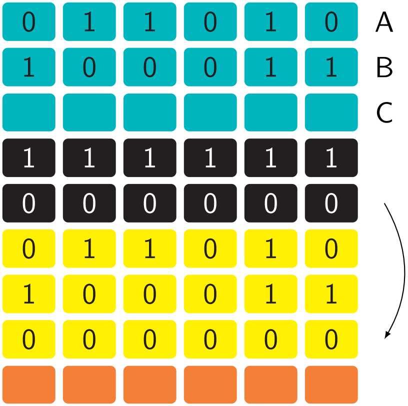

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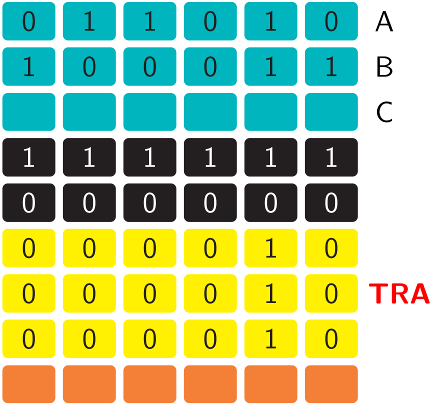

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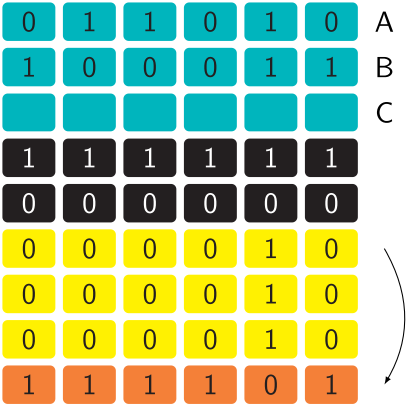

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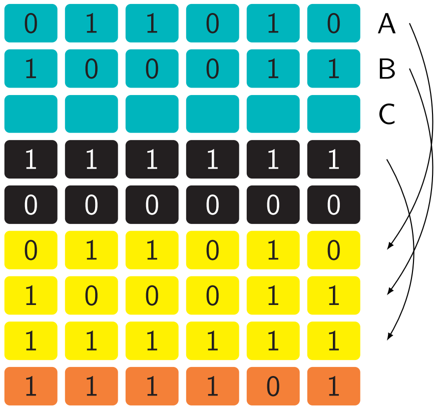

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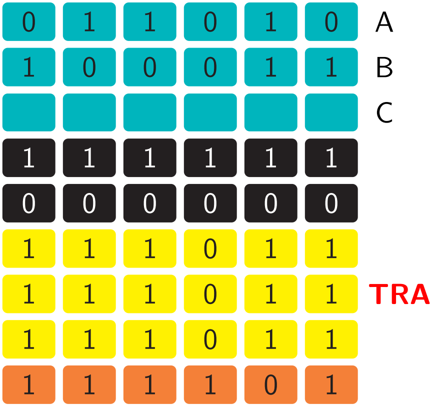

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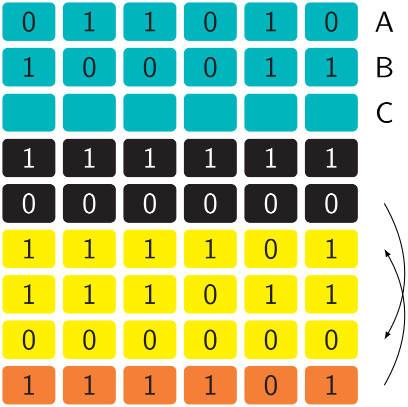

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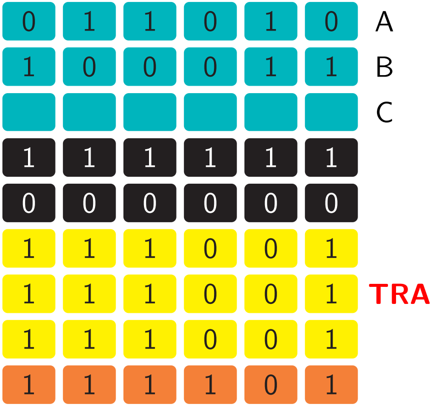
- Do a TRA and copy the result to C



0	1	1	0	1	0	A
1	0	0	0	1	1	B
						C
1	1	1	1	1	1	
0	0	0	0	0	0	
1	1	1	0	0	1	
1	1	1	0	0	1	**TRA**
1	1	1	0	0	1	
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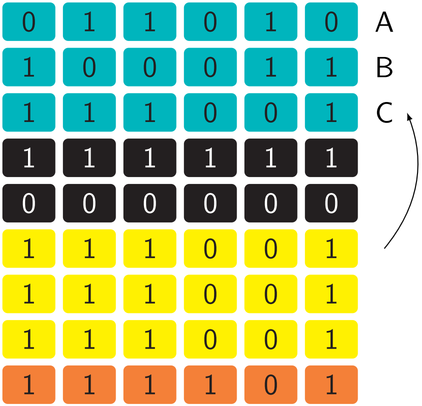

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- As a PCIe device
  - Simple approach, similar to other accelerators
- Directly plugged onto the memory bus
  - Makes sense since Ambit uses the same interface as regular DRAM
  - However, this requires additional support such as a new CPU instruction

Integrating Ambit with the System

Proposal: New CPU instruction

bb*op* dst src1 [src2] size

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- Size is required to be a multiple of the row size
- Source and destination need to be row-aligned
- The CPU checks the constraints. If they are met, Ambit is used to complete the operation. Otherwise, the CPU does the operation normally.

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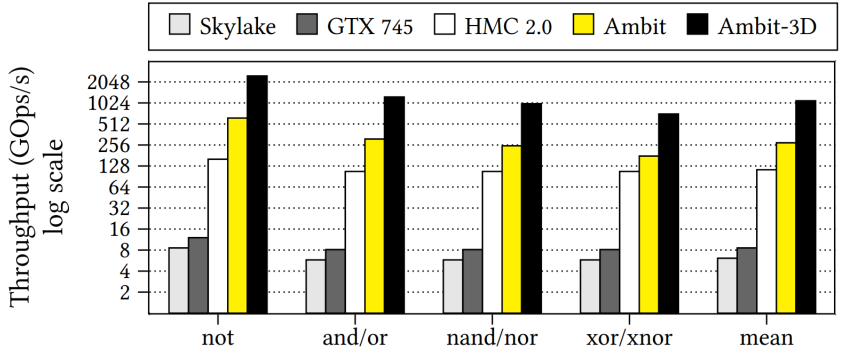
- Cache coherence
  - Ambit changes the contents of memory directly
  - Existing **DMA techniques** can be utilised
  - Alternatively, the bb*op* instruction could implicitly manage the caches as well

Key Results: Methodology & Evaluation

Ambit Throughput & Energy

Microbenchmarks with 32MB input vectors



Ambit Throughput & Energy

- Energy is estimated for DDR3-1333 using the Rambus power model
- Energy numbers include only the DRAM and channel energy, and not the energy consumed by the processor

DRAM & Channel Energy (nJ/KB)

Design	not	and/or	nand/nor	xor/xnor
DDR3	93.7	137.9	137.9	137.9
Ambit	1.6	3.2	4.0	5.5
Energy reduction	**59.5x**	**43.9x**	**35.1x**	**25.1x**

Methodology

Evaluations were carried out using the Gem5 full-system simulator. Major simulation parameters:

Processor	x86, 8-wide, out-of-order, 4 Ghz 64-entry instruction queue
L1 cache	32 KB D-cache, 32 KB I-cache, LRU policy
L2 cache	2 MB, LRU policy, 64 B cache line size
Memory Controller	8 KB row size, FR-FCFS scheduling
Main memory	DDR4-2400, 1-channel, 1-rank, 16 banks

Workloads:

- Set Operations - Comparing to bitvectors and red-black trees
- Bitmap Indices
- Bitweaving - Column scans using bulk bitwise operations

Workload: Sets

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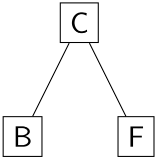
- The set $\{B, C, F\}$ may be represented by:

a tree



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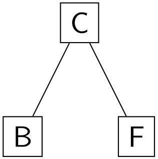

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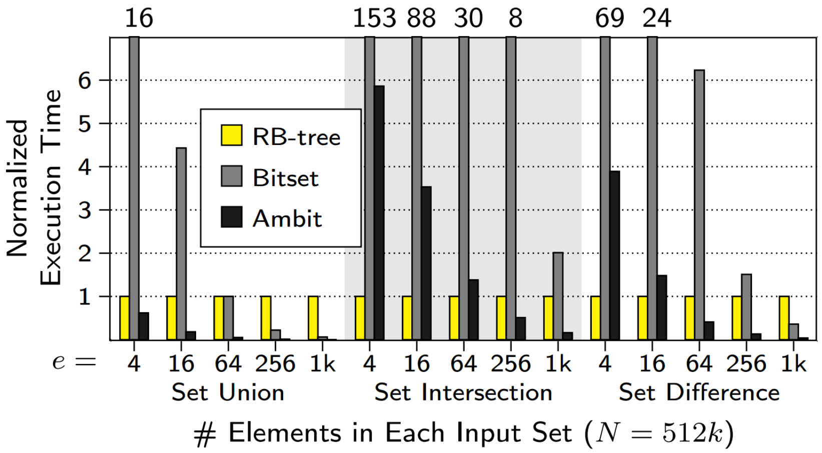
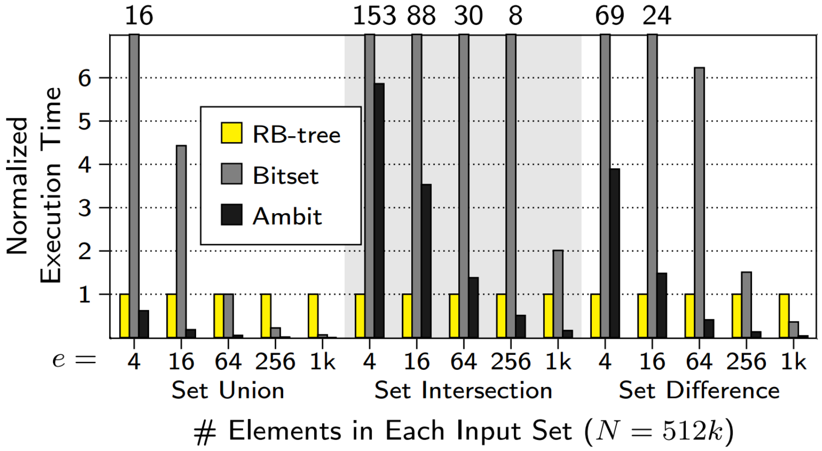
- Set operations on trees **scale with the number of elements in the set**, whereas bitvectors also have to **process elements that are not in the set**

Performance of Set Operations



Performance of Set Operations

- Ambit shifts the balance heavily in favor of bitvectors



Workload: Bitmap Index

- Using bitsets to build database indices

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- As an example, consider this table:

USER_ID	REGION	INCOME_LEVEL
101	east	bracket_1
102	central	bracket_1
103	west	bracket_2
104	east	bracket_2

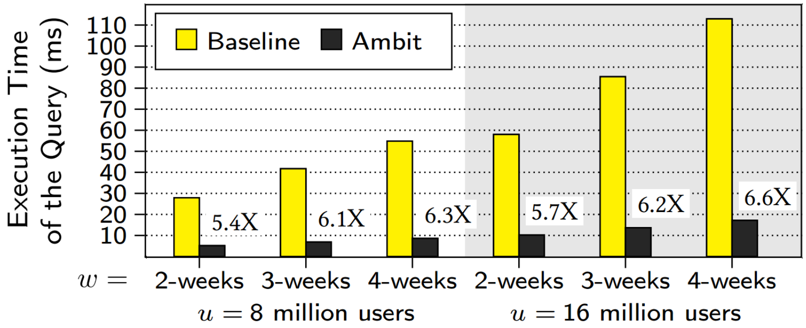
Workload: Bitmap Index

- A bitmap for the REGION and INCOME_LEVEL columns might look like this:

REGION			INCOME	
east	central	west	bracket_1	bracket_2
1	0	0	1	0
0	1	0	1	0
0	0	1	0	1
1	0	0	0	1

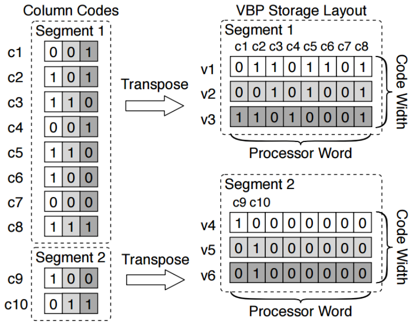
Bitmap Index Performance

Running an analytic query using a bitmap index.
Each query takes $\mathrm{O}(w)$ bulk bitwise operations, each of which takes $\mathrm{O}(u)$ time.



Workload: Bitweaving

- Used to speed up predicate evaluation in databases
- Tables are stored columnwise, but at the bitlevel

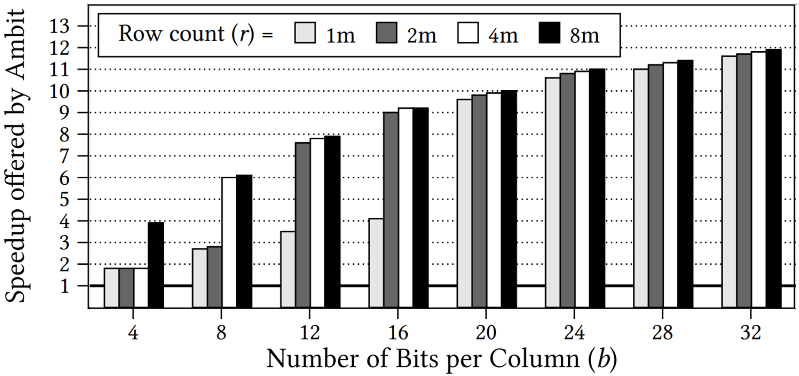


- For details on how it works, refer to **BitWeaving: Fast Scans for Main Memory Data Processing** by Yinan Li and Jignesh M. Patel

Bitweaving Performance

- Evaluated Query:

```
select count(*) from T where c1 <= val <= c2
```



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  - **Activate multiple DRAM rows** to compute AND/OR
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    - **less than 1%** area overhead
- Results compared to state-of-the-art:
    - **32x** performance improvement, **35x** energy reduction averaged across 7 bulk bitwise operations
    - **3x-7x** performance improvement for real-world data intensive workloads

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- Potential for further work

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  - **Pinatubo: A Processing-in-Memory Architecture for Bulk Bitwise Operations in Emerging Non-volatile Memories** (2016)
    Shuangchen Li, Cong Xu, Qiaosha Zou, Jishen Zhao, Yu Lu, Yuan Xie

Questions?

Discussion Starters

How could we better support bitvectors whose length is not a multiple of the row size?

Masking

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- But: Even if mask creation is cheap, it still requires **4 additional operations** to mask off a single useful operation

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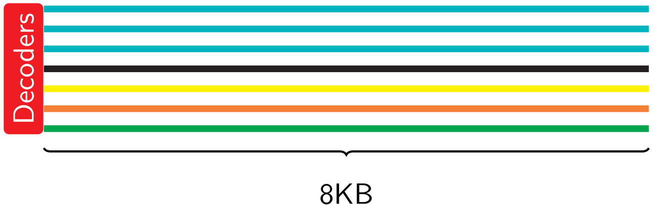

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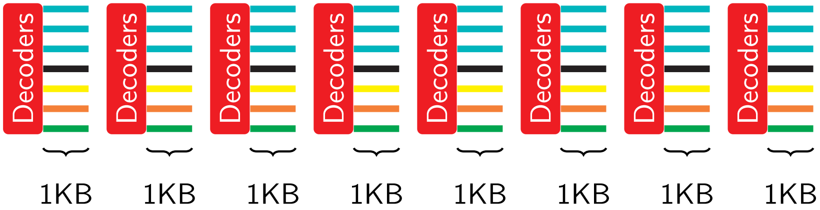

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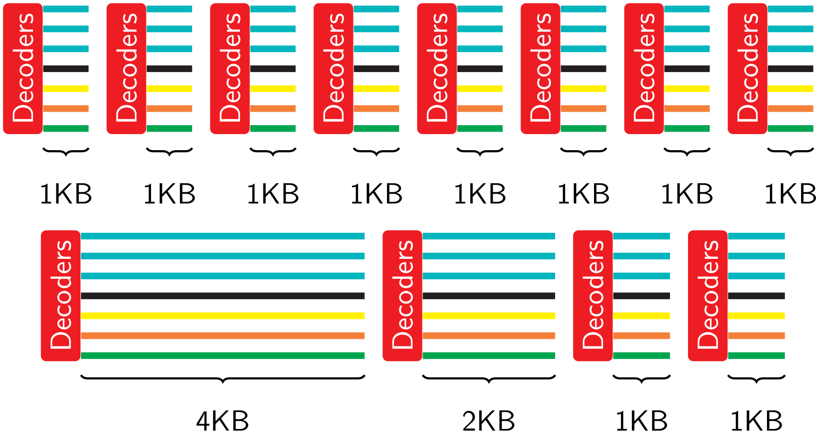

Discussion Starters

What kind of changes thoughout the system might be necessary to make Ambit useful for applications?

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