# Online Design Bug Detection

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# Executive Summary

- Problem:
  - **Increasing complexity** of modern CPUs makes **Design Bugs** in commercial products **more common**
  - They are hard to fix/avoid in software and usually unfixable in hardware
- Goal:
  - develop hardware solutions that enables **detecting** when a **Design Bug triggered**
  - has to be **flexible** to detect new bugs as they are discovered

# Executive Summary

- Contributions:
  - in-depth **study of design bugs** of a quasi-commercial CPU at a low level
  - novel mechanism to **monitor** internal CPU signals and deciding whether a Design Bug can be triggered
  - Makes hardware "updatable" with bug patches like software
- Evaluation:
  - To cover 80% of all bugs found in the study:
  - low power overhead **(3.5%)**
  - moderate area overhead **(10%)**
  - when combined with Hardware Fault Detection, some hardware can be shared and total overhead reduces

# Presentation Outline

Paper Summary

- Problem
- Study of Design Bugs
- Proposed solution
- Major results
- Summary

Analysis

- Strengths
- Weaknesses

Discussion

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- Design **bugs still appear** in widespread commercial CPUs
- Bugs in CPUs make it less usable: Correct software on buggy hardware can produce wrong result
- In commercial CPUs, bugs also lead to bad press and **expensive recalls**
- Many bugs in the past, were usually handled by trying to avoid in software or disabling CPU components

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    - Resulted in 500M $ recall
- Intel F00F bug - certain instruction with the right arguments **locks up entire system**
- AMDs have bugs too - a lot of consecutive pops and rets can cause some AMD Opterons to **incorrectly update stack pointer**

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→ We want to be able to **add** information about design bugs **subsequently**

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  - Fixing and detection is easier, since erroneous hardware **localized to a few gates**
- Timing design bugs
  - Signal latched at the **wrong time**
  - Often fixed by adding/removing a buffer flip-flop

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- Algorithmic or Timing Design bugs
- **Hardware faults** caused by manufacturing process or deterioration of hardware
- Bugs and interference vulnerabilities of **physical nature** (things like Rowhammer) which are hard to detect
- Needs to be detectable by **monitoring internal CPU signals**

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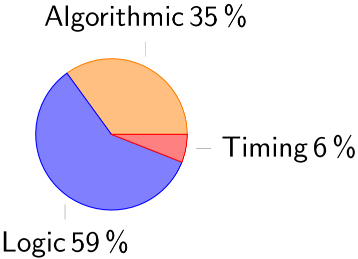

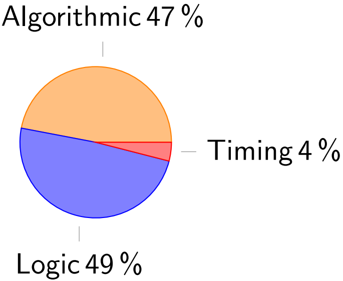

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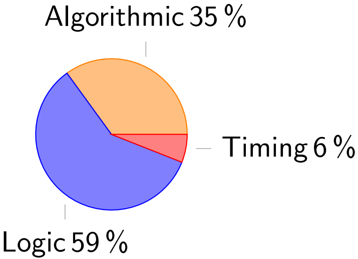

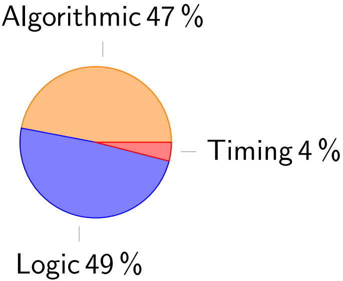

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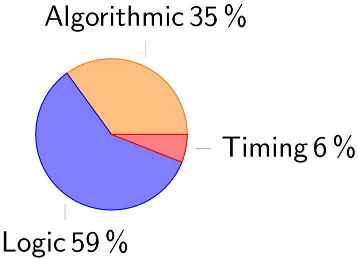

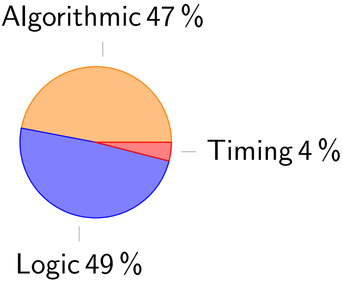

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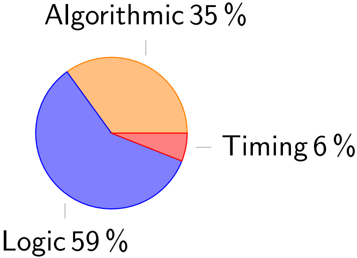
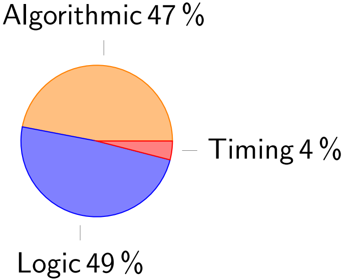




- **Hard to discover** in verification phase, if bug only occurs in very specific states
- Once discovered, **easy to detect** by monitoring source signals
- Algorithmic and Timing bugs could be easier to find in design verification

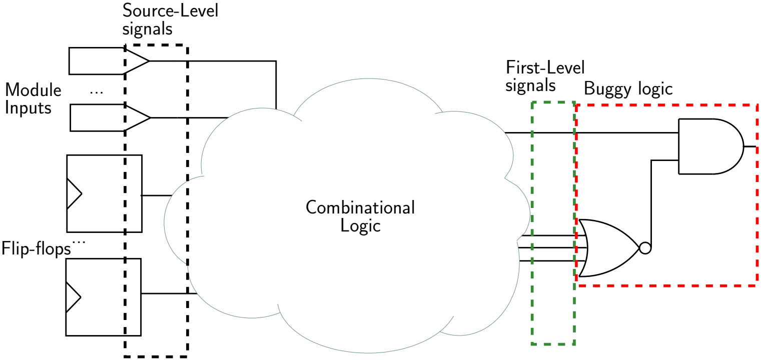
# Example logic design bug

Buggy code:

```
assign buggy_signal = foo & ~(rst | hw_int | sr_int);
```

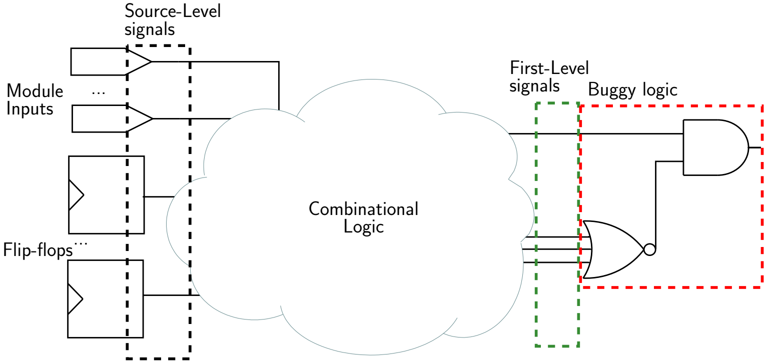
Correct code:

```
assign buggy_signal = foo & ~(rst | sr_int);
```



# What do we learn from this example?

- Semantically, bug occurs on specific combinations of **First-Level Signals**



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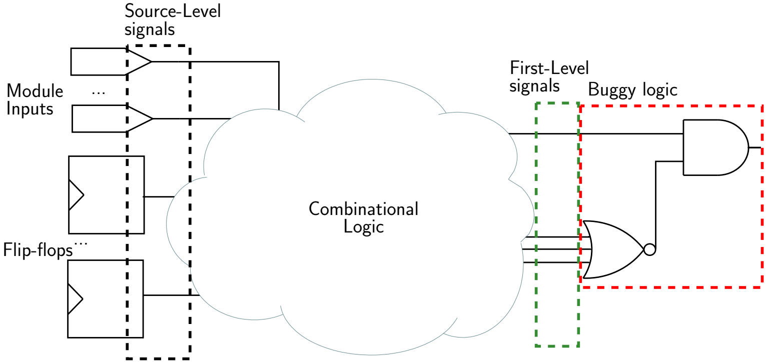
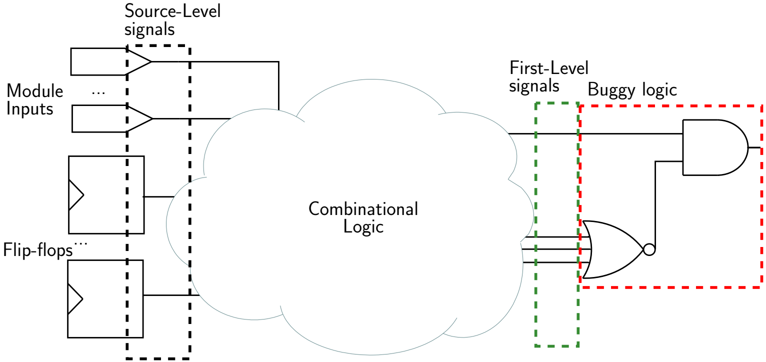


# What do we learn from this example?

- Semantically, bug occurs on specific combinations of **First-Level Signals**
- These **might not exist** in finished CPU
- But because we are at RTL-level it suffices to monitor the **Source-Level signals** corresponding to the First-Level Signals



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- On average 9 of those are not shared with any other bug
- In total, **1118 signals** to be monitored for detection of all 162 (documented) logic design bugs
- This is bad news!
- None of the logic design bugs in T1 had source signals from data or bus registers, **only control signal registers**

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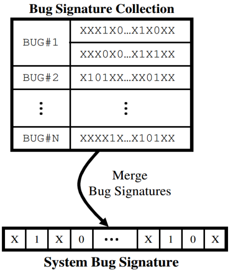
- *Bug Signatures* express what values **Source-Level signals** need to have for the bug to occur (0,1, X - don't care)
- Bug Signatures for all bugs combined into **single** *System Bug Signature*



**Bug Signature Collection**

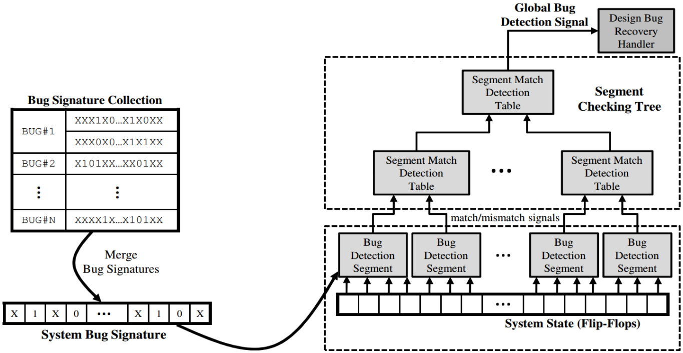
| | |
|---|---|
| BUG#1 | XXX1X0...X1X0XX |
| | XXX0X0...X1X1XX |
| BUG#2 | X101XX...XX01XX |
| ⋮ | ⋮ |
| BUG#N | XXXX1X...X101XX |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| X | 1 | X | 0 | ••• | X | 1 | 0 | X |

**System Bug Signature**

# Basic idea - Segments

- *Bug Detection Segments* monitor signals (**flip-flops**) they are responsible for



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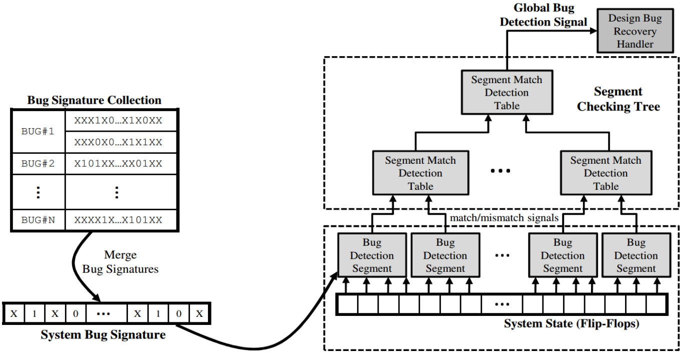

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Merge Bug Signatures

| X | 1 | X | 0 | ... | X | 1 | 0 | X |
|---|---|---|---|---|---|---|---|---|

System Bug Signature

Global Bug Detection Signal

Design Bug Recovery Handler

Segment Match Detection Table

Segment Checking Tree

Segment Match Detection Table

...

Segment Match Detection Table

match/mismatch signals

Bug Detection Segment

Bug Detection Segment

...

Bug Detection Segment

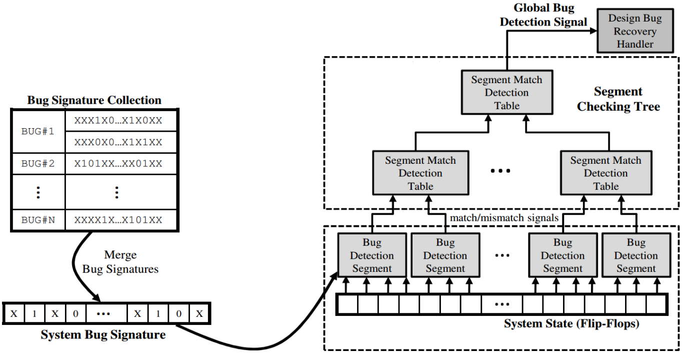
Bug Detection Segment

...

System State (Flip-Flops)

# Basic idea - Segments

- *Bug Detection Segments* monitor signals (**flip-flops**) they are responsible for
- each of those outputs whether all its signals match System Bug Signature
- *Bug Detection Segment* match results are combined using *Segment Match Detection Tables* into a *Segment Checking Tree* to generate Global Bug Detection Signal



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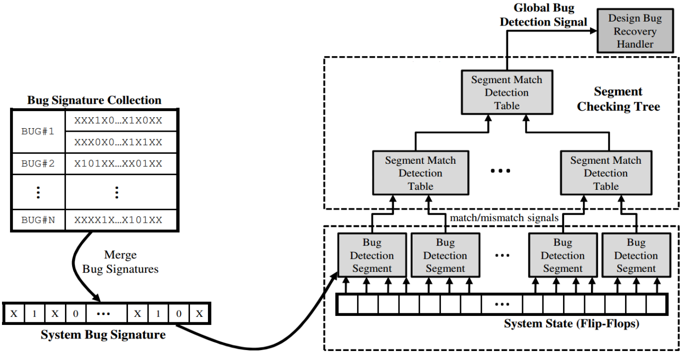

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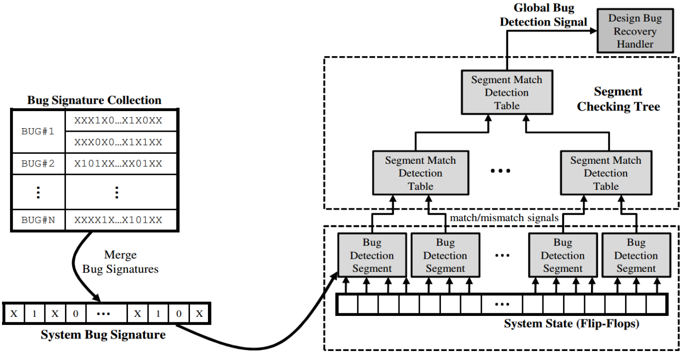
- Firmware updates can then initialize these



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  - This is essentially **demultiplexing** the System Bug Signature
- Tree structure is needed to **reduce number of false positives**, while reducing space used on storing Bug Signatures

# Signature merging example

| | | | |
|---|---|---|---|
| X | 1 | 0 | 0 |
| X | 1 | 0 | 1 |

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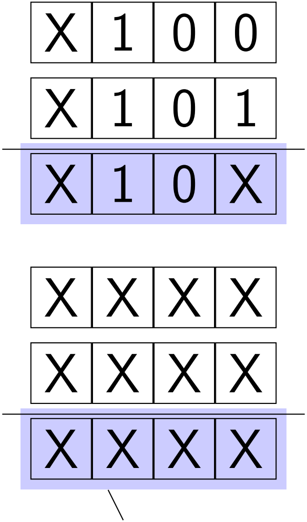

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this segment will be ignored in a node of the checking tree

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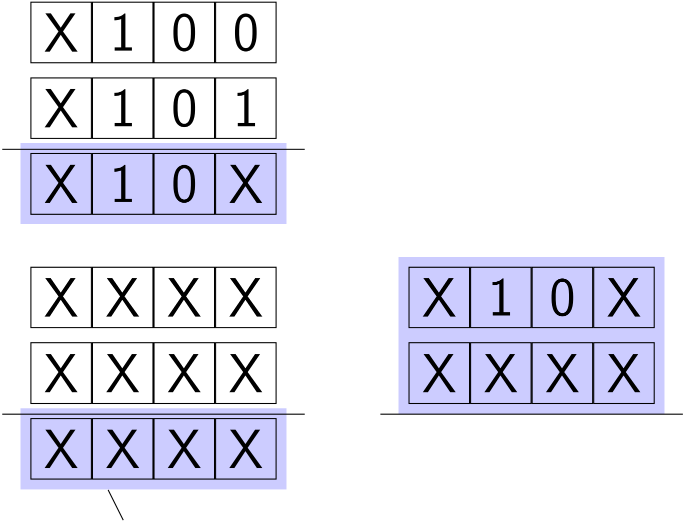

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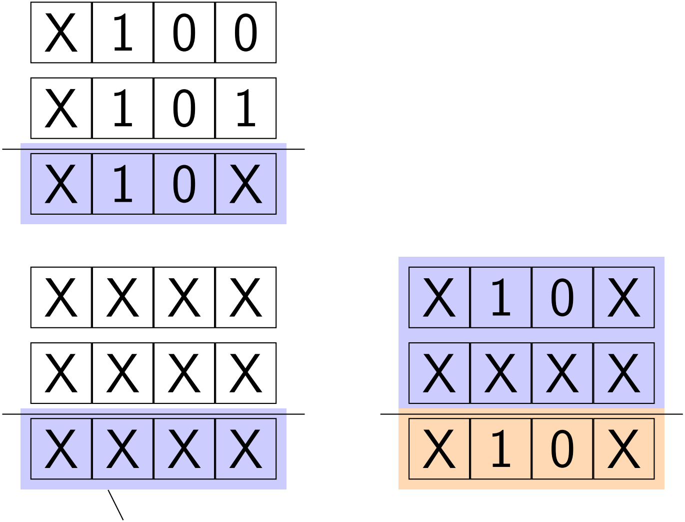

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- System Bug Signature translates into **two signals per flip-flop**: 0/1 and care/don't care(X)
- Bug Detection logic in Flip-flops outputs 0 for a signature match, and 1 for a mismatch
- All flip-flops in one Bug Detection Segment have their local bug detection signals chained together with OR-gates

→ Only if **all** flip-flop's values **match** signature, Bug Detection Segment **sends match** signal up the Segment Checking Tree

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- Allows all flip-flops of the processor to be connected in a Scan chain (like a large shift register) and to be tested using ATPG
- Used once after fabrication, after that scan logic is inactive
- Use **scan logic to load one bit** of System Bug Signature to flip-flops, use additional logic to store the other bit

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- Paper proposes mechanism to tweak false positive rate

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  - Then chain nodes together in a way that we match a temporal pattern
  - But this would mean getting rid of the 'levels' of the Segment Checking tree
  - Also detection of non-Timing Bugs would be delayed by a number of cycles (bad considering a bug could lock up the CPU in the meantime)

Paper Summary

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# Fixing design parameters

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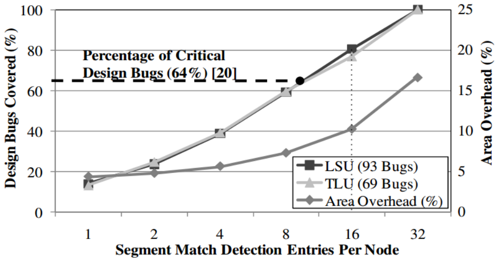

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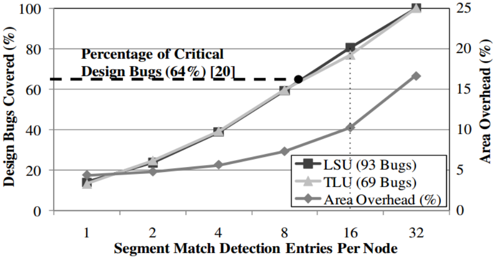

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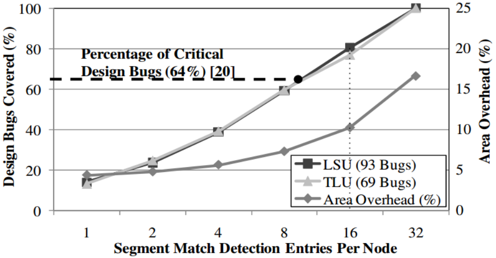

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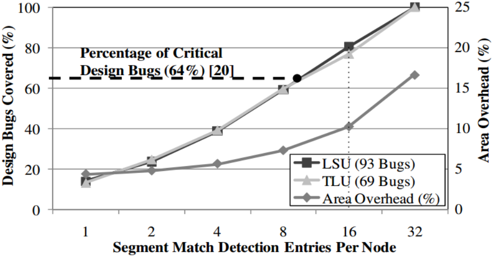

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- Non-critical = errors in performance measurement, error reporting, debugging etc.

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- Design with Online Bug detection - 58.3 W, **3.5% increase**
- **Amortized overhead** when we add online **hardware defect detection** (ACE):
    - 15.15% area and 6.8% power

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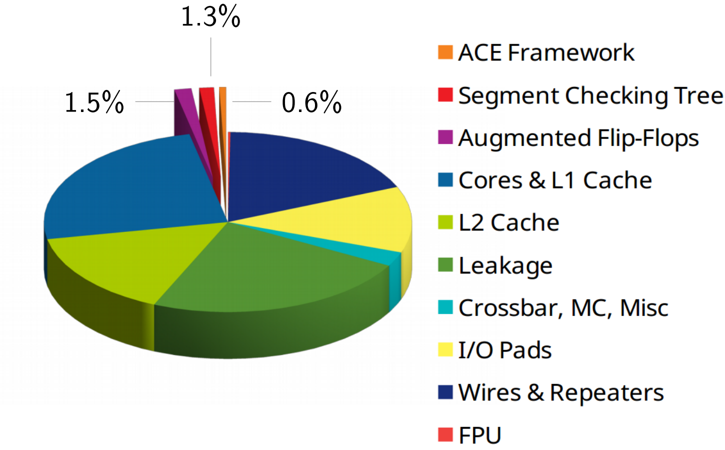

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# Executive Summary

- Problem:
  - **Increasing complexity** of modern CPUs makes **Design Bugs** in commercial products **more common**
  - They are hard to fix/avoid in software and usually unfixable in hardware
- Goal:
  - develop hardware solutions that enables **detecting** when a **Design Bug triggered**
  - has to be **flexible** to detect new bugs as they are discovered

# Executive Summary

- Contributions:
  - in-depth **study of design bugs** of a quasi-commercial CPU at a low level
  - novel mechanism to **monitor** internal CPU signals and deciding whether a Design Bug can be triggered
    - integrated into Flip-Flops, **reusing hardware** used in CPUs today, **field programmable**
    - **Variable amount** of detectable bugs (trade-off w/ area overhead), covering **all signals** of importance
    - Extensible to also do Hardware Fault Detection
  - Makes hardware "updatable" with bug patches like software
    - **Less pressure on verification**, can make development of new CPUs faster
- Evaluation:
  - To cover 80% of all bugs found in the study:
  - low power overhead **(3.5%)**
  - moderate area overhead **(10%)**
  - when combined with Hardware Fault Detection, some hardware can be shared and total overhead reduces

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- Estimated overhead based on assumption that 80% bug coverage is enough
  - Criticality of bugs in OpenSPARC T1 was not analyzed

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    - What about modern CPU **security vulnerabilities** (e.g. Spectre)?

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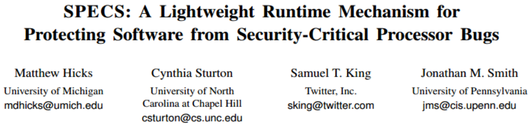
  - Can you apply tactics from algorithm verification? **Invariants** for algorithms in hardware?
  - Actually papers investigating this exist



**SPECS: A Lightweight Runtime Mechanism for Protecting Software from Security-Critical Processor Bugs**

Matthew Hicks
University of Michigan
mdhicks@umich.edu

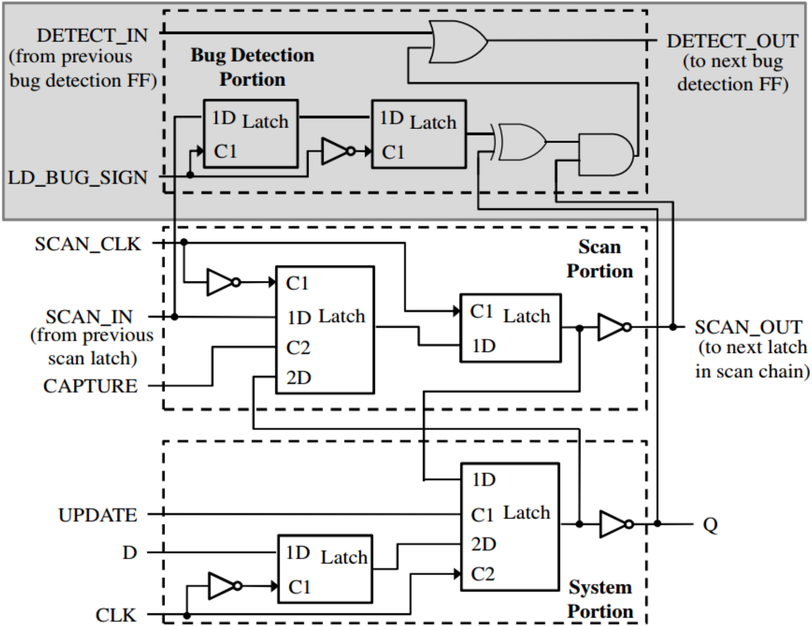
Cynthia Sturton
University of North Carolina at Chapel Hill
csturton@cs.unc.edu

Samuel T. King
Twitter, Inc.
sking@twitter.com

Jonathan M. Smith
University of Pennsylvania
jms@cis.upenn.edu

# End of presentation

# 0: Signature Match 1: Mismatch



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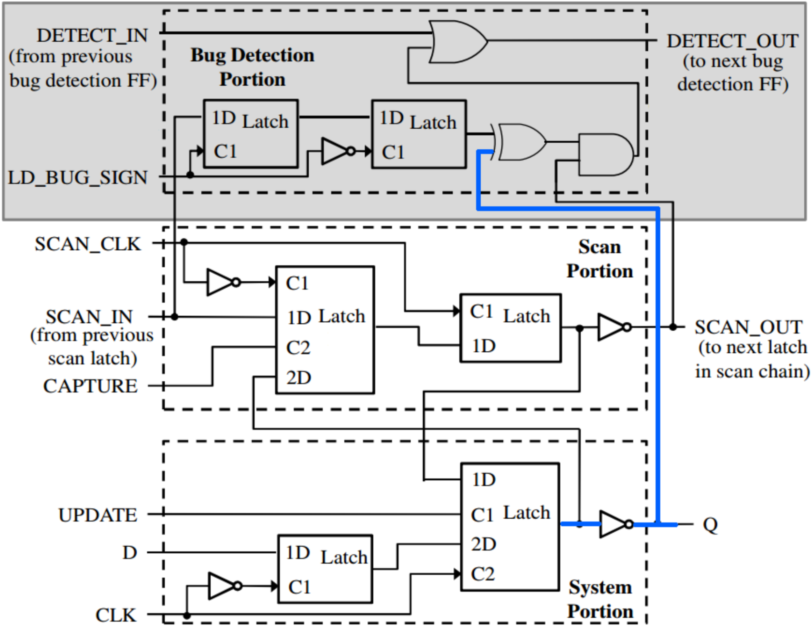

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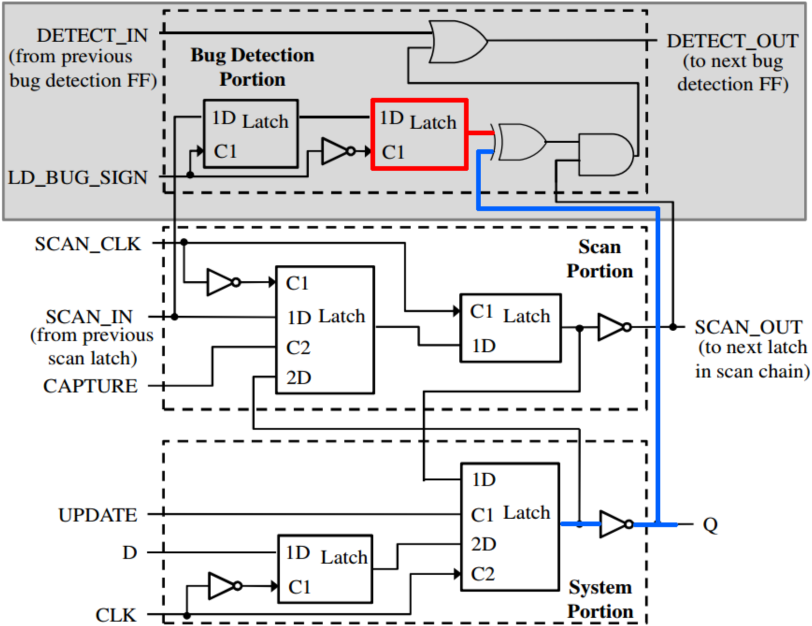

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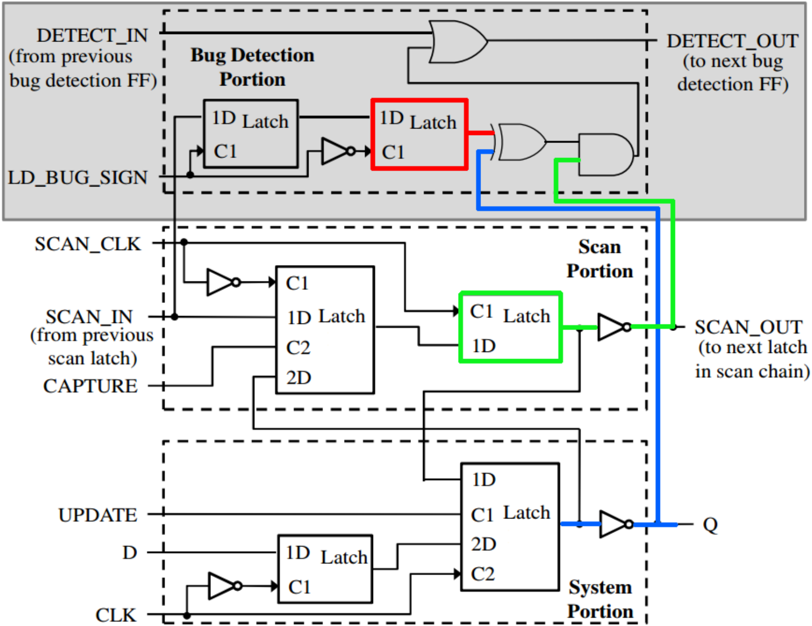

# Signature merging 2

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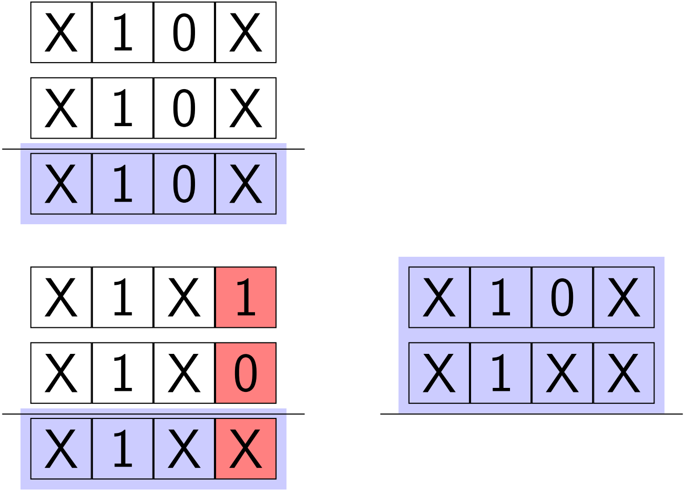

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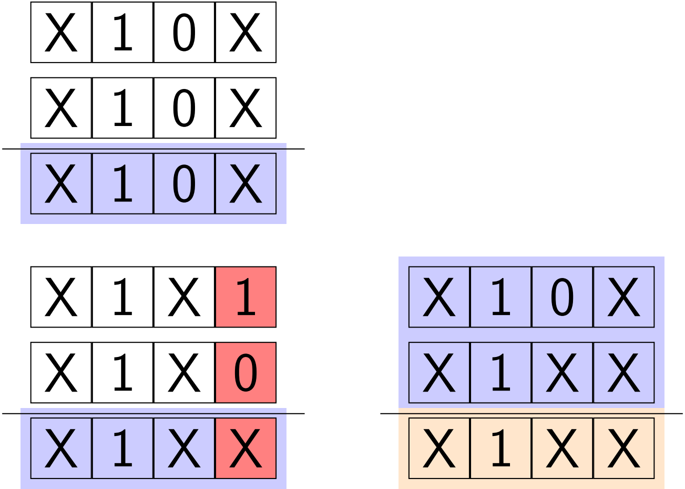

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