ComputeDRAM: In-Memory Compute Using Off-the-Shelf DRAMs

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Executive summary

- **Motivation**: Proof that AMBIT and RowClone are usable.
- **Goal**: Demonstrate row copy and bit-wise logical AND and OR in unmodified, commercial, DRAM.
- **Key Idea**: Violate DRAM timing constraints to enable charge sharing across multiple rows in the same sub-array.
- **Mechanism**: Perform operations with DRAM, by carefully violating its timing constraints.
- **Implementation**: Provide an in-memory compute framework to allow arbitrary computation.
- **Results**: Enable high computational throughput, up to 347x more energy efficient than using a vector unit.
Outline

1. Motivation
2. Solution Approaches
3. Recap on DRAM
4. Key Idea
5. Mechanism of ComputeDRAM
6. Operation Reliability
7. Implementation of ComputeDRAM
8. Methodology
9. Evaluation
10. Conclusion
Motivation

Google consumer workloads\cite{1}:

Data movement contributes to 62.7% of the total energy consumption.

\cite{1}: A. Boroumand et al. 2018. Google Workloads for Consumer Devices: Mitigating Data Movement Bottlenecks. In ASPLOS '18;
Motivation

Reduce memory bandwidth demand:

[1]: Illustration from Prof. Mutlu’s presentation on RowClone, pp 23.
# Solution Approach

Eliminating data movement by bringing computation closer to memory.

<table>
<thead>
<tr>
<th>Approach</th>
<th>Enabling Technologies</th>
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</thead>
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<tr>
<td>Processing-Near-Memory</td>
<td>Logic layers in 3D-stacked memory</td>
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<td>Silicon interposers</td>
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<td>Logic in memory controllers</td>
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<tr>
<td>Processing-Using-Memory</td>
<td>SRAM</td>
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<tr>
<td></td>
<td>DRAM</td>
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<tr>
<td></td>
<td>Phase-change memory (PCM)</td>
</tr>
<tr>
<td></td>
<td>Magnetic RAM (MRAM)</td>
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<td>Resistive RAM (RRAM)/memristors</td>
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</tbody>
</table>

Recap: DRAM Hierarchy

1. Channel
2. Rank
3. Chip
4. Bank
5. Sub-Array
6. Row/Colum
7. Cell
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Recap: DRAM Commands

- **Activate:**
  - On row level
  1. Open target row
Recap: DRAM Commands

- **Activate:**
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  1. Open target row
  2. Amplify bit-line charge
Recap: DRAM Commands

- **Activate:**
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- **Precharge:**
  - On bank level
  3. Close all rows
Recap: DRAM Commands

- **Activate:**
  - On row level
  1. Open target row
  2. Amplify bit-line charge

- **Precharge:**
  - On bank level
  3. Close all rows
  4. Drive bit-lines to $V_{dd}/2$
Motivation

RowClone: Intra-Subarray Copy

Data gets copied

Sense Amplifier (Row Buffer)

 Amplify the difference

\( V_{DD}/2 \quad \forall \delta \)

src 0 ←

dst 0 ←

\( V_{DD}/2 + \delta \)
Motivation

Triple-Row Activation: Majority Function

activate all three rows

enable sense amp

Sense Amp

Animation from: https://www.archive.ece.cmu.edu/~safari/pubs/ambit-bulk-bitwise-dram_micro17-talk.pptx
Key Idea

DRAM Operation Timing

• **Timing constraints** guarantee correctness

- $T_1$, Row Access Strobe $t_{RAS}$: time to open a row, enable sense amplifier, wait for voltage to reach $V_{dd}$ or $GND$
- $T_2$, Row Precharge $t_{RP}$: ensures that the previously activated row is closed, and the bit-line voltage has reached $V_{dd}/2$
Key Idea

DRAM Operation Timing

- Timing constraints guarantee correctness

Key Idea:

Violate timing constraints of $T1$ and $T2$ to perform operations.
Mechanism

Performing Row Copy

1. Issue **Activate** R1
Mechanism

Performing Row Copy

1. Issue **Activate** R1
2. Bit-line gets amplified
Mechanism

Performing Row Copy

1. Issue **Activate** R1
2. Bit-line gets amplified
3. Issue **Precharge**

![Diagram of row copy mechanism with steps labeled and timing indicated](image)
Mechanism

Performing Row Copy
1. Issue **Activate R1**
2. Bit-line gets amplified
3. Issue **Precharge**
4. 
   - R1 closed, driving $V_{dd}/2$
   - Interrupt **Precharge** with **Activate R2**
Mechanism

Performing Row Copy
1. Issue Activate R1
2. Bit-line gets amplified
3. Issue Precharge
4. 
   - R1 closed, driving $V_{dd}/2$
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5. Bit-line and cell of R2 get amplified
Mechanism

Performing Row Copy
1. Issue Activate R1
2. Bit-line gets amplified
3. Issue Precharge
4. 
   - R1 closed, driving $V_{dd}/2$
   - Interrupt Precharge with Activate R2
5. Bit-line and cell of R2 get amplified
6. R1 successfully copied to R
Mechanism

Performing Bulk-Bitwise logical AND/OR

By further reducing $T1$ and $T2$, three different rows can be opened simultaneously.

- The second Activate is sent while setting the word-line.
- The word-line according to the value on the row address bus is being driven.
- Intermediate row is being opened as well.
Mechanism

Performing Bulk-Bitwise logical AND/OR

- **Speculation:**
  - Row address is updated from LSB to MSB

- **Note:**
  - The row address update order is dependent on the manufacturer.
  - It will not work the same on every DRAM chip
Operation Reliability

Manufacturing Variations

- Capacitance variations require different timings

- Faulty cells due to manufacturing imperfections
  - Their row addresses are being remapped to another physical location
Implementation

As part of the **proof of concept**, computeDRAM introduces an in-memory compute framework.

**In-memory compute framework**
- Software interface to perform **arbitrary computation** using the three basic operations as building blocks.
- Manages the rows, where computations are being executed.
- Addresses the issue of errors due to faulty cells, by introducing an **error table**.
Performing arbitrary computation

- AND and OR are not logically complete on their own, the NOT operation is missing

- Workaround: Save negated values in pairwise fashion with their nominals.

\[
\begin{pmatrix}
A & \bar{A} \\
B & \bar{B} \\
C & \bar{C}
\end{pmatrix}
\]

- Overhead is quite substantial:
  - Generate the negated pair
  - Double the memory space needed
  - Twice the number of operations needed.
Implementation

Implementation choices

- Computations only performed in the first three rows.

- Operations require a setup:
  1. **Copy** the operands and the op-constant to these 3 rows
  2. **Perform** the computation
  3. **Copy** the result back to the destination row
Implementation

Challenge

– The library ensures that operand rows are in the same sub-array by checking their address.

– The addresses of remapped rows are not consistent with their physical locations.

– There is no way to guarantee that data is on the same sub-array, as the new row could be anywhere.
Implementation

Solution: Error Table

– Idea: **Exclude “bad” columns and rows** from computation with a custom mapping.

– Requires a scanning process to **discover “bad” parts** and save them to the error table.

– The error table requires **periodical re-scans**, due to natural wear out etc.
Methodology

• Host system + FPGA running SoftMC to control the DRAM module

• Limitations:
  – **Timing intervals** are limited to multiples of 2.5 ns
  – DDR3 chips only

Extensive tests on **environment temperature** have been made
Evaluation

Which manufacturers work?

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Micron_2G_1066</th>
<th>Micron_2G_1333</th>
<th>Elpida_2G_1333</th>
<th>Nanya_4G_1333</th>
<th>Corsair_4G_1333</th>
<th>TimeTec_4G_1333</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>0123456789</td>
<td>0123456789</td>
<td>0123456789</td>
<td>0123456789</td>
<td>0123456789</td>
<td>0123456789</td>
</tr>
<tr>
<td>T2</td>
<td>0123456789</td>
<td>0123456789</td>
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- **TimeTec_4G_1333**

**ETH zürich**
Evaluation

Computational Throughput
- Overhead does not change as we move from scalar to vector operations of 64k elements

Energy efficiency
- Eliminates the high energy overhead of transferring data between CPU and main memory.
- 347x more efficient than using a vector unit for row copy.
- 48x more efficient for 8-bit AND/OR
- 9.3x more efficient for 8-bit ADD
Conclusion

• **Motivation**: Proof that AMBIT and RowClone are usable.

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• **Results**: Enable high computational throughput, up to 347x more energy efficient than using a vector unit.
Strengths

• Working proof of concept
  – No additional hardware required
  – Accessible in form of a library
• Addresses an important problem
• Well written
Weaknesses

- Requirement for pairwise saving of negated values
- Not applicable to every DRAM chip
  - Getting the timings right is substantial
- Requires data to be in the same sub array
- No solution for inter subarray row copy
- Proof of concept
  - No thorough evaluation
Related Work

Low-Cost Inter-Linked Subarrays (LISA): Enabling Fast Inter-Subarray Data Movement in DRAM

Kevin K. Chang†, Prashant J. Nair*, Donghyuk Lee†, Saugata Ghose†, Moinuddin K. Qureshi*, and Onur Mutlu†

†Carnegie Mellon University    *Georgia Institute of Technology

AlignS: A Processing-In-Memory Accelerator for DNA Short Read Alignment Leveraging SOT-MRAM

Shaahin Angizi†, Jiao Sun‡, Wei Zhang‡ and Deliang Fan†

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Related Work

**Duality Cache for Data Parallel Acceleration**
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Reetuparna Das
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University of Michigan

**A Case for Exploiting Subarray-Level Parallelism (SALP) in DRAM**
Yoongu Kim
Vivek Seshadri
Donghyuk Lee
Jamie Liu
Onur Mutlu
Carnegie Mellon University

**DRISA: A DRAM-based Reconfigurable In-Situ Accelerator**
Shuangchen Li$^1$
Dimin Niu$^2$
Krishna T. Malladi$^2$
Hongzhong Zheng$^2$
Bob Brennan$^2$
Yuan Xie$^1$

$^1$University of California, Santa Barbara
$^2$Samsung Semiconductor Inc.
Related Work

DrAcc: a DRAM based Accelerator for Accurate CNN Inference

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Open Discussion

• Is ComputeDRAM practical for actual use?
  – What overhead is imposed?
  – Do you think the overhead is acceptable?
  – Are there any additional requirements to the system?

• What workloads can benefit from ComputeDRAM?

• Is there a way to enable more general computation?
  – E.g. multiplication, division, floating point arithmetic…
  – Where are the limits in complexity?
Open Discussion

• Will the solution become more important over time?

• What alternatives do you see?
Thank you for your attention!