Self-Optimizing Memory Controllers: A Reinforcement Learning Approach

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Executive Summary

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Problem, Background and Goal

DRAM bandwidth is the bottleneck

Goal: Efficiently utilize DRAM bandwidth

The Memory Controller

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Must obey many local and global DRAM timing constraints

[0]Onur Mutlu and Thomas Moscibroda, "Parallelism-Aware Batch Scheduling: Enabling High-Performance and Fair Memory Controllers" IEEE Micro, 2009

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Can't anticipate the long term effects of its scheduling decisions

Can't take lessons from the consequences of its past actions to decide better in the future

Novelty, Key Approach & Ideas

Key Idea: Enable the Memory Controller to Learn From Its Actions

Bene ts

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Allows the hardware designer to focus on what speci c goal the MC should accomplish

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More ef ciently utilize DRAM bandwidth (21% more utilization over FR-FCFS)

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- Enables the MC to adapt to workload changes
- Hopefully enables the MC to make farsighted decisions
- Creates an MC which can use its experience in new, but similar situations
- More ef ciently utilize DRAM bandwidth (21% more utilization over FR-FCFS)
- Improved system performance (19% performance improvement over FR-FCFS)

Mechanisms

Reinforcement Learning

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Formulate memory access scheduling as an in nite horizon (continuous) task

Scheduler always has 1 DRAM clock cycle to decide what it wants to do

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Reward = 1 if a read/write command was issued. Otherwise, Reward = 0

Reward function

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At every time step, the scheduler will make the decision it thinks will maximize the reward function, which is de ned as [1]

[1] R. Sutton and A. Barto. Reinforcement Learning. MIT Press, Cambridge, MA, 1998.

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Note that we also have

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All attributes available in the controller's transaction queue ! fast access

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- Update the Q-value of the previous command

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Q_{prev} (1)Q_{prev} + (r + $Q_{selected}$)

Note: Correct operation is ensured by adding a set of extra constraints

How to store all the Q-values ef ciently

Figure: Fine-grain

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Figure: Coarse-grain

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Figure: CMAC

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Assumption: Scheduler's pipe can be clocked 10 times each DRAM cycle

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Scheduler can consider 12 commands every cycle

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A constant number per action type !
prevent generalization across different commands

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random shifts of attributes implement the shiftedness of CMAC arrays

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2. logic to update Q-values ! single pipelined 16-bit xed-point multiplier
3. storing the Q-values ! 32 kB on-chip storage

Key Results: Methodology & Evaluation

Methodology

Some important parameters of the simulated CMP:

- Frequency: 4 GHz
- #Cores: 4 (each 2-way simultaneously multithreaded)
- iL1/dL1 size: 32 kB
- Shared L2 cache: 4MB, 8-way

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Some important parameters of the simulated DRAM:

- DDR2-800 SDRAM
- Transaction Queue: 64 entries
- Peak Data Rate: 6.4 GB/s
- DRAM Bus Frequency: 400 MHz
- Single rank with 4 DRAM chips
- #Banks: 4 per DRAM chip
- Row Buffer Size: 2 KB

Applications & Benchmarks

Compared Memory Controllers

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A conventional in-order MC

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MC implementing FR-FCFS

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An ideal scheduler with an ideal memory that can sustain 100% peak bandwidth

Results: Data Bus Utilization

Results: Performance Improvement

Results: Scaled to More Cores

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Strengths & Weaknesses

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Well-written paper

Weaknesses

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More complicated hardware than FR-FCFS

Extending it is hard since hardware will get even more complicated

Heterogeneous workloads are not tested

Can we do better?

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Can we solve the fairness problem?

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Can we solve the fairness problem?

- "ATLAS" [Y. Kim, D. Han, O. Mutlu and M. Harchol-Balter, HPCA 2010]

Periodically order threads based on the service they have attained from the memory controllers so far

Periodically order threads based on the service they have attained from the memory controllers so far

Prioritize the threads that have attained the least service over others in each period

Can we do better?

Can we solve the fairness problem?

- "ATLAS" [Y. Kim, D. Han, O. Mutlu and M. Harchol-Balter, HPCA 2010]
- TCM scheduling [Y. Kim, M. Papamichael, O. Mutlu, M. Harchol-Balter, MICRO 2010]

Dynamically group threads into a latency-sensitive cluster and a bandwidth-sensitive cluster

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Prioritize 1st cluster over 2nd cluster

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Employ different policies within each cluster

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- TCM scheduling [Y. Kim, M. Papamichael, O. Mutlu, M. Harchol-Balter, MICRO 2010]
- "BLISS" [L. Subramanian, D. Lee, V. Seshadri, H. Rastogi, O. Mutlu, IEEE Transactions on Parallel and Distributed Systems 2016]

Mark each application either as vulnerable-to-interference or as interference-causing.

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Prioritize requests from 1st group over requests from 2nd group

Key Takeaways

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Seemingly hard to improve

Open Discussion

Discussion

How can we solve the fairness problem while keeping our RL-based approach?

Discussion

Are there other flaws in this approach?

Discussion

Can this approach be used to solve other scheduling problems?

Discussion

When are machine-learning based approaches applicable in computer architecture?

Backup slides

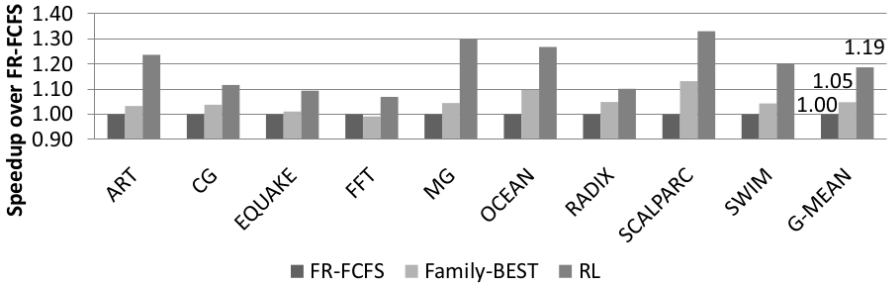
Ensuring correct operation

the scheduler is not permitted to select NOPs when other legal commands are available

the scheduler is only allowed to activate rows due to pending requests in the transaction queue (i.e., the scheduler cannot choose to activate an arbitrary row with no pending requests)

the scheduler is not allowed to precharge a newly activated row until it issues a reador write command to it.

Results: RL versus Family-BEST



Results: RL versus Family-BEST

Preference relations used in Family-BEST:

- Row commands over column commands
- Older commands over younger commands
- Reads over writes
- Load misses over store misses
- More critical load misses over less critical ones, based on sequence numbers

Results: Online versus Offline