Example Paper Presentation
We Will Briefly Review This Paper

Application-Aware Memory Channel Partitioning

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Today’s presenter: Minesh Patel

SAFARI  Carnegie Mellon
Background, Problem & Goal
Main Memory is a Bottleneck

- Main memory latency is long
- Core stalls, performance degrades
- Multiple applications share the main memory
Problem of Inter-Application Interference

- Applications’ requests interfere at the main memory
- This *inter-application interference* degrades system performance
- Problem further exacerbated due to
  - Increasing number of cores
  - Limited off-chip pin bandwidth
Goal:
Mitigate Inter-Application Interference

Previous Approach:
Application-Aware Memory Request Scheduling

Our First Approach:
Application-Aware Memory Channel Partitioning

Our Second Approach:
Integrated Memory Partitioning and Scheduling
Background: Main Memory

- **FR-FCFS memory scheduling policy** [Zuravleff et al., US Patent ’97; Rixner et al., ISCA ’00]
  - Row-buffer hit first
  - Oldest request first
- **Unaware of inter-application interference**
Novelty
Previous Approach

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**Application-Aware Memory Request Scheduling**

- **Monitor** application memory access characteristics

- **Rank** applications based on memory access characteristics

- **Prioritize** requests at the memory controller, based on ranking
An Example: Thread Cluster Memory Scheduling

Memory-non-intensive

Threads in the system

Memory-intensive

Non-intensive cluster

Prioritized

Intensive cluster

Throughput

Fairness

higher priority

higher priority

Figure: Kim et al., MICRO 2010
Advantages

- Reduces interference between applications by request reordering
- Improves system performance

Disadvantages

- Requires modifications to memory scheduling logic for
  - Ranking
  - Prioritization
- Cannot completely eliminate interference by request reordering
Key Approach and Ideas
The Paper’s Approach

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Observation: Modern Systems Have Multiple Channels

A new degree of freedom
Mapping data across multiple channels
Data Mapping in Current Systems

Causes interference between applications’ requests
Partitioning Channels Between Applications

Eliminates interference between applications’ requests
Overview: Memory Channel Partitioning (MCP)

- **Goal**
  - Eliminate harmful interference between applications

- **Basic Idea**
  - Map the data of *badly-interfering applications* to different channels

- **Key Principles**
  - Separate *low and high memory-intensity applications*
  - Separate *low and high row-buffer locality applications*
Key Insight 1: Separate by Memory Intensity

High memory-intensity applications interfere with low memory-intensity applications in shared memory channels. Map data of low and high memory-intensity applications to different channels.
Key Insight 2: Separate by Row-Buffer Locality

High row-buffer locality applications interfere with low row-buffer locality applications in shared memory channels.

Conventional Page Mapping

Channel 0
Bank 0
Bank 1

Channel 1
Bank 0
Bank 1

Request Buffer State

Map data of low and high row-buffer locality applications to different channels.
Mechanisms (in some detail)
Memory Channel Partitioning (MCP) Mechanism

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<td><strong>5. Allocate application pages</strong></td>
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Hardware

System

Software
1. Profile Applications

- Hardware counters collect application memory access characteristics

- Memory access characteristics
  - Memory intensity:
    - Last level cache Misses Per Kilo Instruction (MPKI)
  - Row-buffer locality:
    - Row-buffer Hit Rate (RBH) - percentage of accesses that hit in the row buffer
2. Classify Applications

- **Test MPKI**
  - Low
  - High
    - Low Intensity
    - High Intensity
      - **Test RBH**
        - Low
        - High
          - High Intensity Low Row-Buffer Locality
          - High Intensity High Row-Buffer Locality
3. Partition Channels Among Groups: Step 1

Assign number of channels proportional to number of applications in group.

Low Intensity

High Intensity
Low Row-Buffer Locality

High Intensity
High Row-Buffer Locality

Channel 1
Channel 2
Channel 3
...
Channel N-1
Channel N
3. Partition Channels Among Groups: Step 2

Assign number of channels proportional to bandwidth demand of group.
4. Assign Preferred Channel to Application

- Assign each application a preferred channel from its group’s allocated channels.
- Distribute applications to channels such that group’s bandwidth demand is balanced across its channels.
5. Allocate Page to Preferred Channel

- Enforce channel preferences computed in the previous step

- On a page fault, the operating system
  - allocates page to preferred channel if free page available in preferred channel
  - if free page not available, replacement policy tries to allocate page to preferred channel
  - if it fails, allocate page to another channel
Interval Based Operation

1. Profile applications
2. Classify applications into groups
3. Partition channels between groups
4. Assign preferred channel to applications
5. Enforce channel preferences
Integrating Partitioning and Scheduling

**Goal:**
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Observations

- Applications with very low memory-intensity rarely access memory
  → Dedicating channels to them results in precious memory bandwidth waste

- They have the most potential to keep their cores busy
  → We would really like to prioritize them

- They interfere minimally with other applications
  → Prioritizing them does not hurt others
Always prioritize very low memory-intensity applications in the memory scheduler

Use memory channel partitioning to mitigate interference between other applications
Key Results:
Methodology and Evaluation
Hardware Cost

- **Memory Channel Partitioning (MCP)**
  - Only profiling counters in hardware
  - No modifications to memory scheduling logic
  - 1.5 KB storage cost for a 24-core, 4-channel system

- **Integrated Memory Partitioning and Scheduling (IMPS)**
  - A single bit per request
  - Scheduler prioritizes based on this single bit
Methodology

- **Simulation Model**
  - 24 cores, 4 channels, 4 banks/channel
  - Core Model
    - Out-of-order, 128-entry instruction window
    - 512 KB L2 cache/core
  - Memory Model – DDR2

- **Workloads**
  - 240 SPEC CPU 2006 multiprogrammed workloads (categorized based on memory intensity)

- **Metrics**
  - **System Performance**
    \[
    Weighted\ Speedup = \sum_i \frac{IPC_i^{\text{shared}}}{IPC_i^{\text{alone}}}
    \]
Previous Work on Memory Scheduling

- **FR-FCFS** [Zuravleff et al., US Patent 1997, Rixner et al., ISCA 2000]
  - Prioritizes row-buffer hits and older requests
  - Application-unaware

- **ATLAS** [Kim et al., HPCA 2010]
  - Prioritizes applications with low memory-intensity

- **TCM** [Kim et al., MICRO 2010]
  - Always prioritizes low memory-intensity applications
  - Shuffles request priorities of high memory-intensity applications
Comparison to Previous Scheduling Policies

Significant performance improvement over baseline FRFCFS at lower hardware cost

Better system performance than the best previous scheduler

Averaged over 240 workloads
IMPS improves performance regardless of scheduling policy. Highest improvement over FRFCFS as IMPS designed for FRFCFS.
Summary
Summary

- Uncontrolled inter-application interference in main memory degrades system performance

- **Application-aware memory channel partitioning (MCP)**
  - Separates the data of badly-interfering applications to different channels, eliminating interference

- **Integrated memory partitioning and scheduling (IMPS)**
  - Prioritizes very low memory-intensity applications in scheduler
  - Handles other applications’ interference by partitioning

- MCP/IMPS provide better performance than application-aware memory request scheduling at lower hardware cost
Strengths
Strengths (1/2)

- Novel solution to a key problem in multi-core systems
  - Memory interference
  - The importance of problem will increase over time

- Keeps the memory scheduling hardware simple

- Enables HW and SW components to work cooperatively where each works best

- Combines multiple interference reduction techniques
Strengths (2/2)

- Can provide performance isolation across applications mapped to different channels

- General idea of partitioning can be extended to smaller granularities in the memory hierarchy: banks, subarrays, etc.

- Well-written paper

- Thorough simulation-based evaluation
Weaknesses
Weaknesses

- Overhead of moving pages between channels restricts mechanism’s benefits

- Load imbalance across channels can reduce performance
  - The paper addresses this and compares to another mechanism

- Software-hardware cooperative solution might not always be easy to adopt

- Evaluation is done solely in simulation

- Evaluation does not consider multi-chip systems

- Are these the best workloads to evaluate?
Recall: Try to Avoid Rat Holes

Performance Analysis Rat Holes

Benchmark

Performance Criteria

Configuration

Specific Details

Limitations of the Mechanism

- Mechanism may not work effectively if workload changes behavior after profiling.
- Small number of memory channels reduces the scope of partitioning.
- Adds restrictions on physical-to-DRAM address mapping.
Thoughts and Ideas
Extensions

- Can this idea be extended to different granularities in memory?
  - Partition banks, subarrays, mats across workloads

- Can this idea be extended to provide performance predictability and performance isolation? How?

- How can MCP be combined effectively with other interference reduction techniques?
  - E.g., source throttling methods [Ebrahimi+, ASPLOS 2010]
  - E.g., thread scheduling methods

- Can this idea be evaluated on a real system? How?
Fairness via Source Throttling

Eiman Ebrahimi, Chang Joo Lee, Onur Mutlu, Yale N. Patt,
"Fairness via Source Throttling: A Configurable and High-Performance Fairness Substrate for Multi-Core Memory Systems"


Fairness via Source Throttling: A Configurable and High-Performance Fairness Substrate for Multi-Core Memory Systems

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Bank Partitioning

Liu Liu, Zehan Cui, Mingjie Xing, Yungang Bao, Mingyu Chen, Chengyong Wu,

A Software Memory Partition Approach for Eliminating Bank-level Interference in Multicore Systems

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Bank Partitioning

- Min Kyu Jeong, Doe Hyun Yoon, Dam Sunwoo, Mike Sullivan, Ikhwan Lee, Mattan Erez,


Balancing DRAM Locality and Parallelism in Shared Memory CMP Systems

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‡ ARM Inc.
Takeaways
Key Takeaways

- A novel method to reduce memory interference
- Simple and effective
- Hardware/software cooperative

- Good potential for work building on it to extend it
  - To different structures
  - To different metrics
  - Multiple works have already built on the paper (see bank partitioning works in PACT 2012, HPCA 2012)

- Easy to read and understand paper
Open Discussion
Discussion Starters

- Thoughts on the previous ideas?
- How practical is this?
- Will the problem become bigger and more important over time?
- Will the solution become more important over time?
- Are other solutions better?
- Is this solution clearly advantageous in some cases?