Self-Optimizing Memory Controllers: A Reinforcement Learning Approach

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Executive Summary

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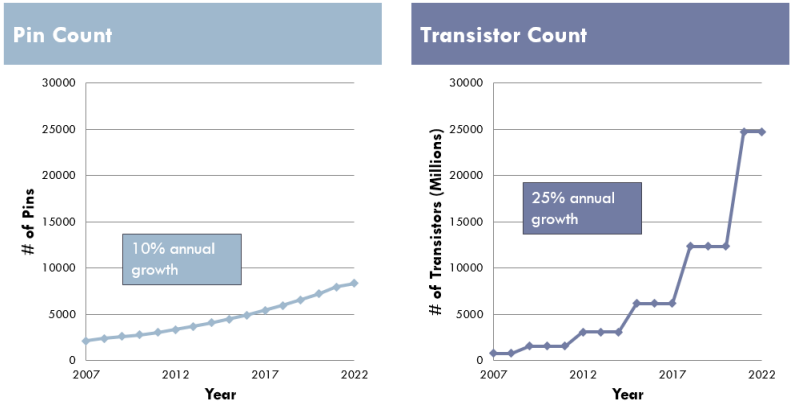
- Scales as well as the best static policy

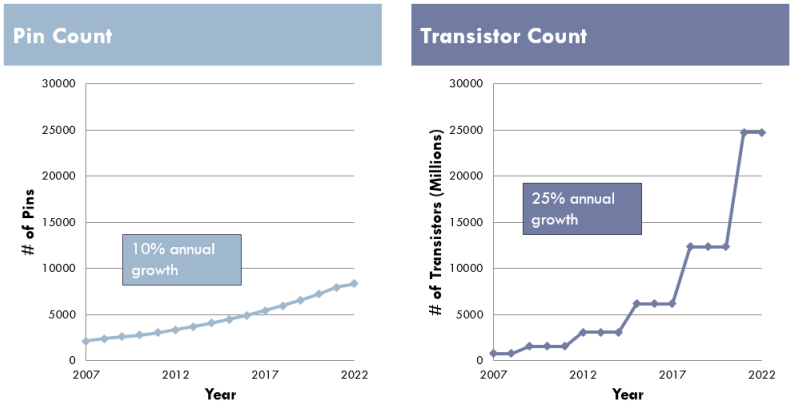
Problem, Background and Goal

DRAM bandwidth is the bottleneck



ITRS 2007 Executive Summary

Goal: Efficiently utilize DRAM bandwidth



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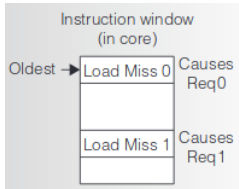

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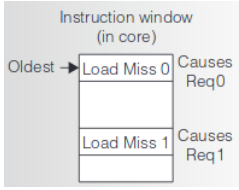

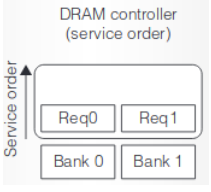

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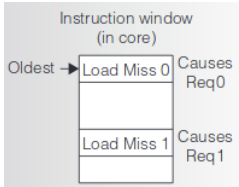

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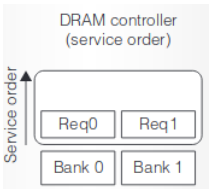

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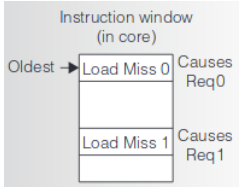

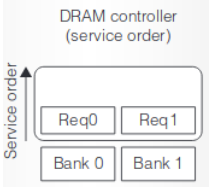

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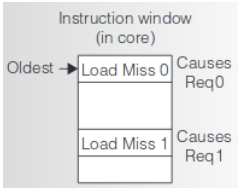

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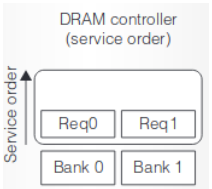
- Must obey many local and global DRAM timing constraints



[0]Onur Mutlu and Thomas Moscibroda, "Parallelism-Aware Batch Scheduling: Enabling High-Performance and Fair Memory Controllers" IEEE Micro, 2009

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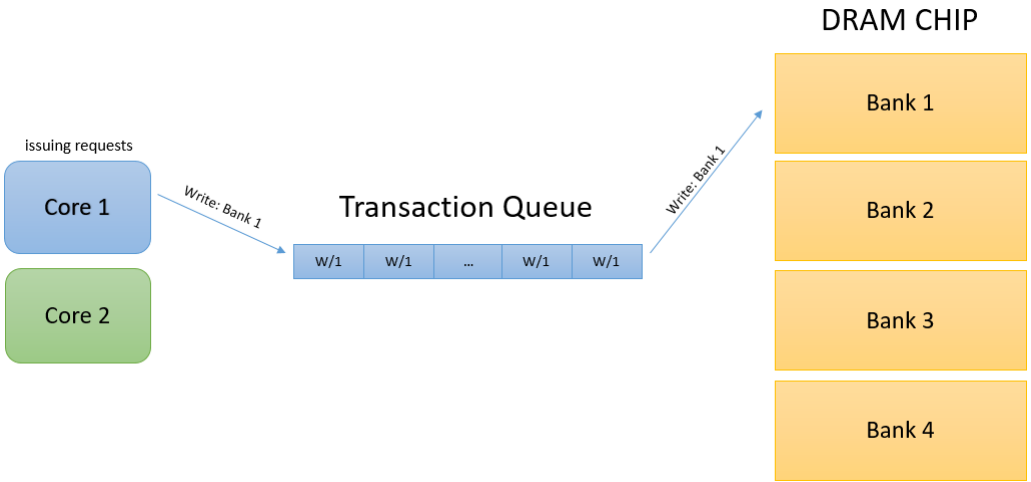
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Bank 1
Bank 2
Bank 3
Bank 4
issuing requests
Core 1
Core 2
Write: Bank 1
Transaction Queue
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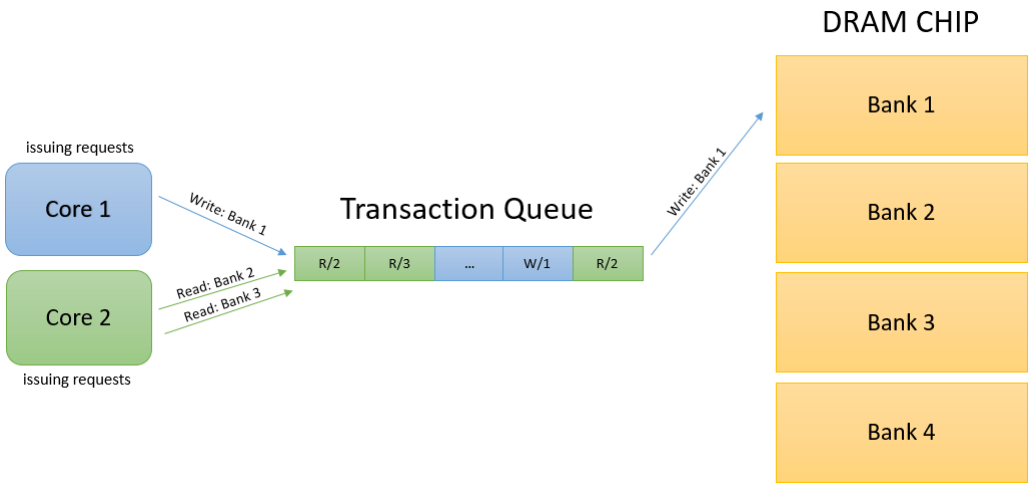
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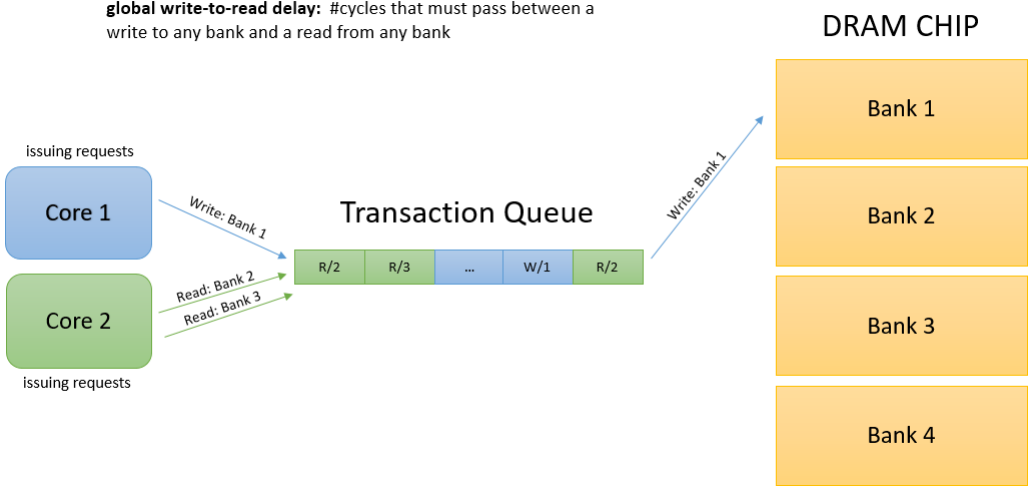

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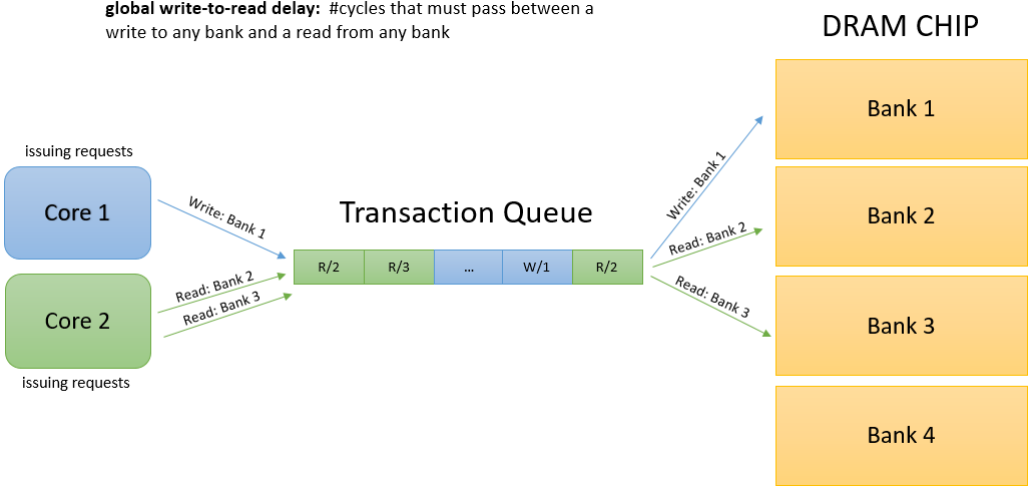

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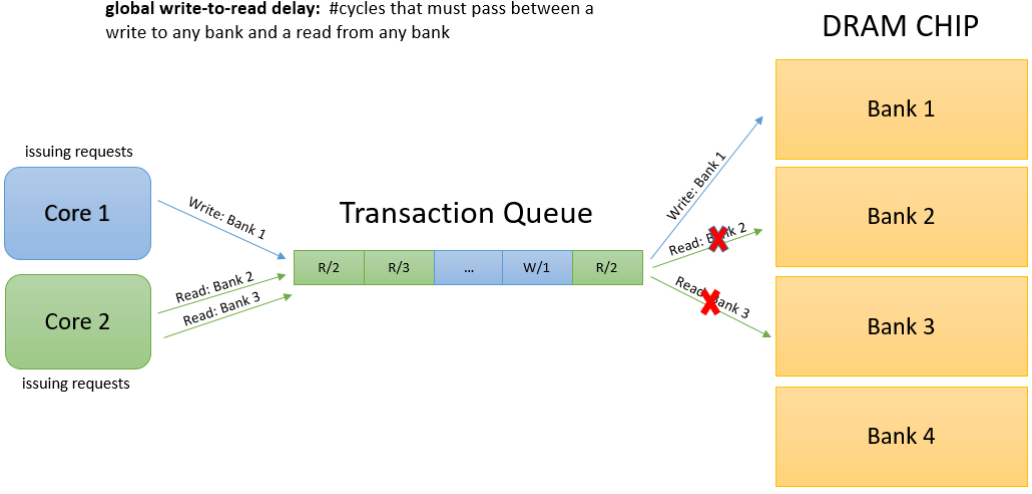

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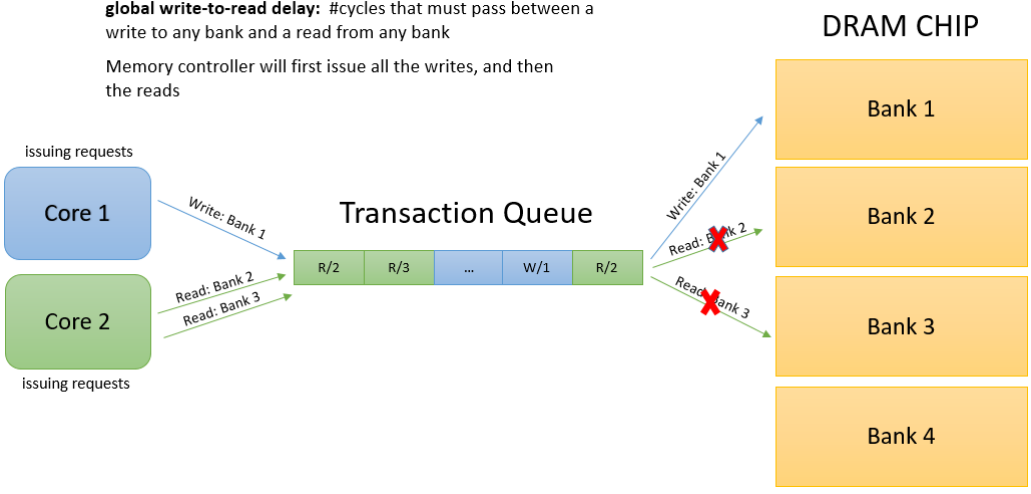

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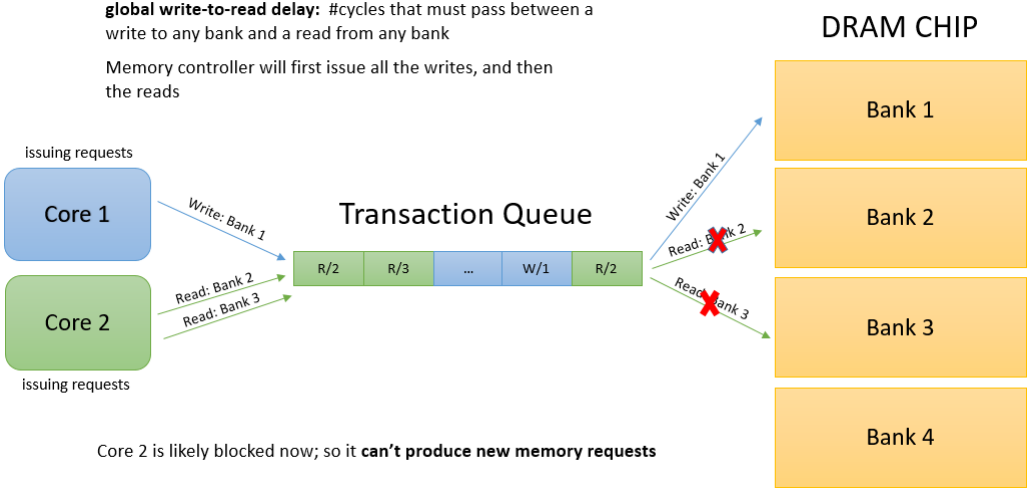

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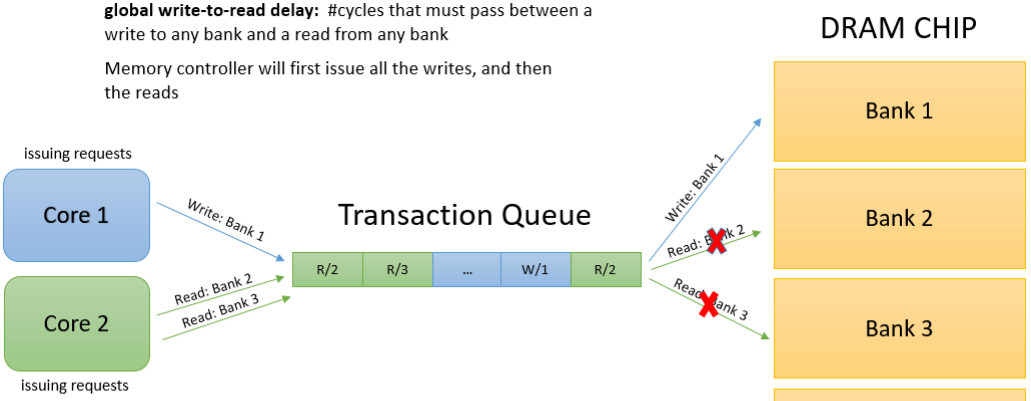

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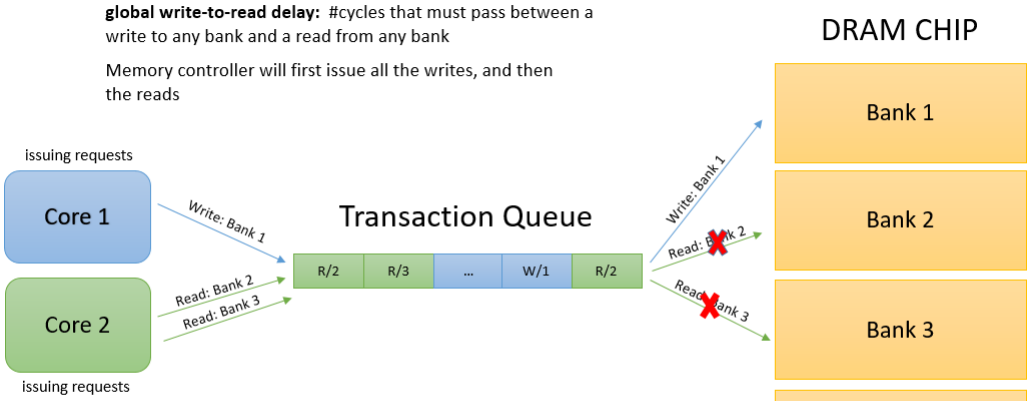

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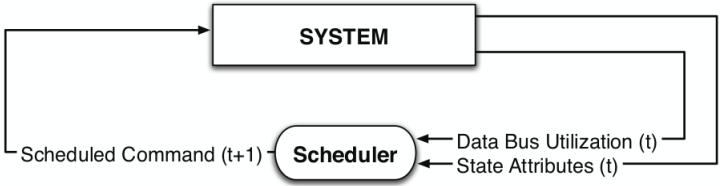
A static policy **will repeat its mistake** in every similar situation

Novelty, Key Approach & Ideas

Key Idea: Enable the Memory Controller to **Learn** From Its Actions



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- **More efficiently utilize DRAM bandwidth (21% more utilization over FR-FCFS)**
- **Improved system performance (19% performance improvement over FR-FCFS)**

Mechanisms

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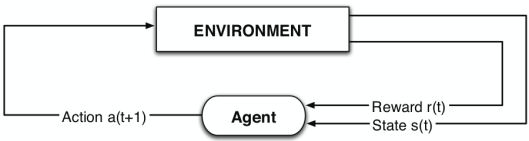

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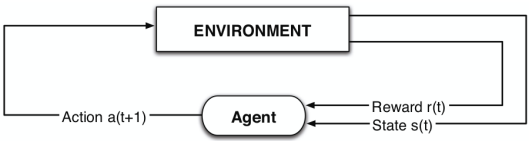

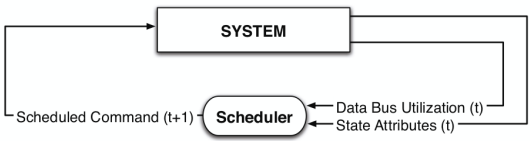

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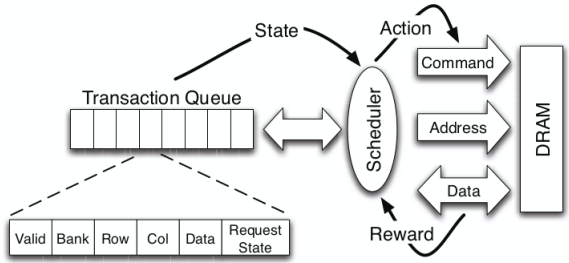

Figure 4: High-level overview of an RL-based scheduler.

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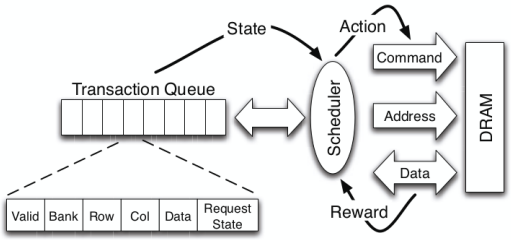

Figure 4: High-level overview of an RL-based scheduler.

Reward = 1 if a read/write command was issued. Otherwise, Reward = 0

Reward function

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At every time step, the scheduler will make the decision it thinks will maximize the reward function, which is defined as[1]

$$G_t \doteq R_{t+1} + \gamma R_{t+2} + \gamma^2 R_{t+3} + \cdots = \sum_{k=0}^{\infty} \gamma^k R_{t+k+1}$$

[1] R. Sutton and A. Barto. Reinforcement Learning. MIT Press, Cambridge, MA, 1998.

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Note that we also have

$$\begin{aligned} G_t &\doteq R_{t+1} + \gamma R_{t+2} + \gamma^2 R_{t+3} + \gamma^3 R_{t+4} + \cdots \\ &= R_{t+1} + \gamma \big(R_{t+2} + \gamma R_{t+3} + \gamma^2 R_{t+4} + \cdots \big) \\ &= R_{t+1} + \gamma G_{t+1} \end{aligned}$$

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$$q_\pi(s,a) \doteq \mathbb{E}_\pi[G_t \mid S_t = s, A_t = a] = \mathbb{E}_\pi\left[\sum_{k=0}^{\infty} \gamma^k R_{t+k+1} \,\middle|\, S_t = s, A_t = a\right]$$

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All attributes available in the controller's transaction queue $\rightarrow$ fast access

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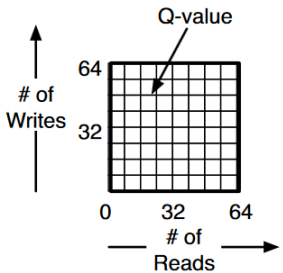
- $Q_{prev} \leftarrow (1 - \alpha)Q_{prev} + \alpha(r + \gamma Q_{selected})$

Note: Correct operation is ensured by adding a set of extra constraints

How to store all the Q-values efficiently



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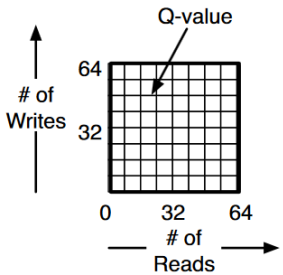

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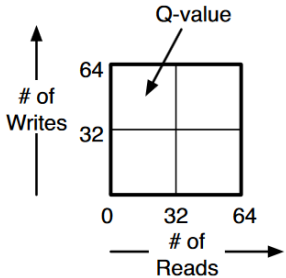

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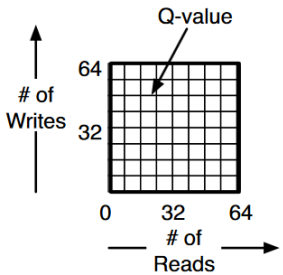

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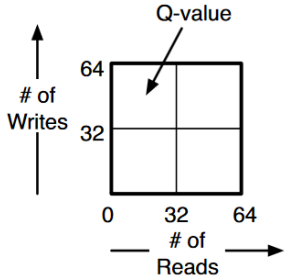

Figure: Coarse-grain

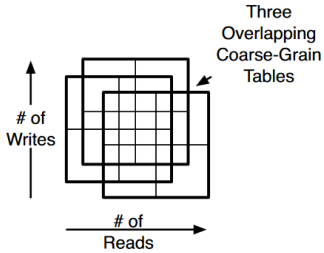

Figure: CMAC

Implementation

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$$cmd \leftarrow \text{select\_command\_with\_max\_Q-value}(C)$$

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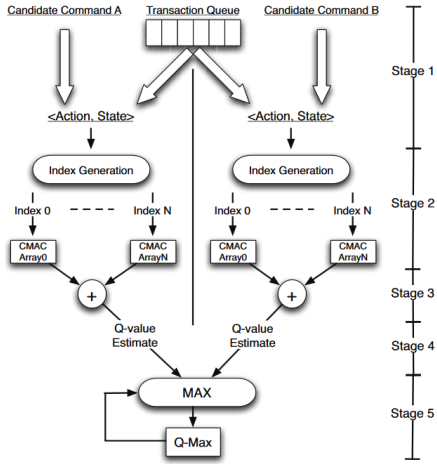
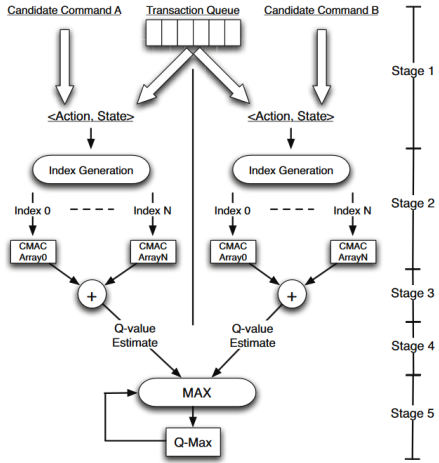


(a) 2-wide Q-value Estimation Pipeline

Implementation

$$cmd \leftarrow \text{select\_command\_with\_max\_Q-value}(C)$$

- Assumption: Scheduler's pipe can be clocked 10 times each DRAM cycle
- Scheduler can consider 12 commands every cycle



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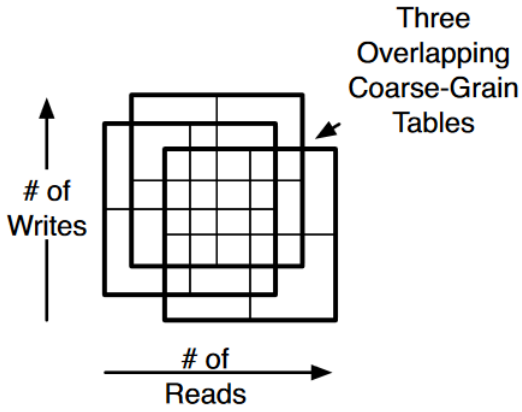

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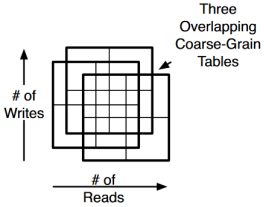
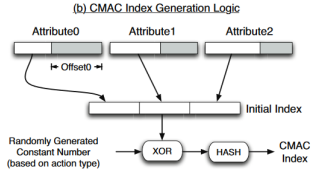
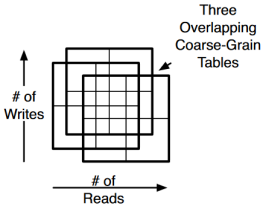
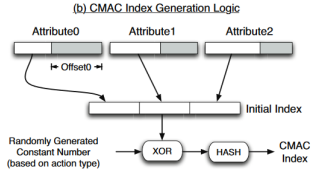




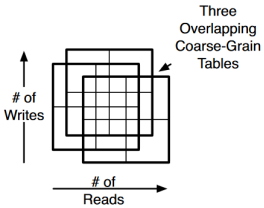
Implementation





- A constant number per action type $\rightarrow$ prevent generalization across different commands

Implementation



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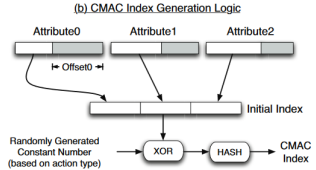

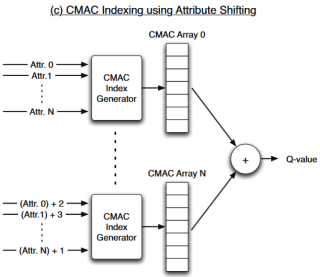

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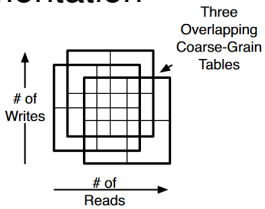

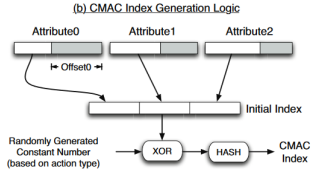

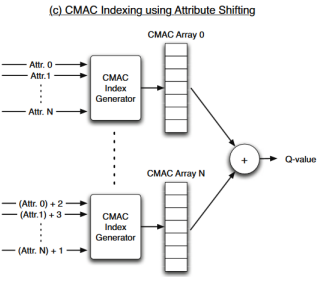

- A constant number per action type $\rightarrow$ prevent generalization across different commands
- random shifts of attributes implement the shiftedness of CMAC arrays

(Additional) Hardware Overhead

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1. logic to compute state attributes $\rightarrow$ counters that are updated every DRAM cycle

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2. logic to update Q-values $\rightarrow$ single pipelined 16-bit fixed-point multiplier
3. storing the Q-values $\rightarrow$ 32 kB on-chip storage

Key Results: Methodology & Evaluation

Methodology

Some important parameters of the simulated CMP:

- Frequency: 4 GHz
- #Cores: 4 (each 2-way simultaneously multithreaded)
- iL1/dL1 size: 32 kB
- Shared L2 cache: 4MB, 8-way

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Some important parameters of the simulated DRAM:

- DDR2-800 SDRAM
- Transaction Queue: 64 entries
- Peak Data Rate: 6.4 GB/s
- DRAM Bus Frequency: 400 MHz
- Single rank with 4 DRAM chips
- #Banks: 4 per DRAM chip
- Row Buffer Size: 2 KB

Applications & Benchmarks

Benchmark	Description	Problem size
Data Mining		
SCALPARC	Decision Tree	125k pts., 32 attributes
NAS OpenMP		
MG	Multigrid Solver	Class A
CG	Conjugate Gradient	Class A
SPEC OpenMP		
SWIM-OMP	Shallow water model	MinneSpec-Large
EQUAKE-OMP	Earthquake model	MinneSpec-Large
ART-OMP	Self-Organizing Map	MinneSpec-Large
Splash-2		
OCEAN	Ocean movements	514×514 ocean
FFT	Fast Fourier transform	1M points
RADIX	Integer radix sort	2M integers

Table 3: Simulated applications and their input sizes.

Compared Memory Controllers

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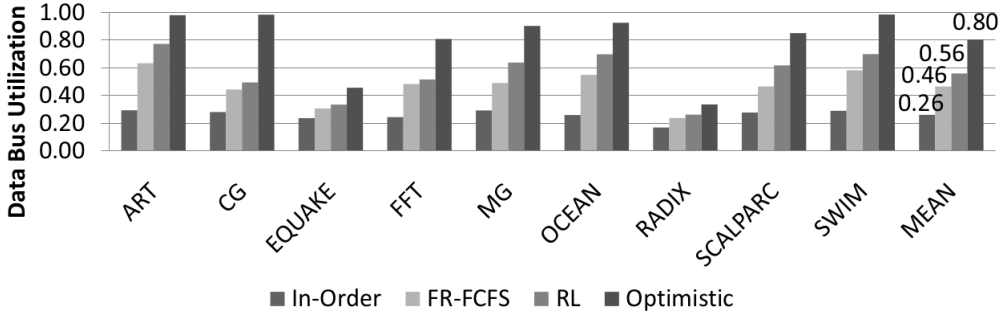
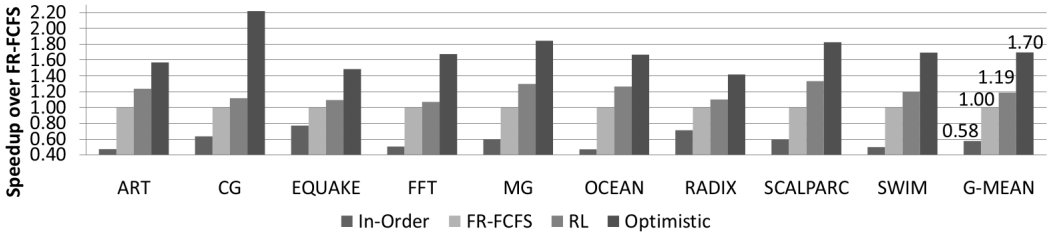
- An ideal scheduler with an ideal memory that can sustain 100% peak bandwidth

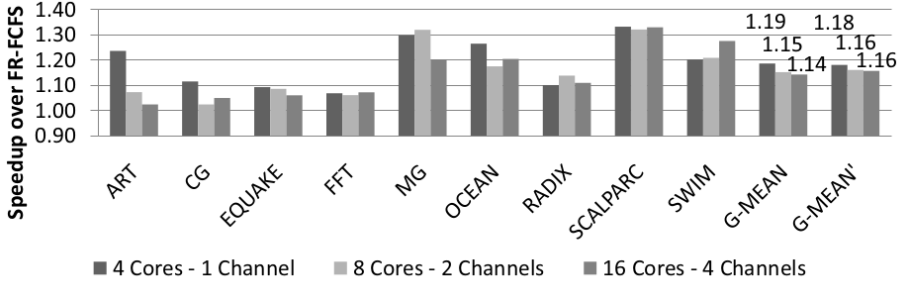
Results: Data Bus Utilization



Results: Performance Improvement



Results: Scaled to More Cores



Executive Summary

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Problem: Scheduling policies

- Cannot anticipate the long term effects of their scheduling decisions
- Cannot take lessons from the consequences of their past actions

Solution: RL-based controller computes learning, far-sighted policy $\rightarrow$ efficient bandwidth utilization

Results:

- 19% speedup, 21% more bandwidth utilization over best static policy
- Scales as well as the best static policy

Strengths & Weaknesses

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- Significantly improves overall performance and data bus utilization
- The paper accurately predicts that the DRAM bandwidth is going to be the main problem, 11 years ago!
- Well-written paper

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- More complicated hardware than FR-FCFS
- Extending it is hard since hardware will get even more complicated
- Heterogeneous workloads are not tested

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- Prioritize the threads that have attained the least service over others in each period

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- Dynamically group threads into a latency-sensitive cluster and a bandwidth-sensitive cluster

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- Dynamically group threads into a latency-sensitive cluster and a bandwidth-sensitive cluster
- Prioritize 1st cluster over 2nd cluster
- Employ different policies within each cluster

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  - "BLISS" [*L. Subramanian, D. Lee, V. Seshadri, H. Rastogi, O. Mutlu, IEEE Transactions on Parallel and Distributed Systems 2016*]

BLISS: Balancing Performance, Fairness and Complexity in Memory Access Scheduling

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- Mark each application either as vulnerable-to-interference or as interference-causing.

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- Prioritize requests from 1st group over requests from 2nd group

Key Takeaways

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- Comes with some hardware cost
- QoS-unaware $\rightarrow$ no fairness
- Seemingly hard to improve

Open Discussion

Discussion

How can we solve the fairness problem while keeping our RL-based approach?

Discussion

Are there other flaws in this approach?

Discussion

Can this approach be used to solve other scheduling problems?

Discussion

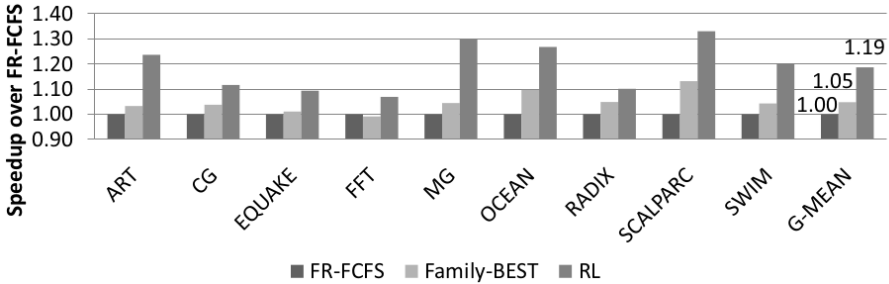
When are machine-learning based approaches applicable in computer architecture?

Backup slides

Ensuring correct operation

- the scheduler is not permitted to select NOPs when other legal commands are available
- the scheduler is only allowed to activate rows due to pending requests in the transaction queue (i.e., the scheduler cannot choose to activate an arbitrary row with no pending requests)
- the scheduler is not allowed to precharge a newly activated row until it issues a reador write command to it.

Results: RL versus Family-BEST



Results: RL versus Family-BEST

Preference relations used in Family-BEST:

- Row commands over column commands
- Older commands over younger commands
- Reads over writes
- Load misses over store misses
- More critical load misses over less critical ones, based on sequence numbers

Results: Online versus Offline