Mirage Cores

The Illusion of many Out-of-Order Cores Using In-order Hardware

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Executive Summary

- **Problem:**
  - Practical power and thermal constraints limit the deployment of homogeneous multicore systems with many big OoO cores
  - Low performance of InO cores limits their widespread usage

- **Goal:**
  - The goal is to design a Het-CMP with near OoO performance and InO energy consumption

- **Idea:**
  - The idea is to use clusters of InO cores around one OoO core
  - The OoO core is used as a «scheduler» and the InO cores as «workers»

- **Evaluation:**
  - The Mirage Core can achieve on average **84% performance** of a Homo-CMP, while conserving **55% of energy** and **25% of area costs**
Overview

- Background, Problem and Goal
- Novelty, Key Approach and Ideas
- Mechanisms (in some detail)
- Key results, Methodology and Evaluation
- Summary
- Strengths and Weaknesses
- Thoughts and Ideas
- Key Takeaways
- Open Discussion
Out-of-Order cores

- Improve latency of programs
- Contain additional HW to reorder instructions to minimize stalls (ROB, RS, LSQ, etc.)
- This increased performance comes at the cost of increased power consumption

![Graph showing comparison between Out-of-Order (OoO) and InOrder (InO) cores for Performance, Power, Energy, and Area. The graph compares overall, HPD category, and LPD category.]
Heterogeneous Computing

- Systems contain mixed processor types (e.g. CPUs and GPUs on the same chip)
- Built in logic for interfacing with additional HW
- Hardware accelerators
Goal

Design a processor that...

- has high throughput and single-threaded performance...
- and is very energy-efficient
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ARM big.LITTLE Architecture

- **Released in 2011**
  - Many Android Smartphones
  - Apple A series (A14 used in iPhone 12s)
  - Nintendo Switch using Nvidia Tegra XL
Mirage Core Architecture

(i) Homogeneous OoO CMP
- Low system throughput
- Shorter execution latency

(ii) Homogeneous InO CMP
- High system throughput
- Longer execution latency

(iii) Mirage Cores
- High system throughput
- Shorter execution latency
Mirage Core Architecture
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Memoization

- Calculating the 5th Fibonacci Number using recursion

```
<table>
<thead>
<tr>
<th>fib(5)</th>
<th>fib(3)</th>
<th>fib(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>fib(4)</td>
<td>fib(1) = 1</td>
<td>fib(1) = 1</td>
</tr>
<tr>
<td>fib(0) = 0</td>
<td>fib(0) = 0</td>
<td>fib(0) = 0</td>
</tr>
</tbody>
</table>
```
Memoization

- Calculating the 5th Fibonacci Number with Memoization, by storing intermediate values in an array.

**Stored values for Fibonacci**

<table>
<thead>
<tr>
<th>fib(n)</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
</tbody>
</table>
Memoization

- Reordering of long latency events only accounts for 19% of the performance advantage of OoO’s.
- Most applications spend most of their time in loops.
- This means that scheduling usually holds the same pattern in similar contexts.
Memoizability

Switching after n cycles

Performance relative to no switching
% Ttotal instructions memoized

Memoizability
Designing the Arbitrator

- Energy-Efficiency Oriented Arbitration
- System Throughput Oriented Arbitration
- Fairness Oriented Arbitration
Energy-Efficiency Oriented Arbitration

- Schedule Cache Misses per Kilo Instructions (SC-MPKI) quantify the usefulness of memoization.
- Picks the application with the highest SC-MPKI above a certain threshold.
- If none are above the threshold, OoO is turned off to conserve energy.

\[
\Delta SC-MPKI = \frac{SC-MPKI_{InO} - SC-MPKI_{OoO}}{SC-MPKI_{OoO}}
\]
Energy-Efficiency Oriented Arbitration

- Application 1
  - Has high SC-MPKI\textsubscript{InO}
  - Has low SC-MPKI\textsubscript{OoO}
  - InO-OoO is high
  - -> good candidate for memoization, as it performs well on OoO, but bad on InO

- Application 2
  - Has low SC-MPKI\textsubscript{InO}
  - Has low SC-MPKI\textsubscript{OoO}
  - InO-OoO is near 0
  - -> bad candidate for memoization, as it already performs near OoO

- Application 3
  - Has high SC-MPKI\textsubscript{InO}
  - Has high SC-MPKI\textsubscript{OoO}
  - InO-OoO is near 0
  - -> bad candidate for memoization, because the code probably has unpredictable control flow
System Throughput Oriented Arbitration

- Overall system throughput (STP) as metric for the scheduler
- Migrates the slowest application to the OoO
- Traditional design on heterogeneous chips

\[
\text{speedup}_i = \left( \frac{IPC_{InO(i)}}{IPC_{OoO(i)}} \right)
\]
Fairness Oriented Arbitration

- Arbitrator migrates application in **round robin order**
- \( \text{Util}(i) \) metric to determine each application’s timeshare
- Application will be migrated only if either \( \text{Util}(i) \) is less than \( 1/(\#\text{apps}) \) or if \( \Delta \text{SC-MPKI} \) falls below the threshold

\[
\text{Util}(i) = \left( \frac{t_{OoO(i)} + t_{InOmemoize}(i) \times \text{speedup}_i}{t_{\text{overall}}} \right)
\]
Designing the Core Architecture

- Designing the OoO core
- Designing the InO core
- Migration between the cores
Designing the OoO Core

- In order to memoize schedules, the OoO must be able to recognize
  - (a) when a trace is repetitive
  - (b) if its instructions are scheduled in the same order

- Traces that are deemed memoizable are stored in the schedule cache

- Metrics used to compare two traces are execution time, IPC, memory characteristics, branch misses and reordered instructions
DynaMOS: dynamic schedule migration for heterogeneous cores

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University of Michigan, Ann Arbor, MI
Designing the InO Core

Introduces the **OinO mode** with following modifications

- Atomic Execution
- Physical Register File
- Load/Store Queue
- Schedule Cache
Atomic Execution

- InO cores cannot detect unexpected events like branch mispredictions or memory aliases
- Forces the OinO to execute schedules atomically
- On misprediction, resets the whole execution and executes in original, non-memoized program order
Physical Register File

- OinO is supplemented with expanded register file that maps every architectural register to at most 4 physical registers (PR), resulting in a 128 entry PRF
- Bookkeeping adds an additional 28 bytes of storage
- A bigger PRF and tables adds 14% dynamic energy to the InO
Load-Store Queue

- Implemented to circumvent memory alias errors for load and store operations
- Is added to every recorded schedule as a fixed-size meta-data block and adds 20B
- 32 entry LSQ contributes 5.5% overhead to the dynamic energy of OinO
Schedule Cache

- 8KB cache that stores schedules memoized and transferred from the OoO
- Trace mis-speculations and SC writes are very expensive
- Employ an algorithm that is heavily biased against traces that mis-speculate
- Eviction policy: unmemoizable traces -> least recently used
- Contributes 10% towards leakage energy but reduces L1 iCache access energy
Migration between cores

- Must store all of the active core’s state, including the RF, PC, control bits, store buffer entries, etc. into memory on migration and its pipeline must be flushed.
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Methodology

- **OoO:**
  - 3 wide superscalar @ 2 GHz
  - 12 stage pipeline
  - 128 entry ROB
  - 128 entry integer register file
  - 256 entry floating-point register file
  - 8KB Schedule Cache

- **InO:**
  - 3 wide superscalar @ 2 GHz
  - 8 stage pipeline
  - 128 entry integer register file
  - 128 entry floating-point register file
  - 8KB Schedule Cache

- **Memory System:**
  - 32 KB L1 iCache @ 2 cycles
  - 32 KB L1 dCache @ 2 cycles
  - 2 MB shared L2 Cache with stride prefetcher @ 15 cycles
  - 8192 MB Main Memory @ 120 cycles
  - 32 B L1-L2 bus @ 2 GHz
Methodology

- 27 applications from SPEC 2006 benchmark suite
- Gem5 simulator to model Mirage Cores
- McPAT modeling framework to estimate area, static and dynamic energy consumption for the core and L1 caches

<table>
<thead>
<tr>
<th>Category</th>
<th>IPC Ratio</th>
<th>Benchmarks</th>
</tr>
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<tbody>
<tr>
<td>High Performance Difference (HPD)</td>
<td>&lt; 60%</td>
<td>cactusADM, bwaves, gamess, gromacs, h264ref, hmmer, leslie3d, libquantum, mcf, milc, povray, tonto, zeusmp</td>
</tr>
<tr>
<td>Low Performance Difference (LPD)</td>
<td>&gt;= 60%</td>
<td>GemsFDTD, astar, bzip2, calculix, dealII, gcc, gobmk, namd, omnetpp, perlbench, sjeng, wrf, xalancbmk</td>
</tr>
<tr>
<td>Evaluation</td>
<td>8:0 Homo-InO</td>
<td>0:8 Homo-OoO</td>
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</table>
Architecture Configuration

![Architecture Configuration diagram]

- **n:0 Homo-InO**
- **n:1 MirageCores**
- **n:1 Traditional Cores**

The diagram shows the area relative to Homo-OoO across different numbers of InO cores per OoO: 4, 8, 12, and 16. The area is represented in percentages, with Homo-OoO at 100%. The chart illustrates the comparison between Homo-InO, MirageCores, and Traditional Cores for each number of cores.
Architecture Configuration

- n:0 Homo-InO
- n:1 MirageCores
- n:1 Traditional Cores

Area relative to Homo-OoO

Number of InO cores per OoO: 4, 8, 12, 16

+55%
Architecture Configuration

Number of InO cores per OoO

Area relative to Homo-OoO

n:0 Homo-InO  n:1 MirageCores  n:1 Traditional Cores

+23%
Performance

![Graph showing performance relative to Homo-InO]

- **Homo-InO**
- **SC-MPKI**
- **SC-MPKI+maxSTP**
- **maxSTP**

Number of InO cores per OoO:
- 4
- 8
- 12
- 16

STP relative to Homo-InO
Performance

The chart shows the performance of different configurations relative to Homo-InO. The configurations include Homo-InO, SC-MPKI, SC-MPKI+maxSTP, and maxSTP. The x-axis represents the number of InO cores per OoO, with values 4, 8, 12, and 16. The y-axis represents STP relative to Homo-InO, ranging from 0% to 100%.
Performance

Number of InO cores per OoO:

- 4
- 8
- 12
- 16

Performance metrics:

- Homo-InO
- SC-MPKI
- SC-MPKI+maxSTP
- maxSTP

STP relative to Homo-InO
Performance

The image shows a bar chart comparing performance across different configurations of InO cores per OoO. The chart compares four different methods:

- Homo-InO
- SC-MPKI
- SC-MPKI+maxSTP
- maxSTP

The x-axis represents the number of InO cores per OoO, with values 4, 8, 12, and 16. The y-axis represents the STP relative to Homo-InO, ranging from 0% to 100%. The bars indicate the performance percentage for each configuration at different core counts.
Energy Consumption

Difference due to bigger PRF and LSQ in OinO
Case Study

maxSTP

SC-MPKI
Analyses of Benchmark Categories

- **8:1 configuration**
Arbitrator for Equal Resource Sharing

- **8:1 configuration**

Utilization of OoO per benchmark in a workload mix for the 8:1 configuration:

- SC-MPKI-fair
- Fair
- SC-MPKI
- maxSTP

Performance:
- Homo-InO
- SC-MPKI-fair
- fair

Utilization:
- Homo-InO
- SC-MPKI-fair
- fair

Energy:
- Homo-InO
- SC-MPKI-fair
- fair

Number of InO cores per OoO core:
- 4
- 8
- 12
- 16
Area Neutral Study

- Performance
- Utilization
- Energy
- Area

Bar chart showing:
- 8:1, SC-MPKI
- 5:3, maxSTP

Relative to Homo-OoO

Key:
- Green arrow indicates improvement
- Red arrow indicates decrease
Cost of Core Migration

![Cost of Core Migration Diagram]
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Summary

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  ▪ Practical power and thermal constraints limit the deployment of homogeneous multicore systems with many big OoO cores
  ▪ Low performance of InO cores limits their widespread usage

▪ Goal:
  ▪ The goal is to design a Het-CMP with near OoO performance and InO energy consumption

▪ Idea:
  ▪ The idea is to use clusters of InO cores around one OoO core
  ▪ The OoO core is used as a «scheduler» and the InO cores as «workers»

▪ Evaluation:
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Strengths

- Simple Idea, that can achieve high system throughput and low energy consumption without having to make a heavy tradeoff on single thread performance.
- Scheduler is flexible to fulfil the users needs, hence applicable to many systems.
- Tackles an important problem in energy consumption
- Well-written, easy to understand paper
Weaknesses

- Does not go too much into detail when it comes to multithreaded computing
- Gives no programming model or example design
- Only looks at CPU heterogeneity
- Servers cannot profit off this architecture due to more irregular fetch patterns
- Is only efficient when there is a good mix between LPD and HPD workloads
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Intel Core Alder Lake (2021)

- 8 «little» Gracemont cores for high efficiency
- 8 «big» Golden Cove cores for high performance with multithreading
- 24 threads in total
- including a HW scheduler
- To be released in 2021
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Key Takeaways

- A nice approach to get high system throughput, high single-thread performance and low energy consumption at the same time.
- Does not require a lot of new additional HW
- Flexible Arbitrator Design
- There is a lot to build on with this idea
- Heterogeneous Designs are an important tool for increased energy efficiency
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Open Discussion

- Fields where the Mirage Core can be applied
- What needs to be changed to make it efficient for servers?
- What needs to be changed to make it efficient for multithreading?
- Can the Mirage Cores problems be fixed by adding more heterogeneity in general?
- Hardware accelerators that can be used