Self-Optimzing Memory Controllers: A Reinforcement Learning Approach

Engin Ipek[1,2] Onur Mutlu[2] José F. Martinez[1] Rich Carauana[1]

[1] Cornell University, Ithaca, NY 14850 USA
[2] Microsoft Research, Redmond, WA 98052 USA

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Presented by Valery Fischer

Summary

Problem & Goal

Key Ideas

Novelty

Mechanisms & Implementation

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Main Takeaways

Critique and Discussion

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Discussion

Summary

Executive Summary

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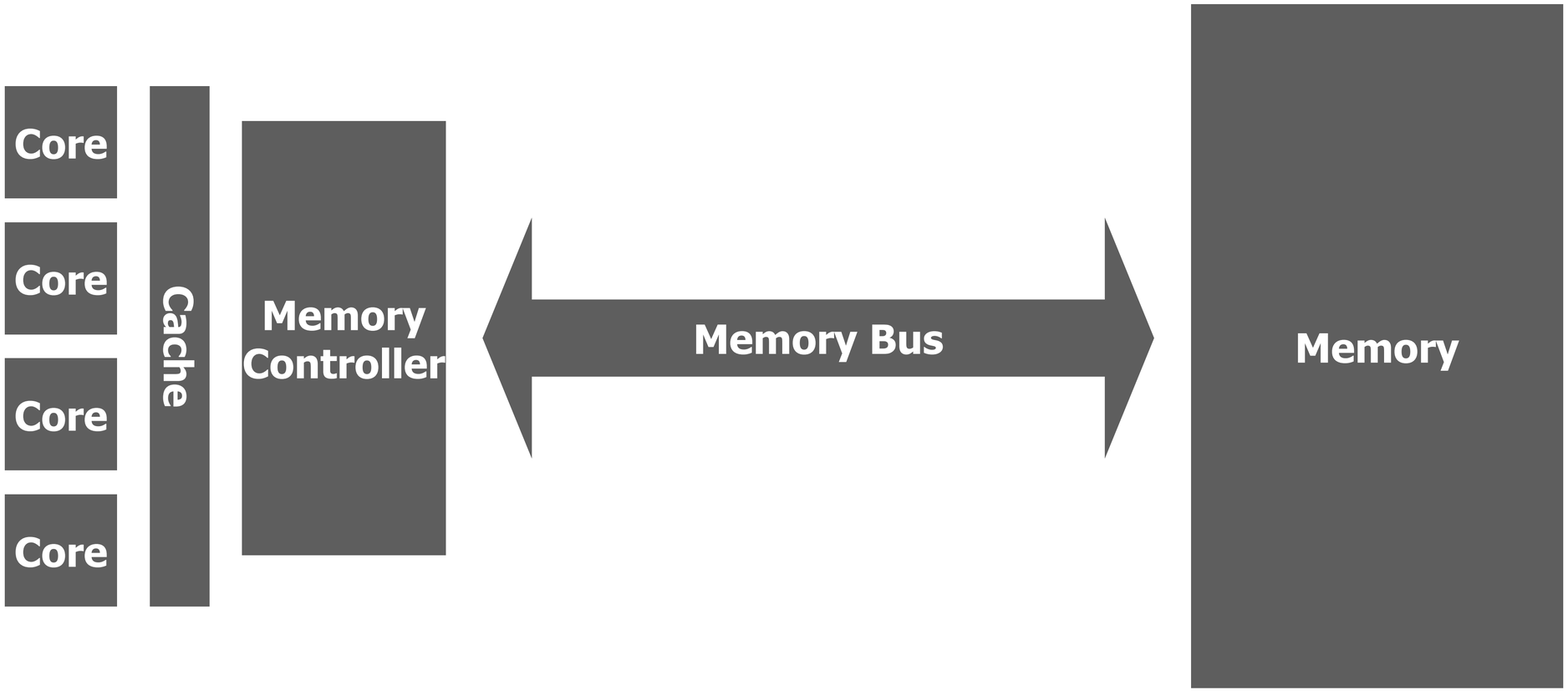
Results: An RL-based memory controller improves performance of parallel applications on a 4-core CMP by 19% on average and DRAM bandwidth utilization by 22% compared to FR-FCFS

Memory Controllers



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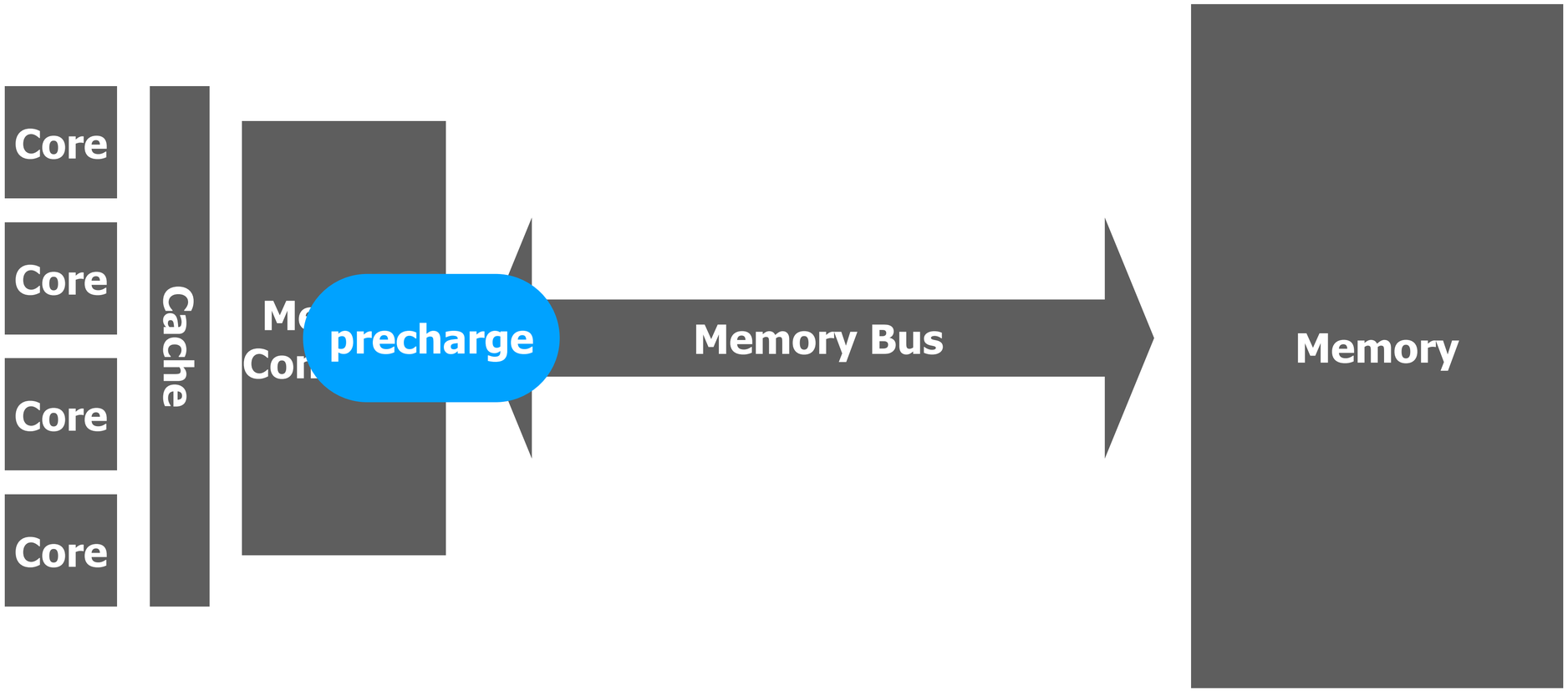

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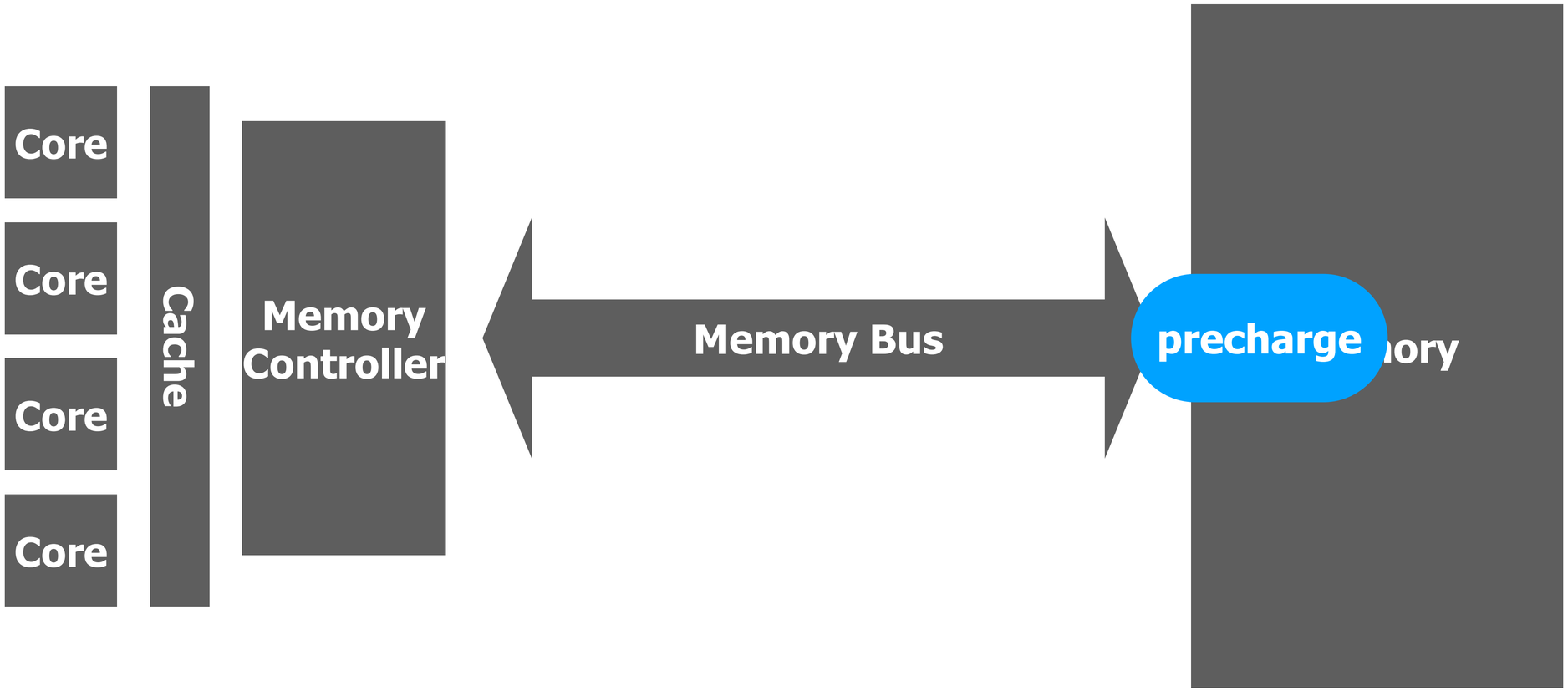
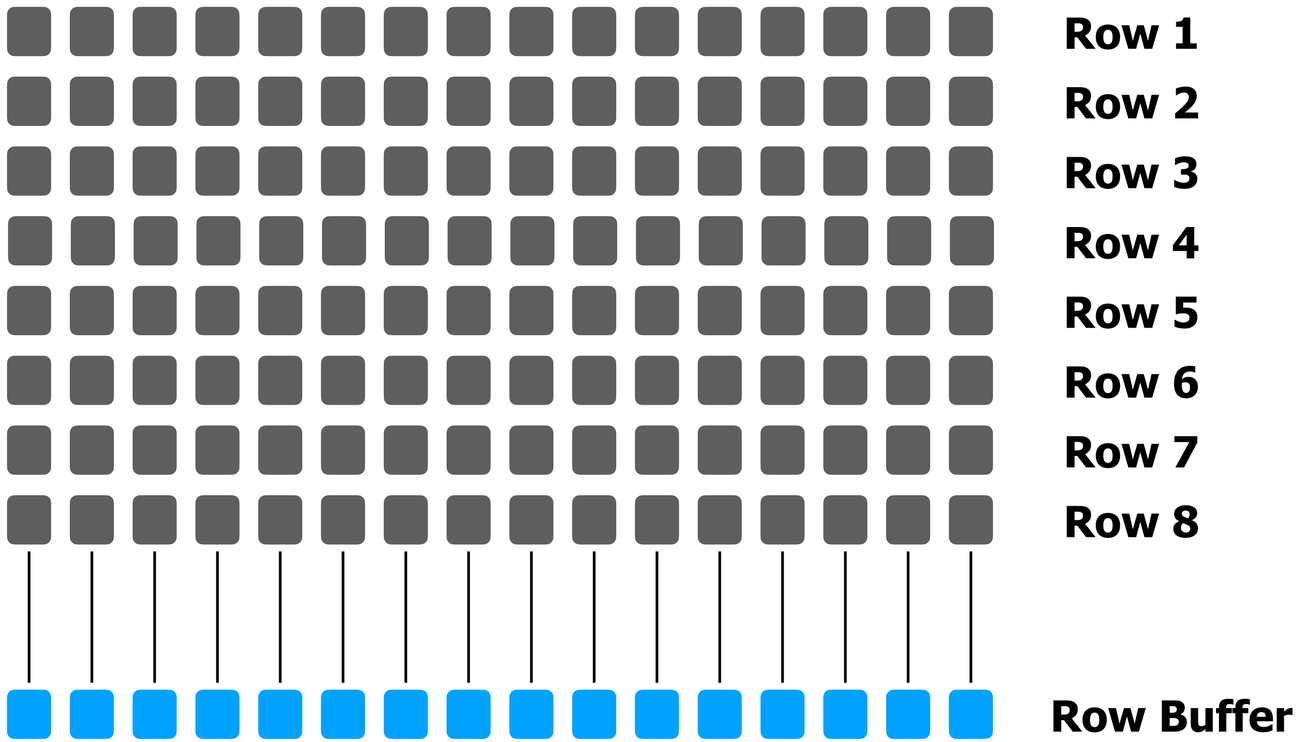


DRAM Bank (Precharge)



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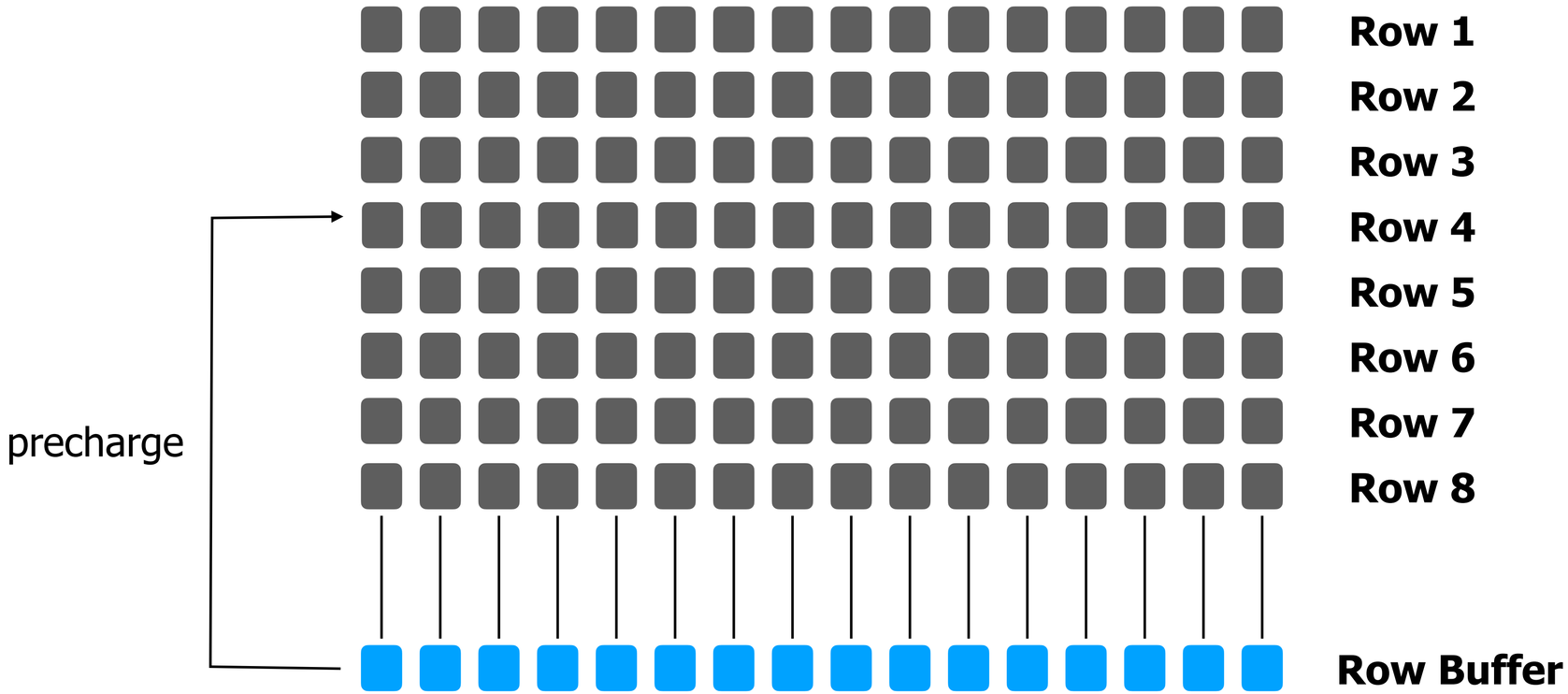

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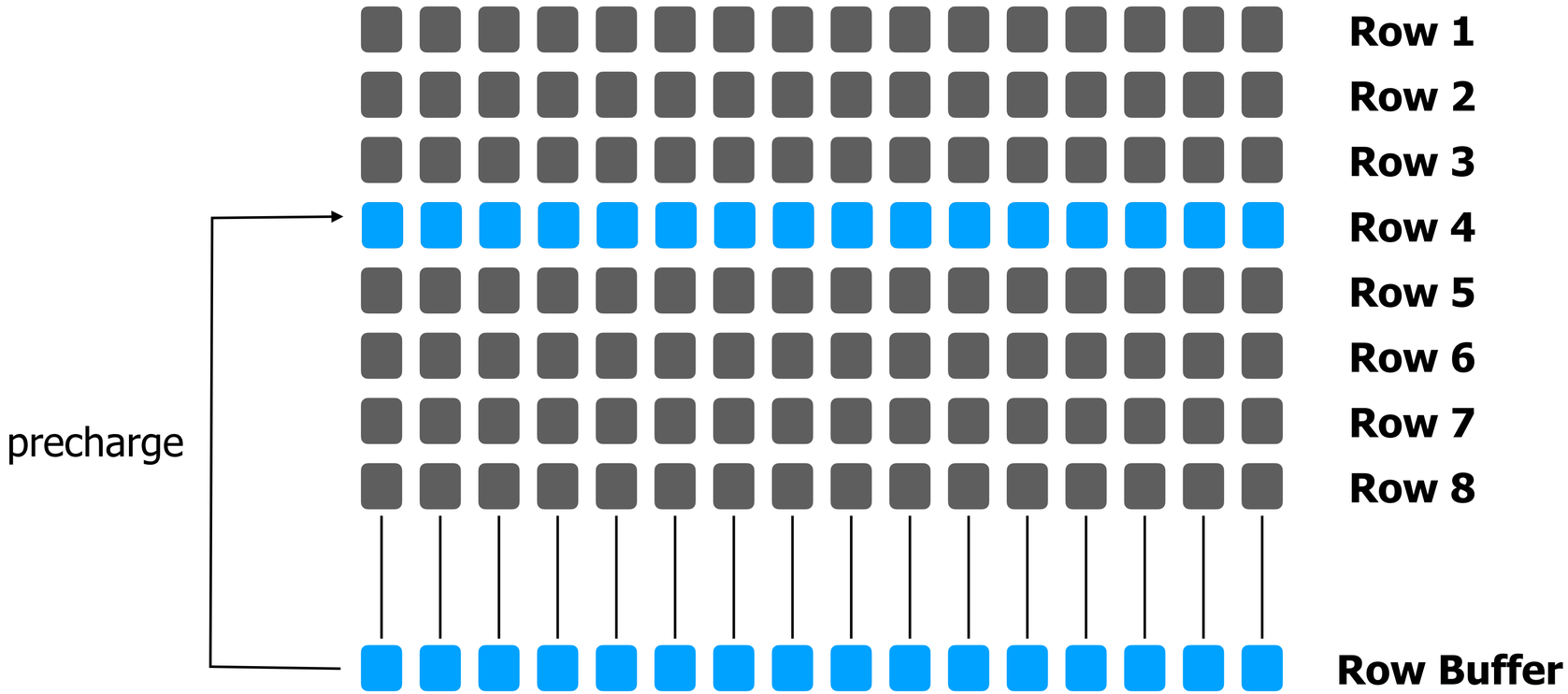

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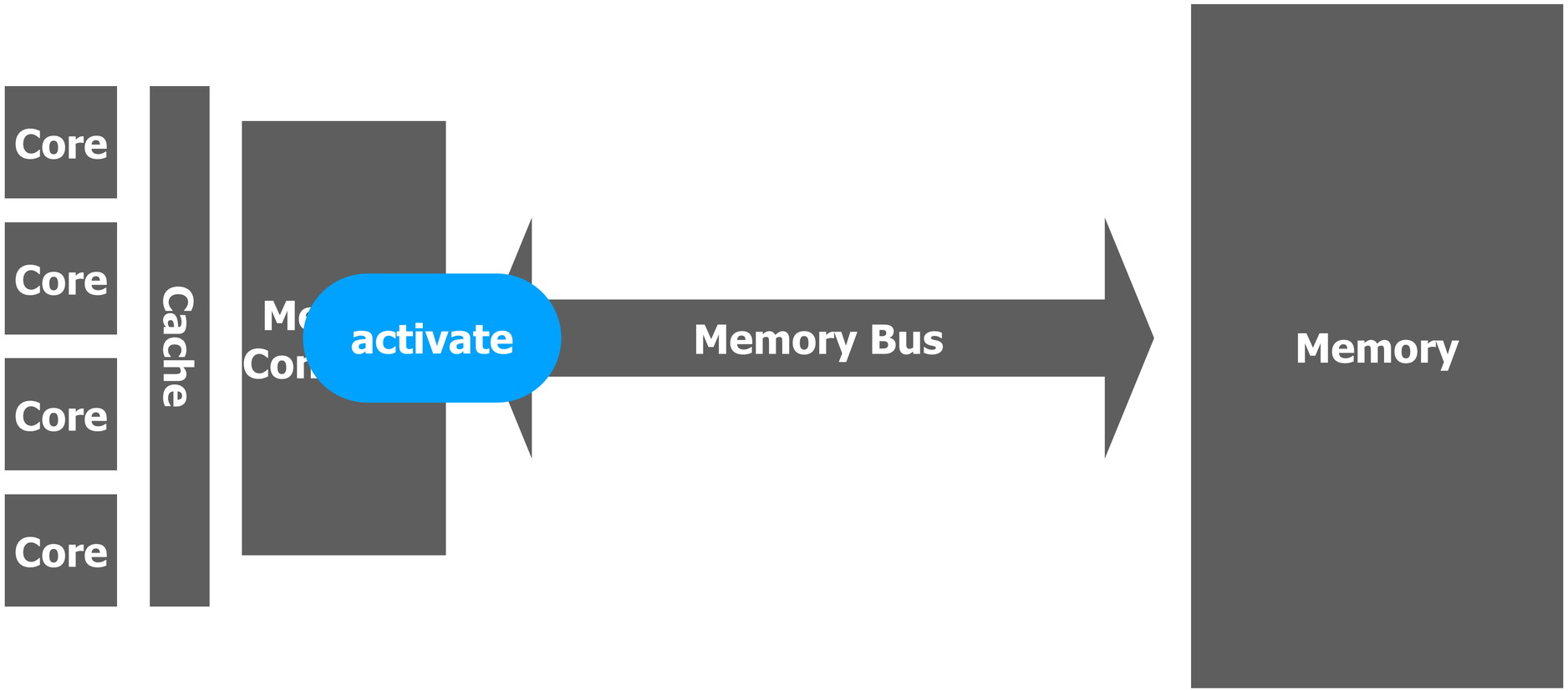

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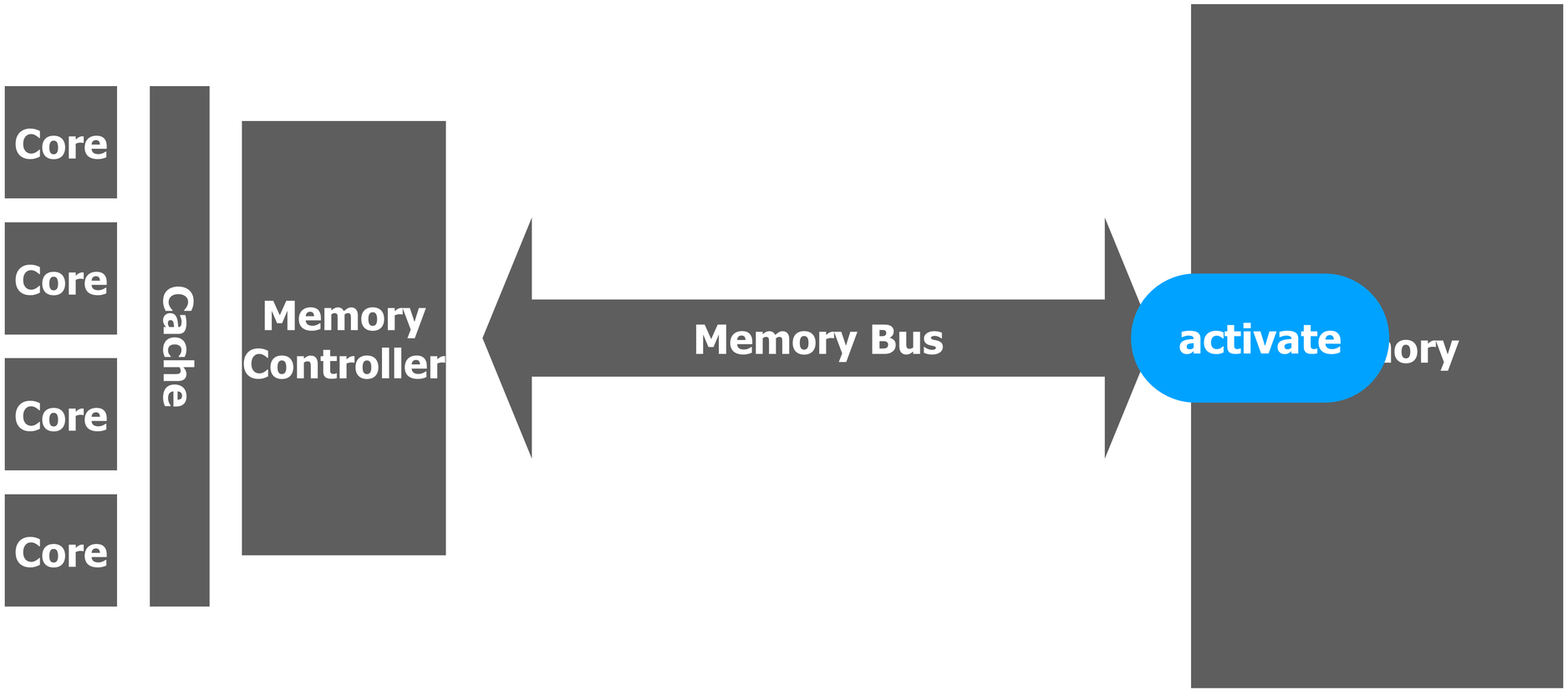
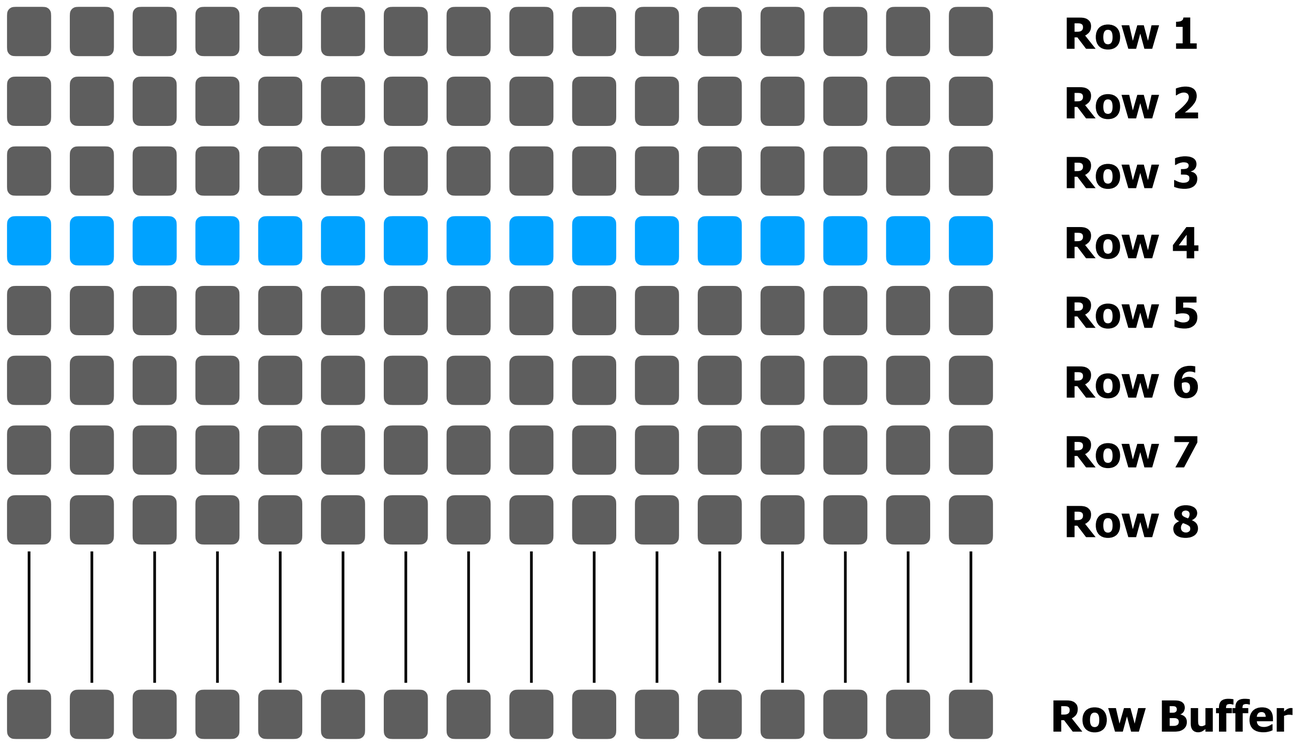


DRAM Bank (activate)



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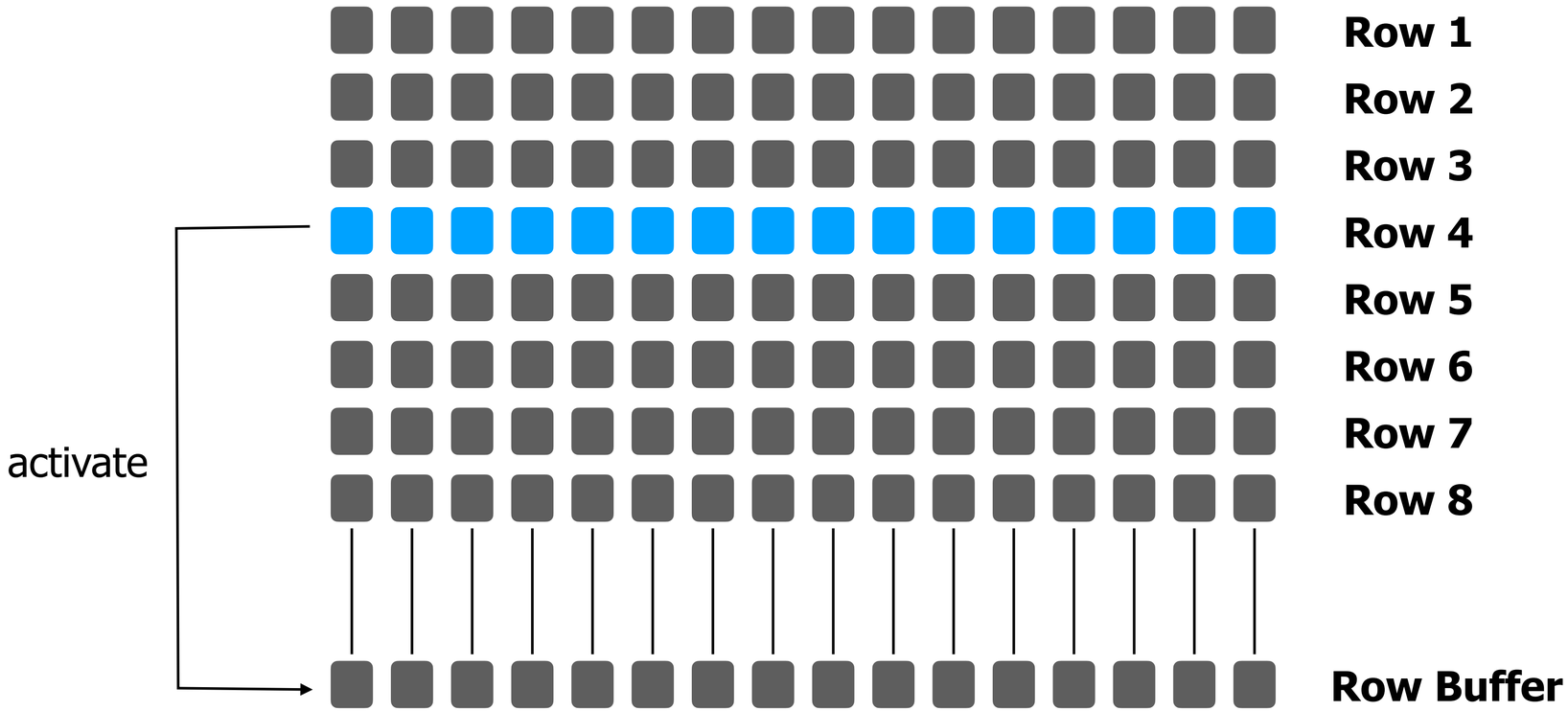

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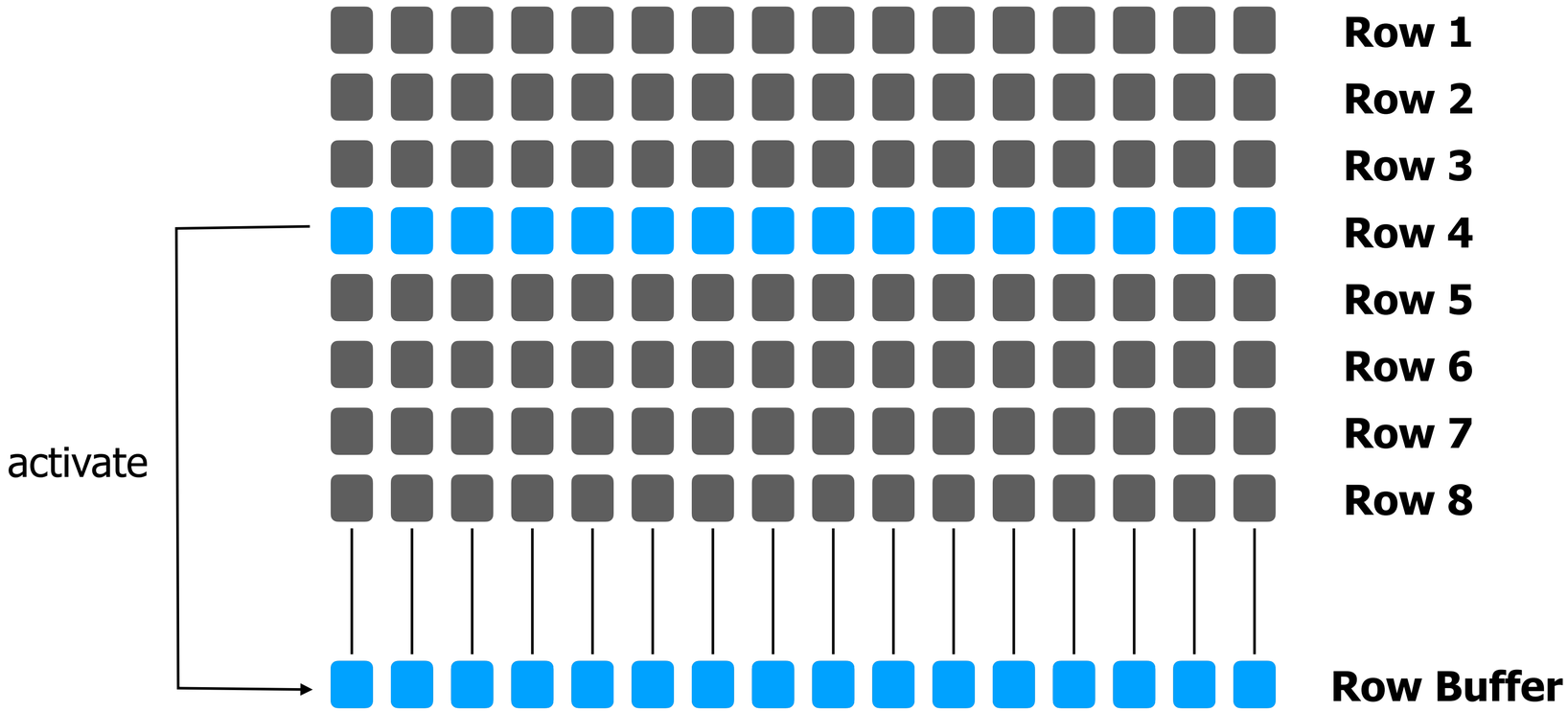

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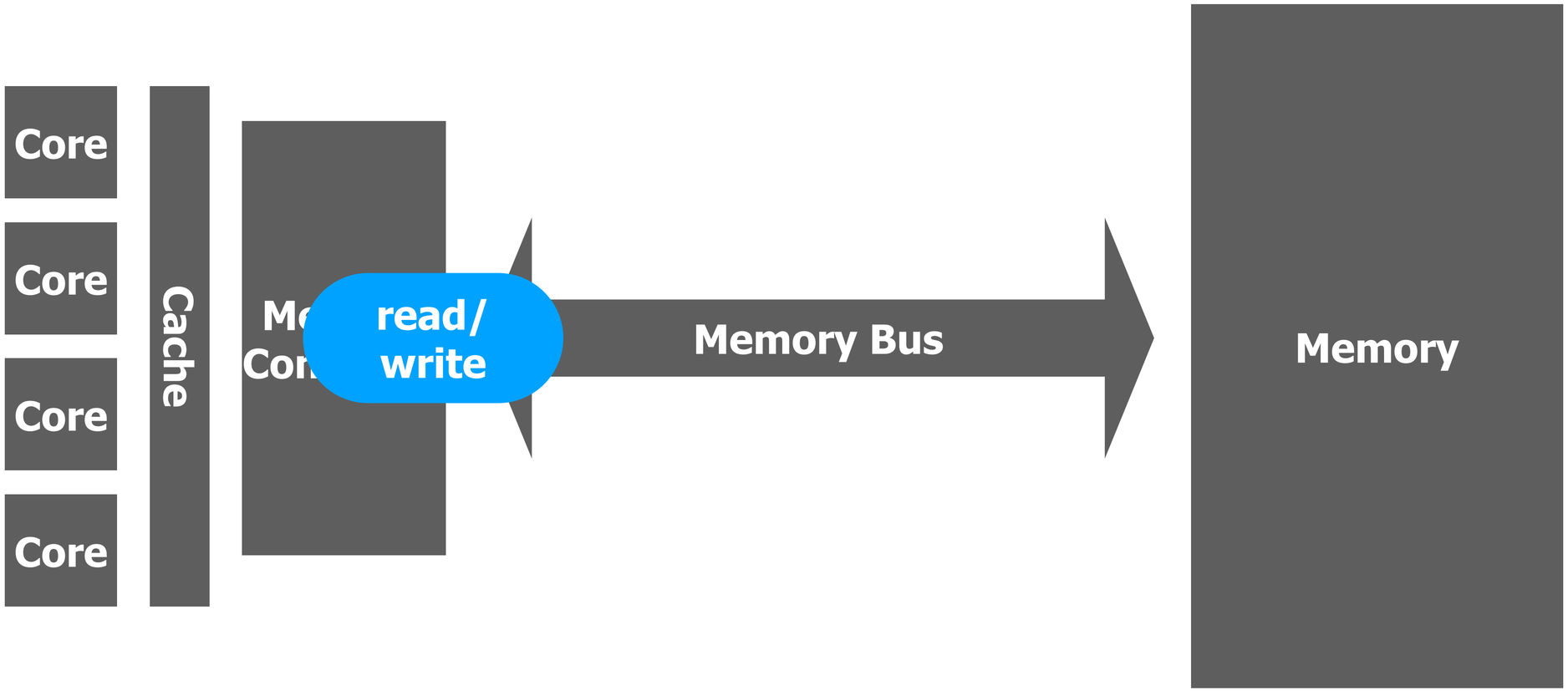

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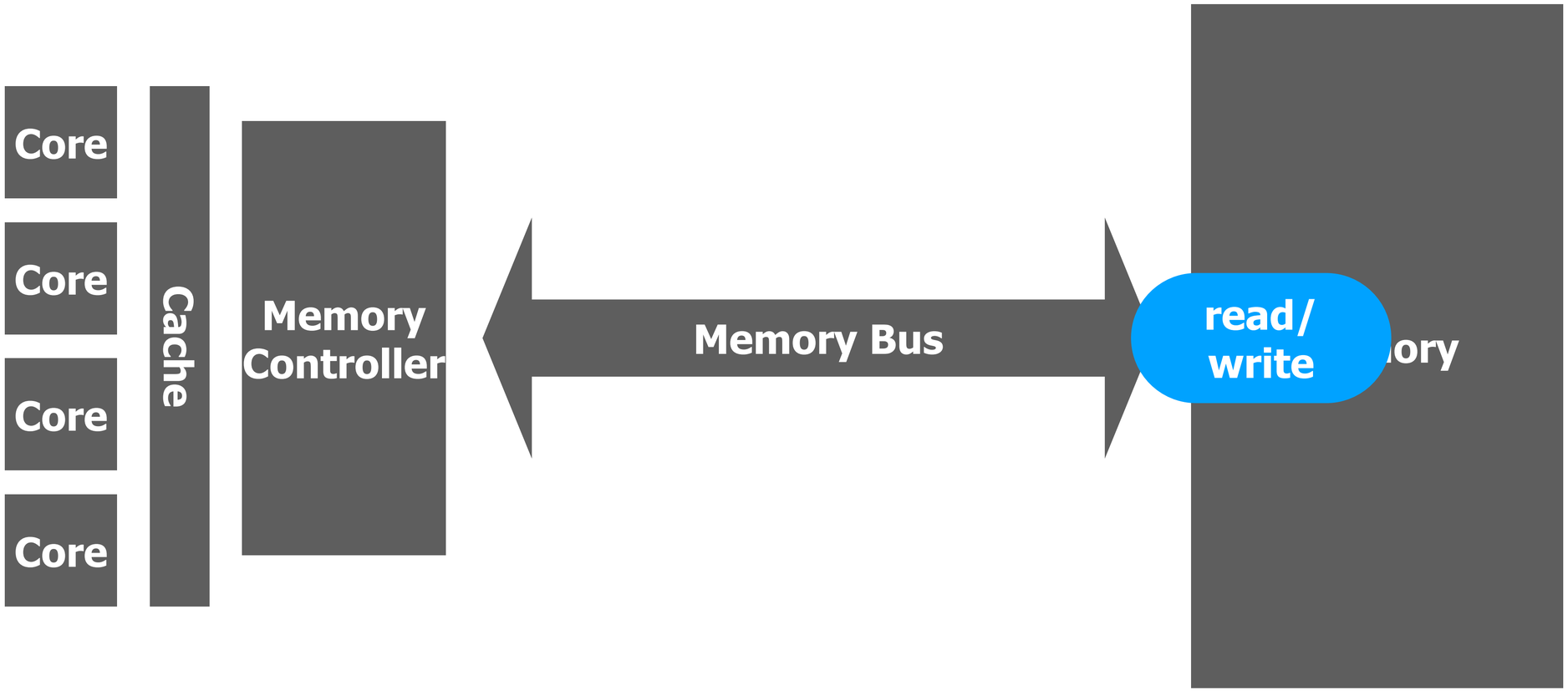
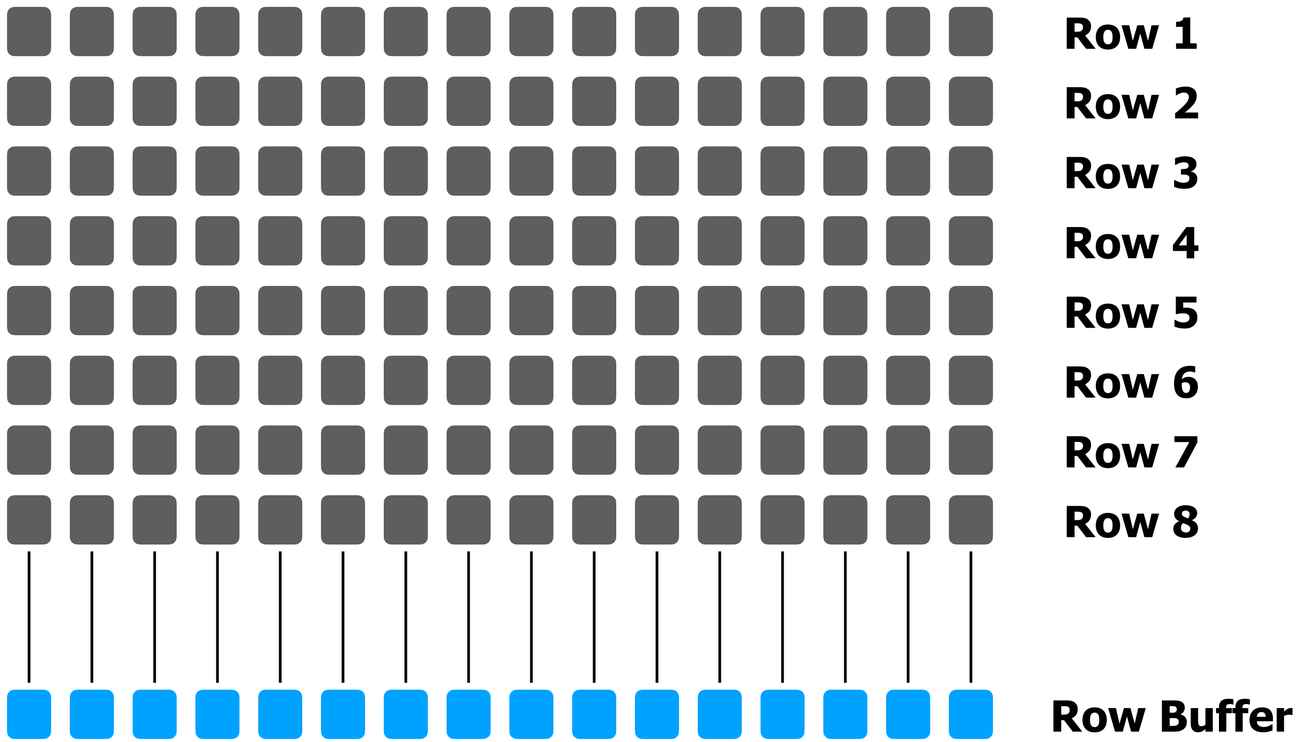


DRAM Bank (read/write)



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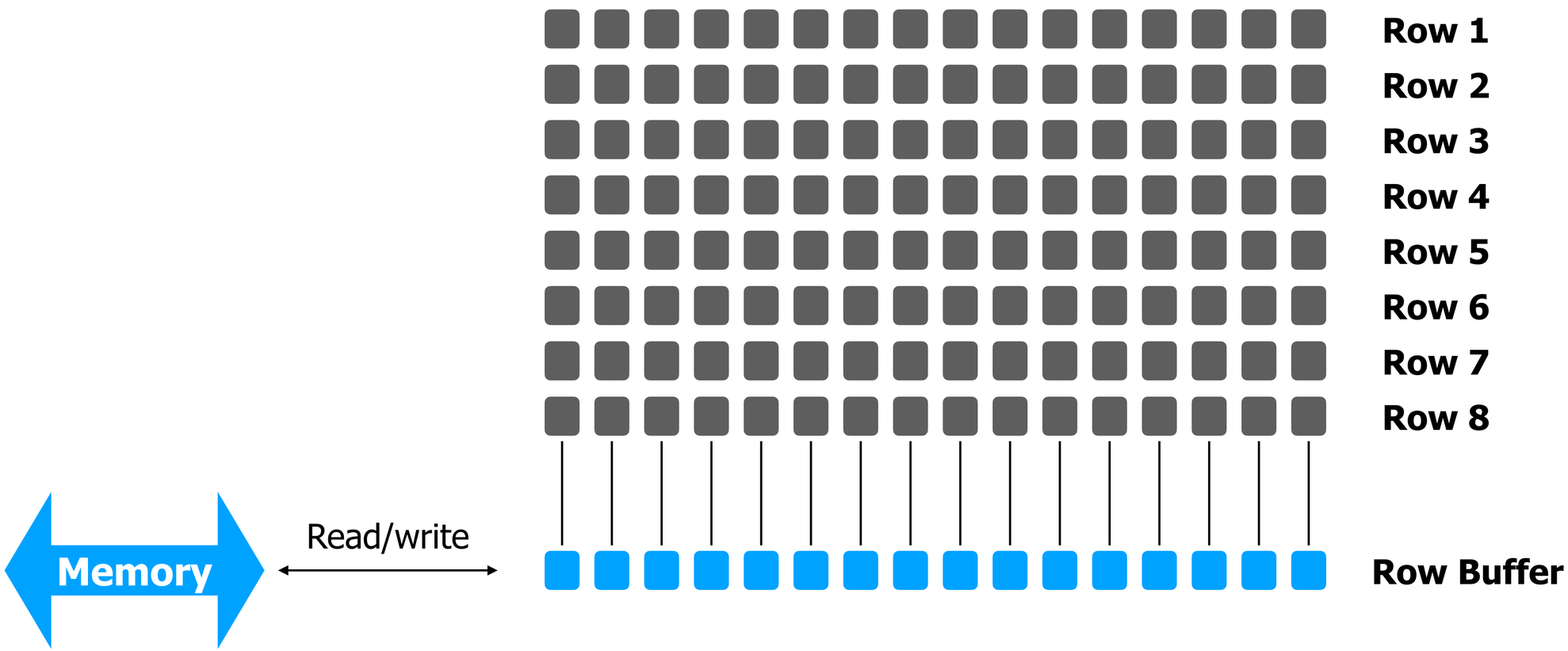

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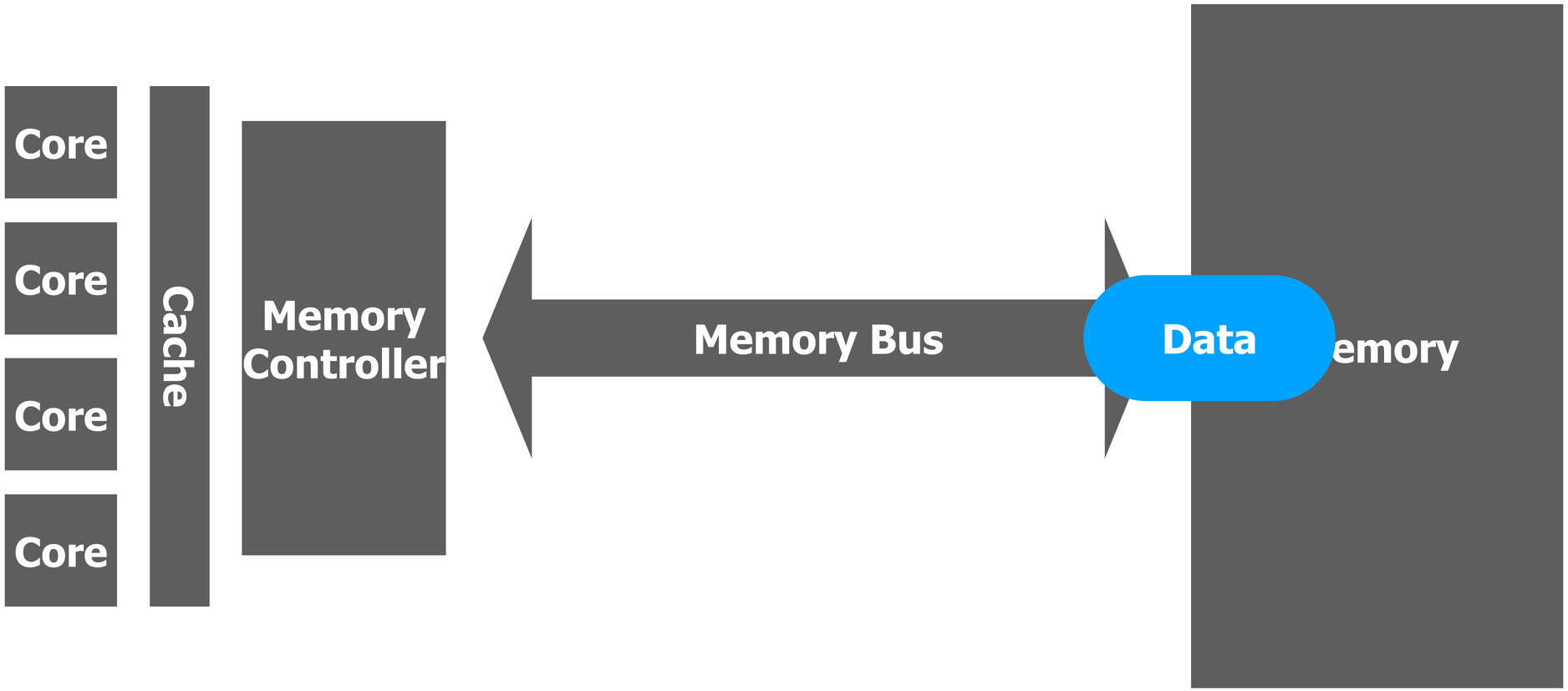

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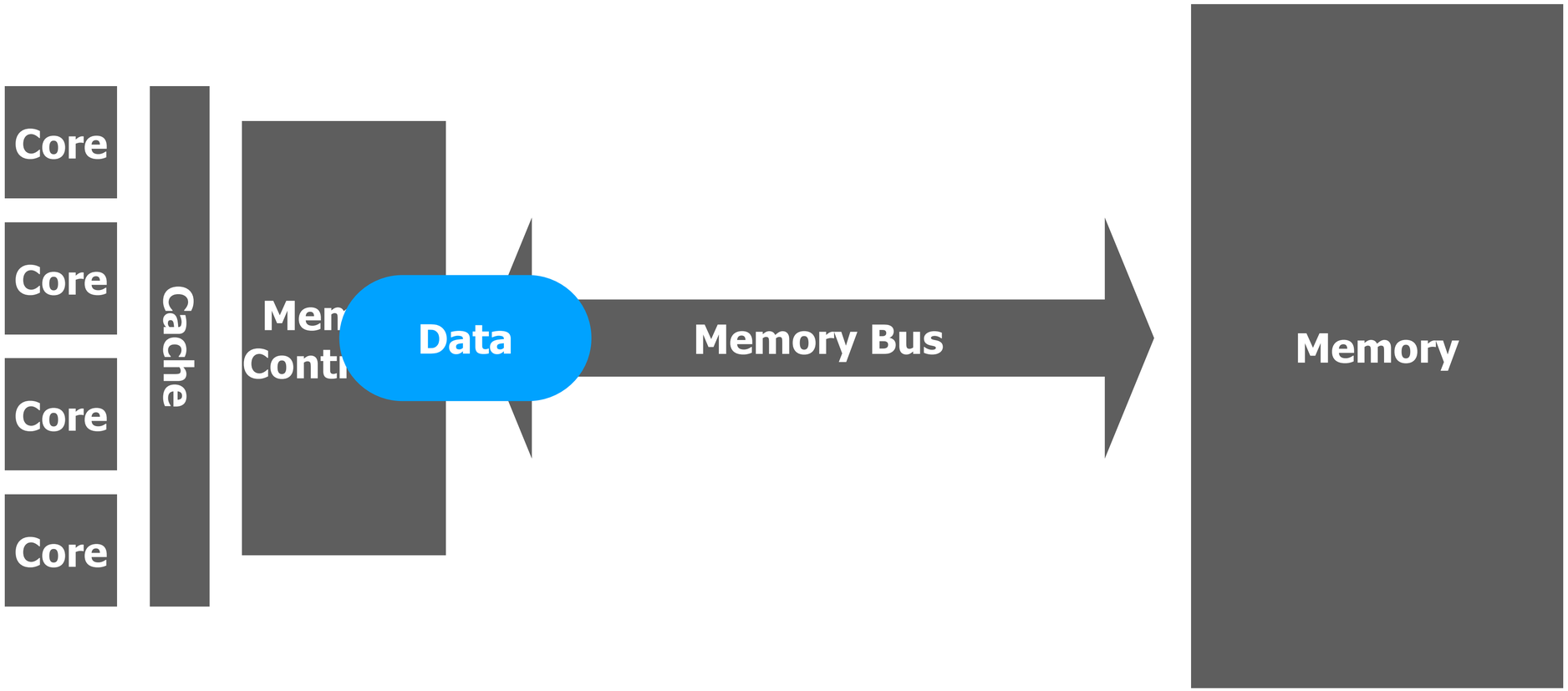

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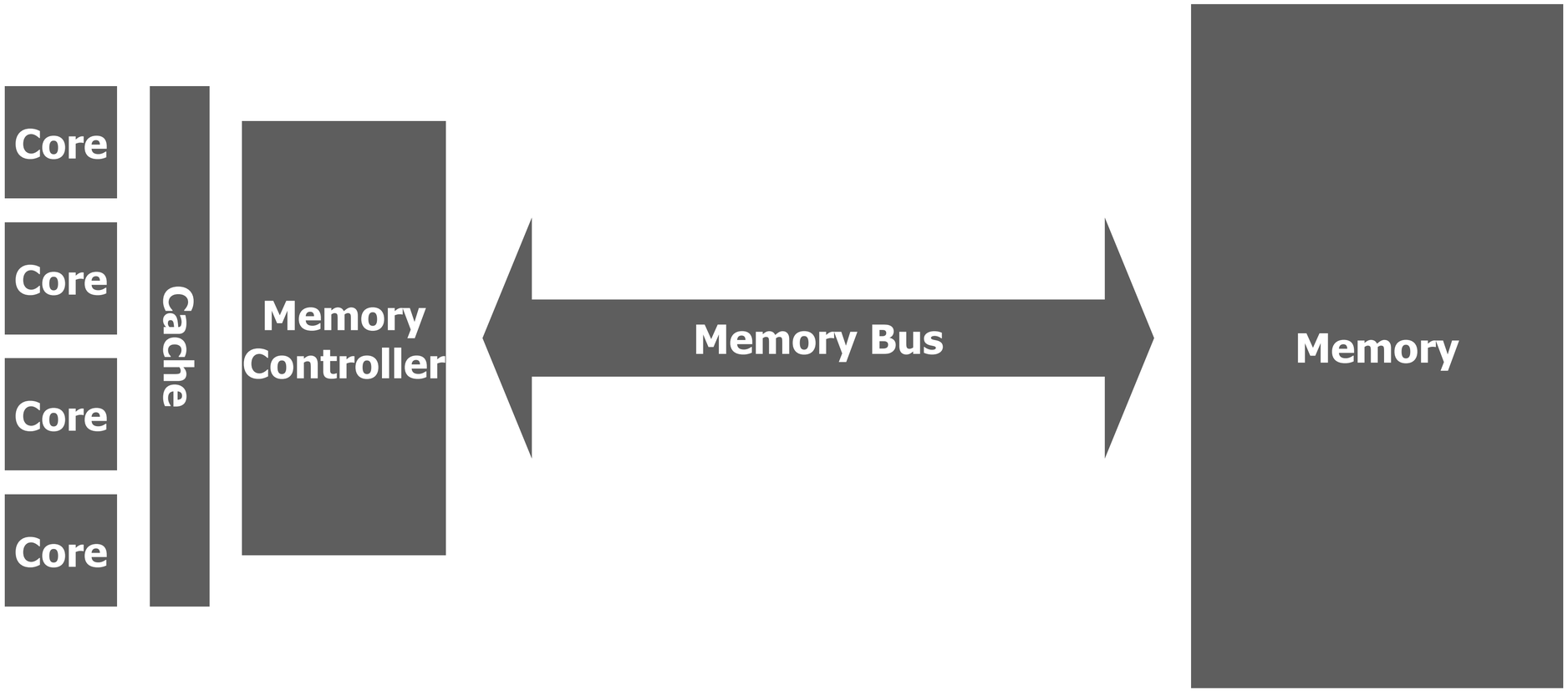

Scalability Issue

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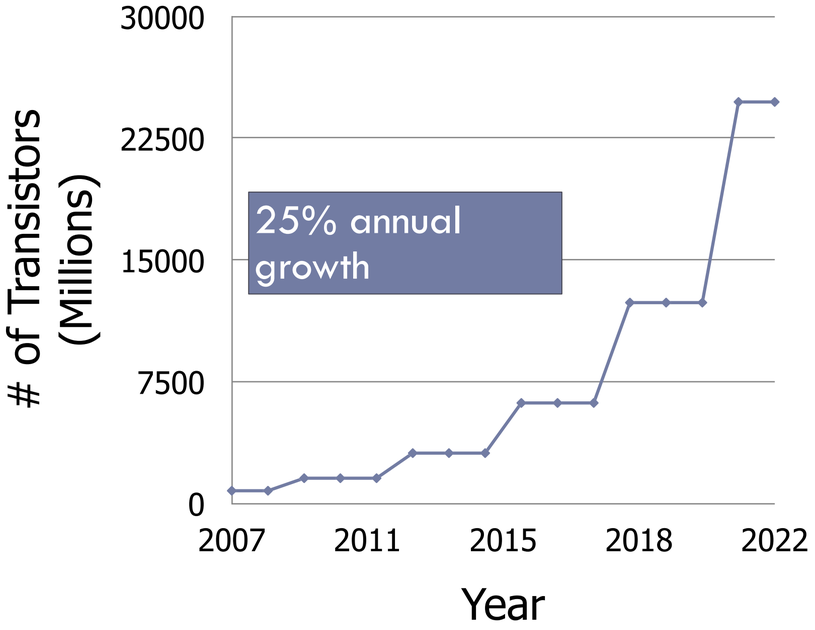
In practice only a fraction of the bandwidth can be used

Transistor Count



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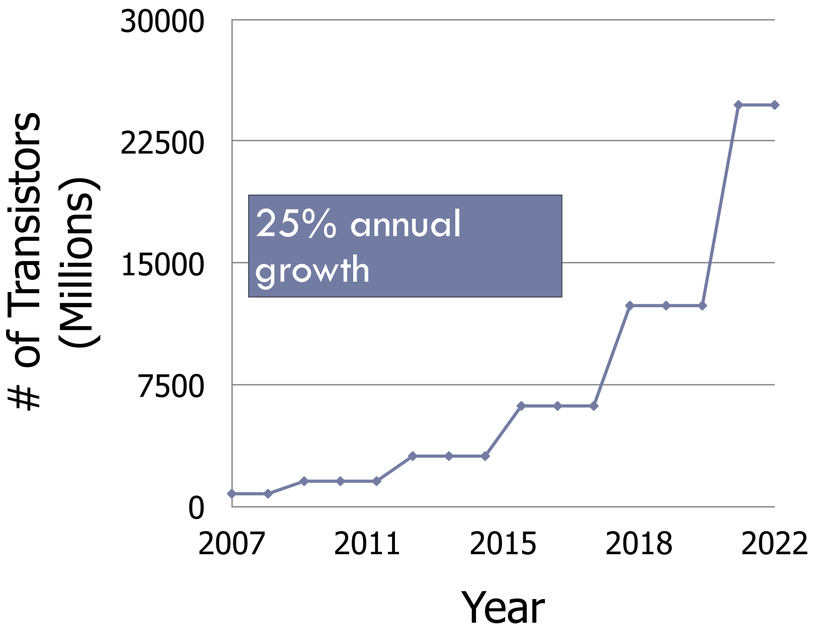

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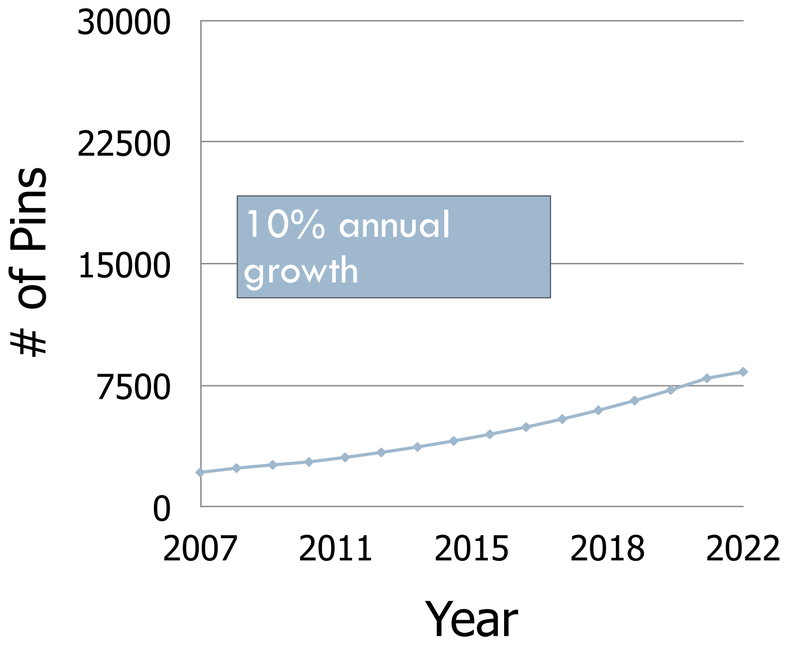

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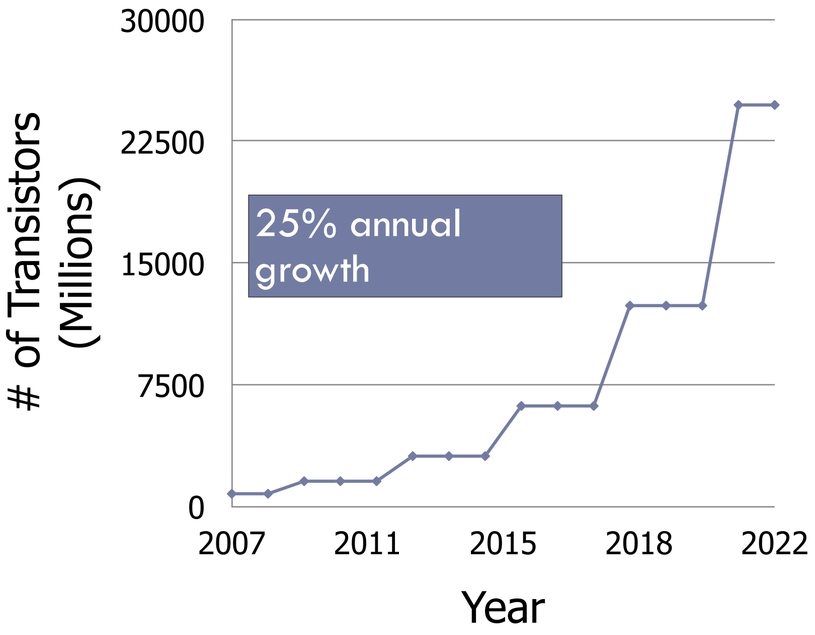

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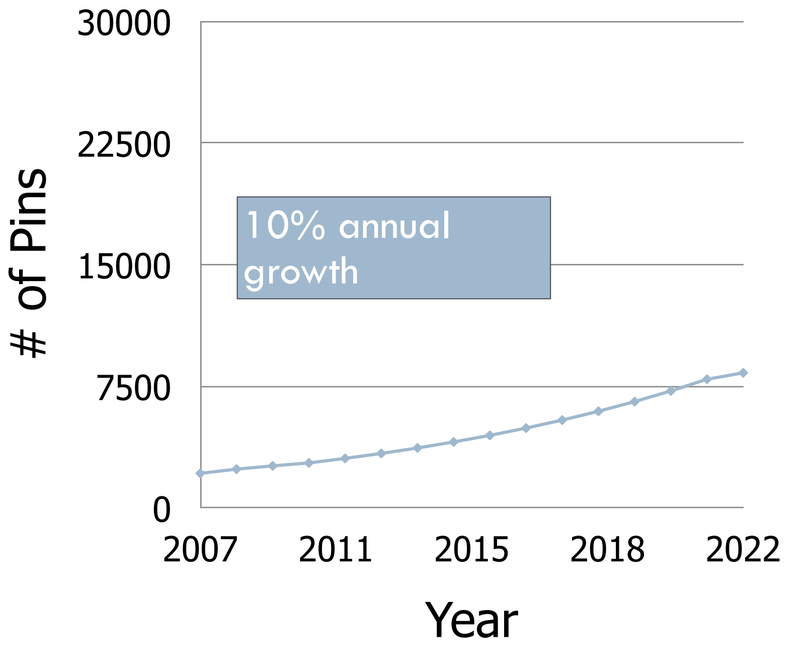

Memory bandwidth, dictated by the pin count, poses a bottleneck for CMP performance

ITRS 2007 Executive Summary

Problem & Goal

Key Ideas

Novelty

Mechanisms & Implementation

Evaluation & Results

Main Takeaways

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State-of-the-art memory controllers deliver low performance due to their fixed, rigid access scheduling policies designed for average-case behaviour

For improvements in CMP architectures, off-chip bandwidth of the memory bus presents a serious impediment to its scalability

DRAM scheduling is a complex problem, as workloads demand differing scheduling policies

Goal: Improve Performance of off-chip bandwidth by designing a better memory controller.

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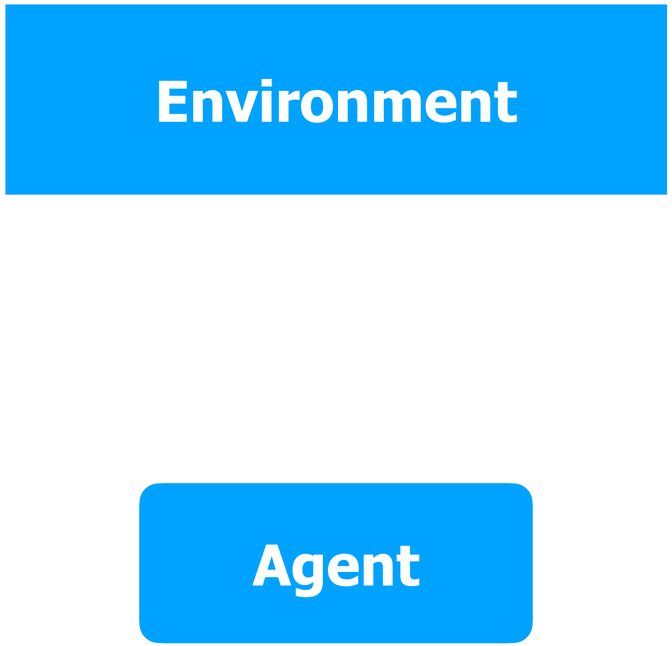
Reinforcement Learning as a self-optimizing agent maps to a flexible, self-optimizing scheduler

Make memory scheduling easier and more efficient

Allows for flexible scheduling in multiple different workloads

Reinforcement Learning



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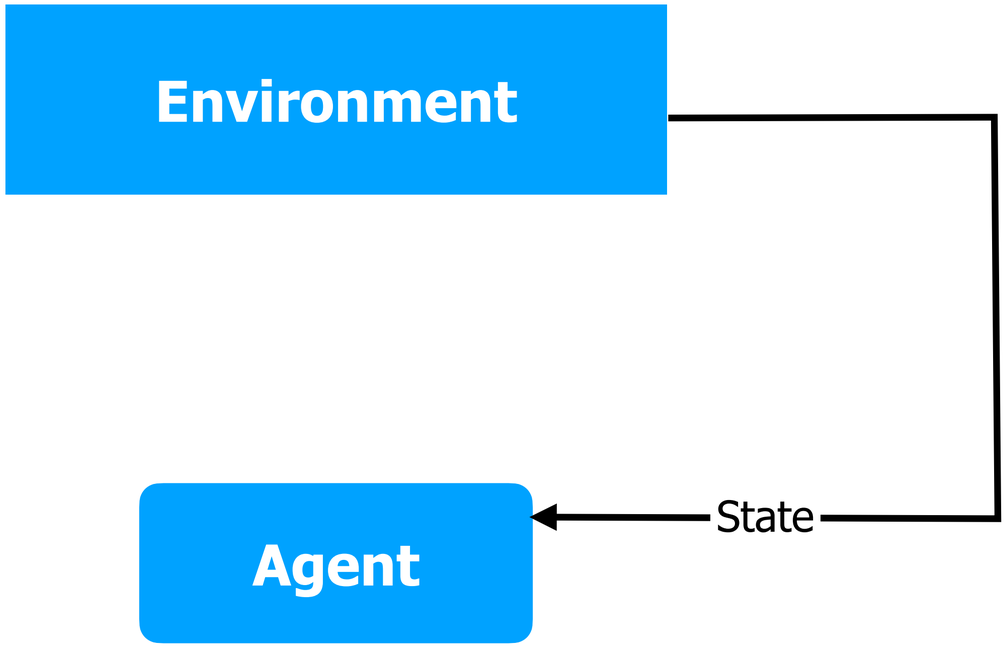

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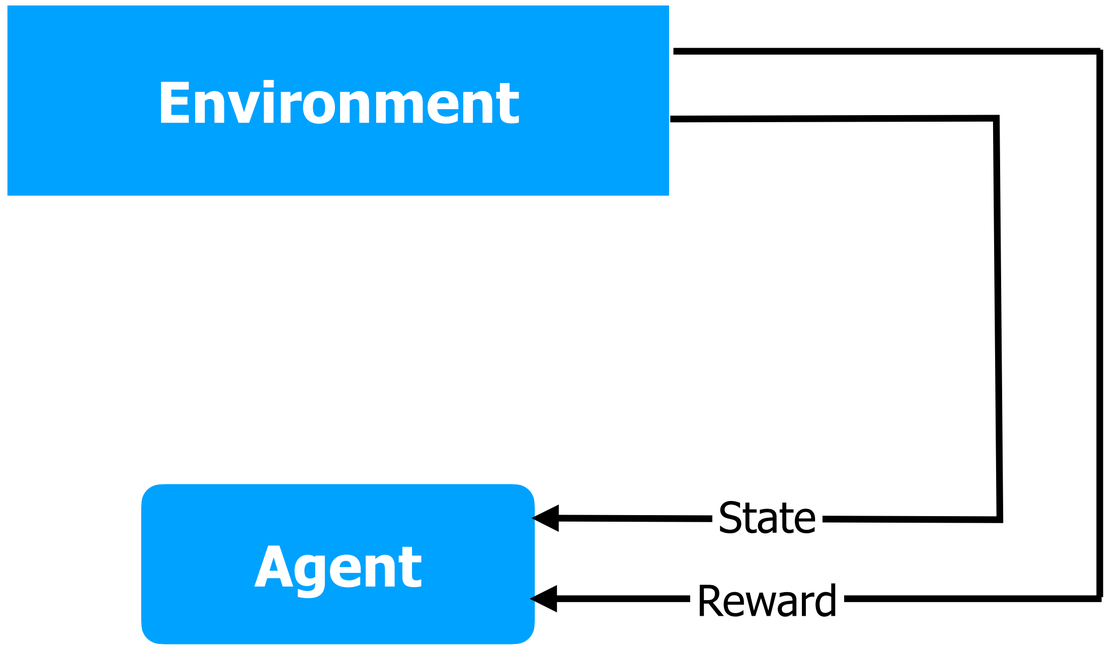

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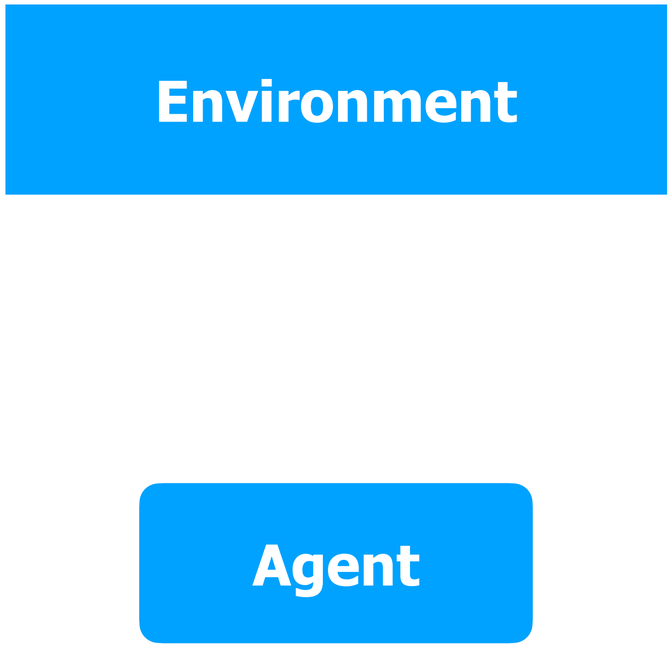

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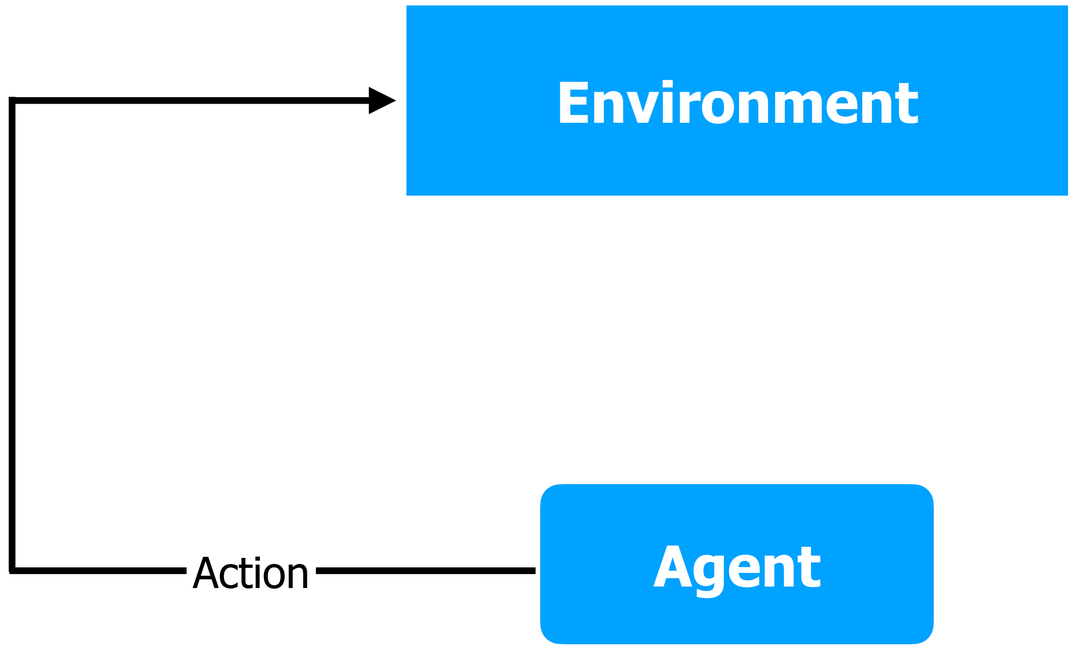

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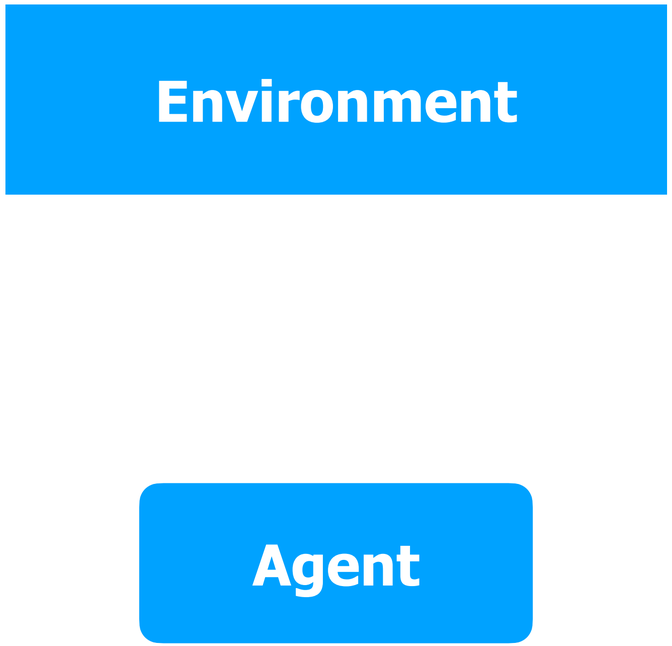

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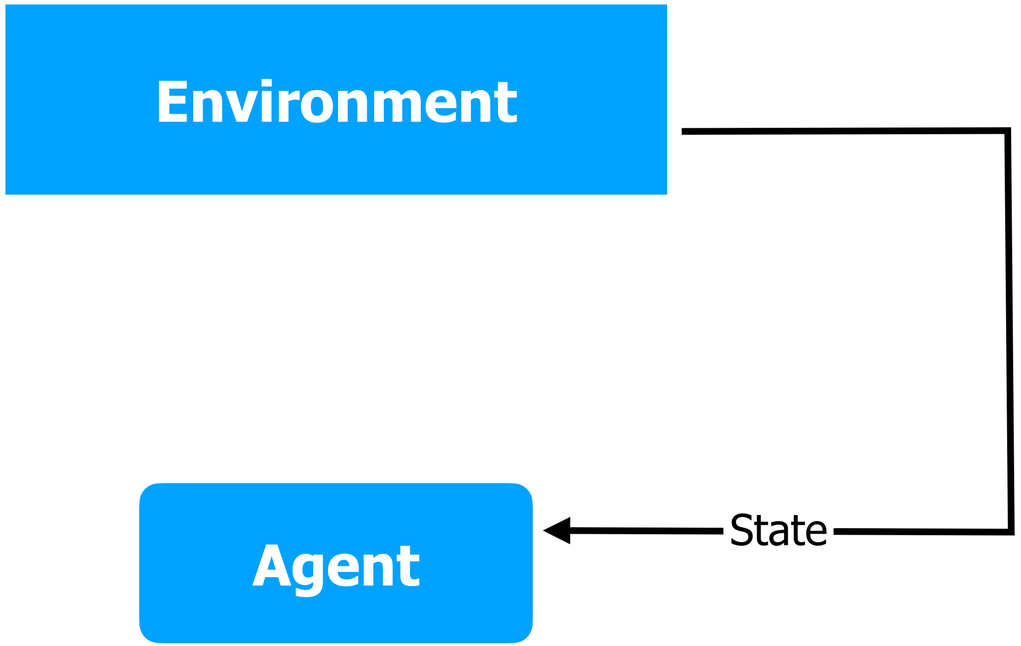

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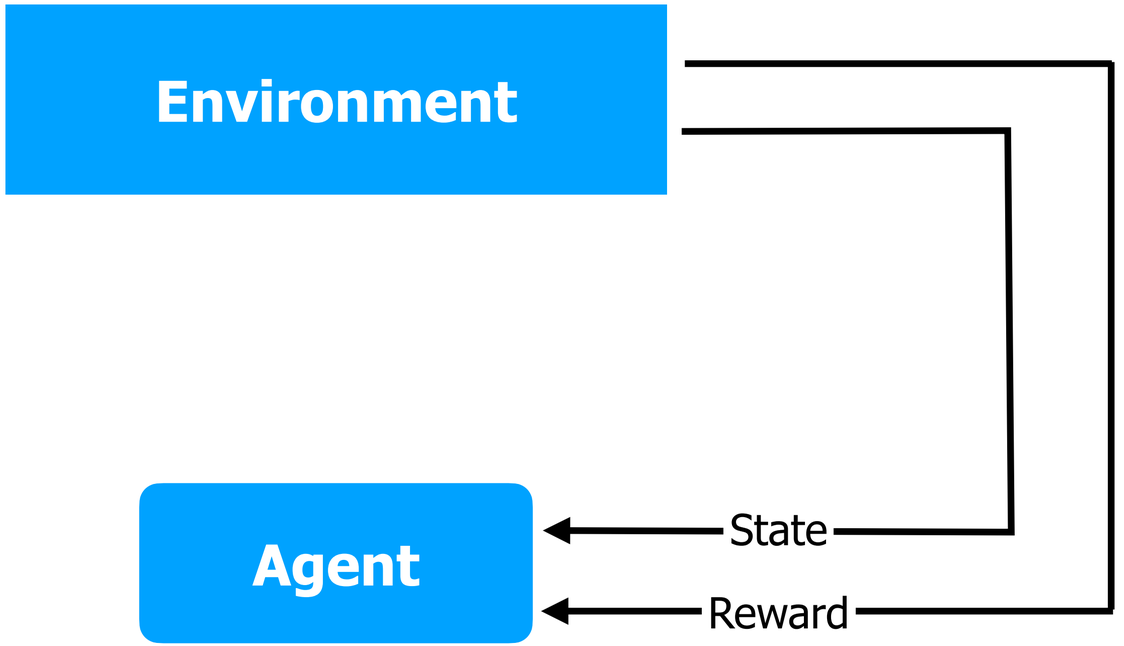

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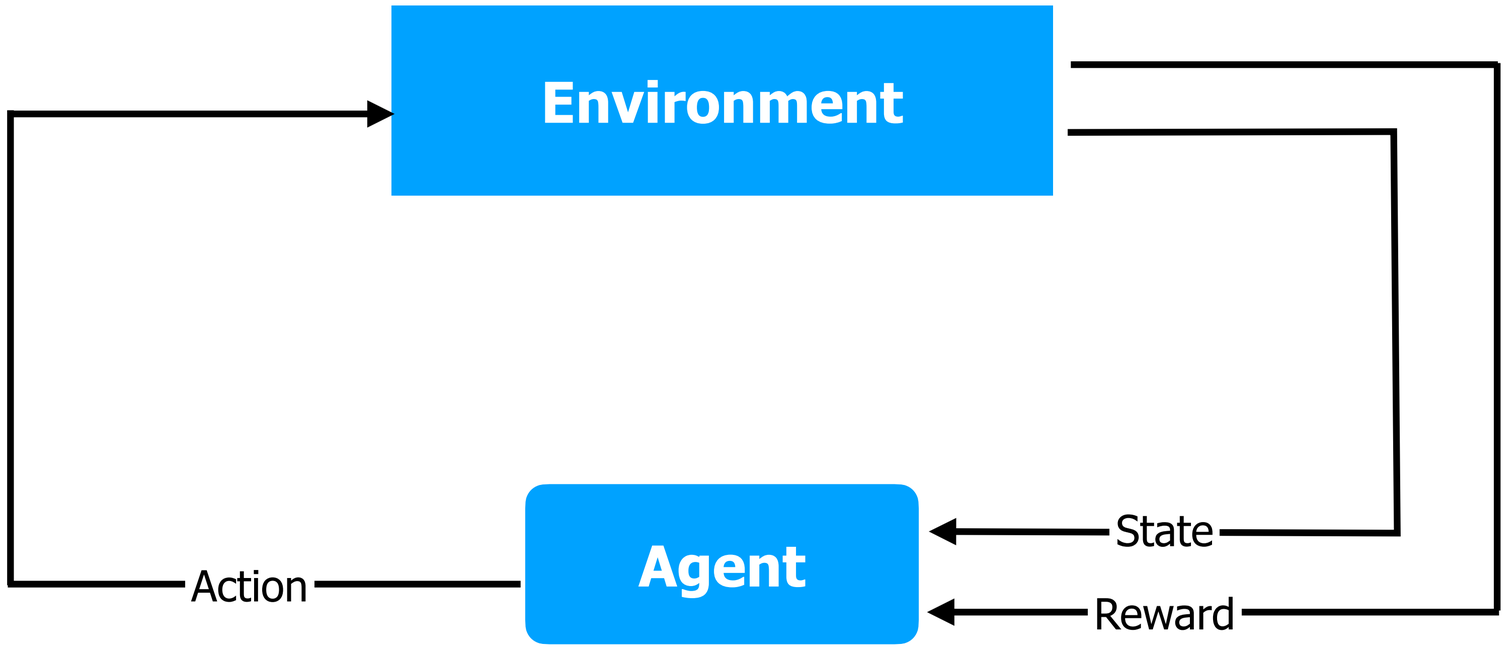

Applicability to Memory Controllers

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RL applies well to Memory Controller design

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Easy translation of Environment, Agent, Action, Reward, and State to System, Scheduler, Command, Bus Utilization, and State Attributes

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Key Idea: Design the memory controller as an RL agent whose goal is to learn an optimal memory scheduling policy via interaction with the system

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System

Scheduler

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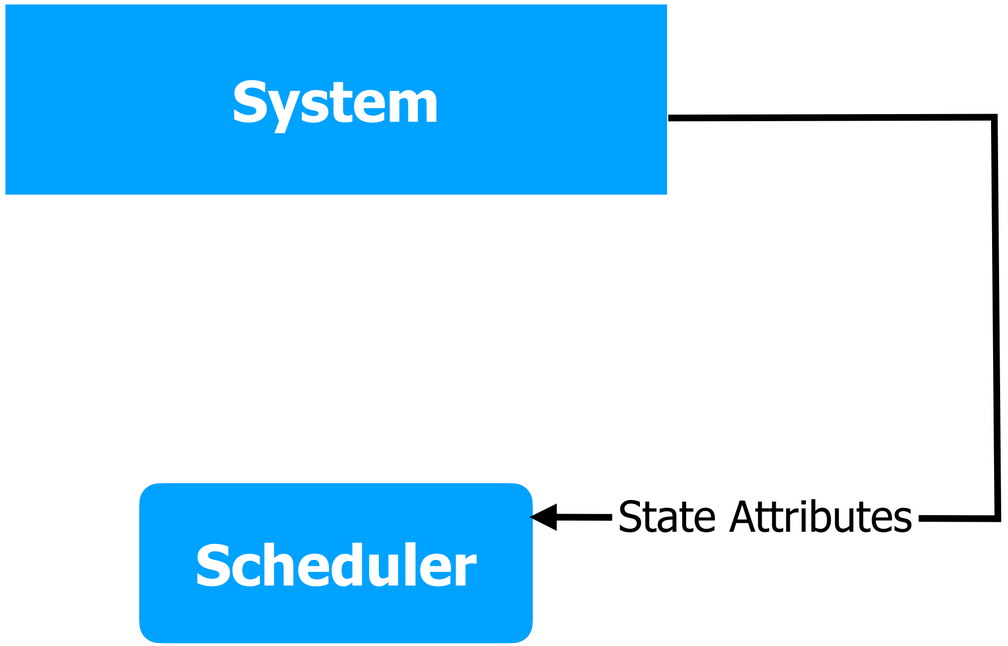

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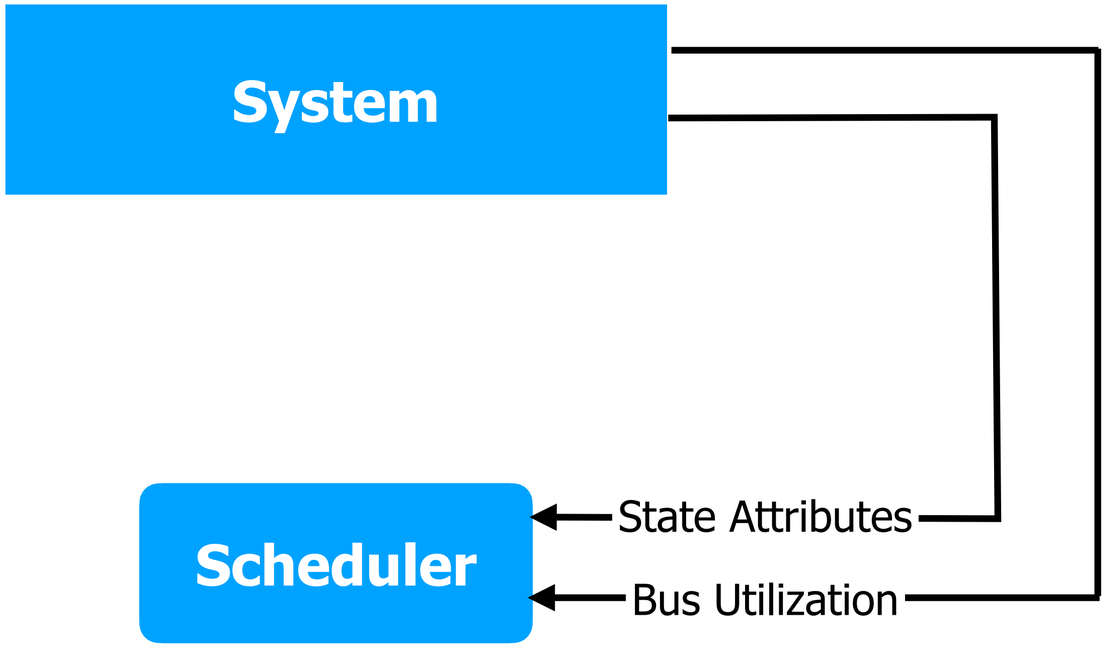

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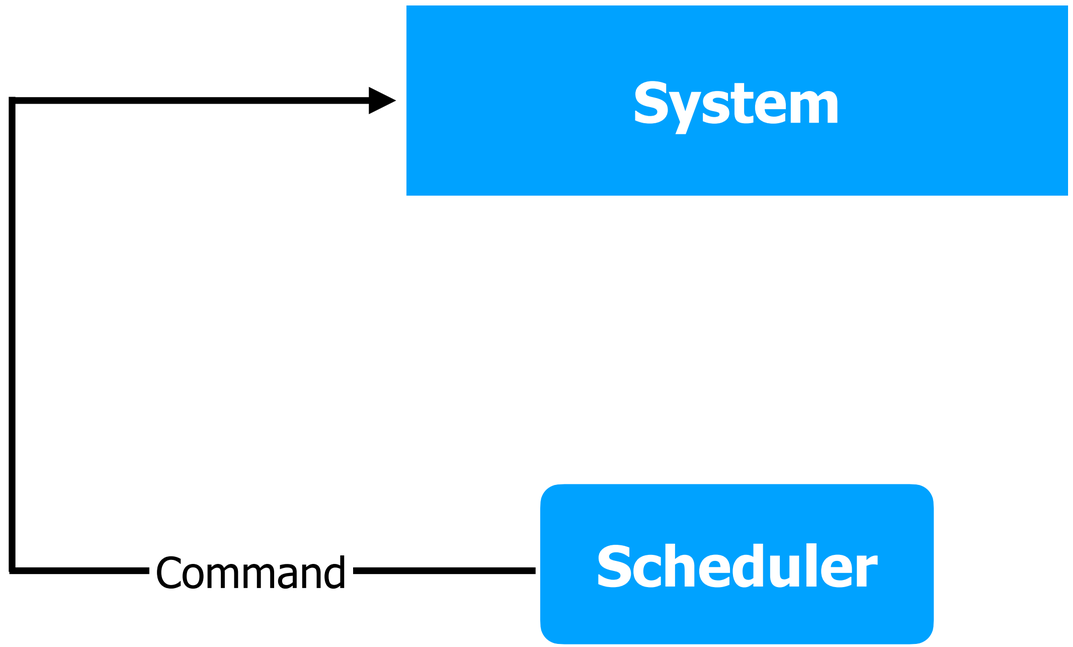

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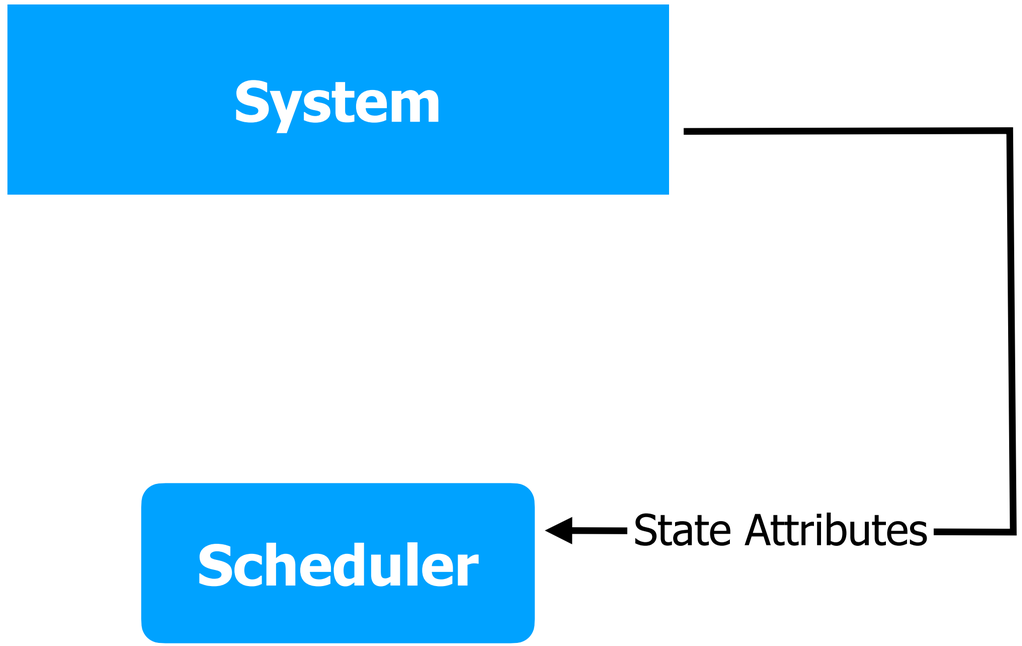

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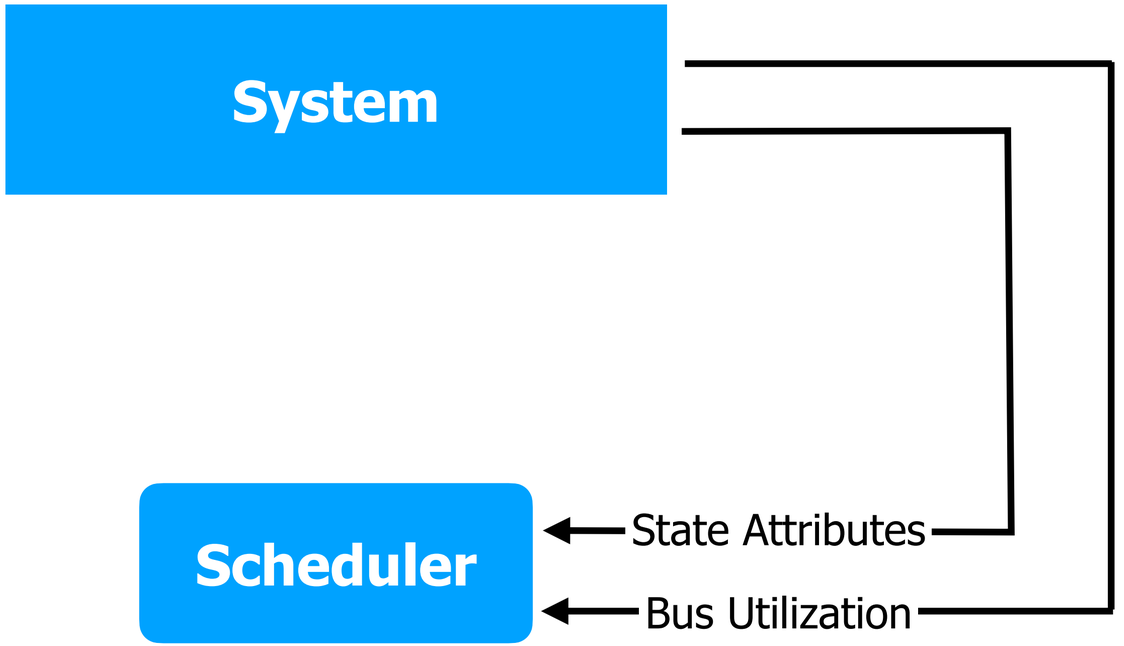

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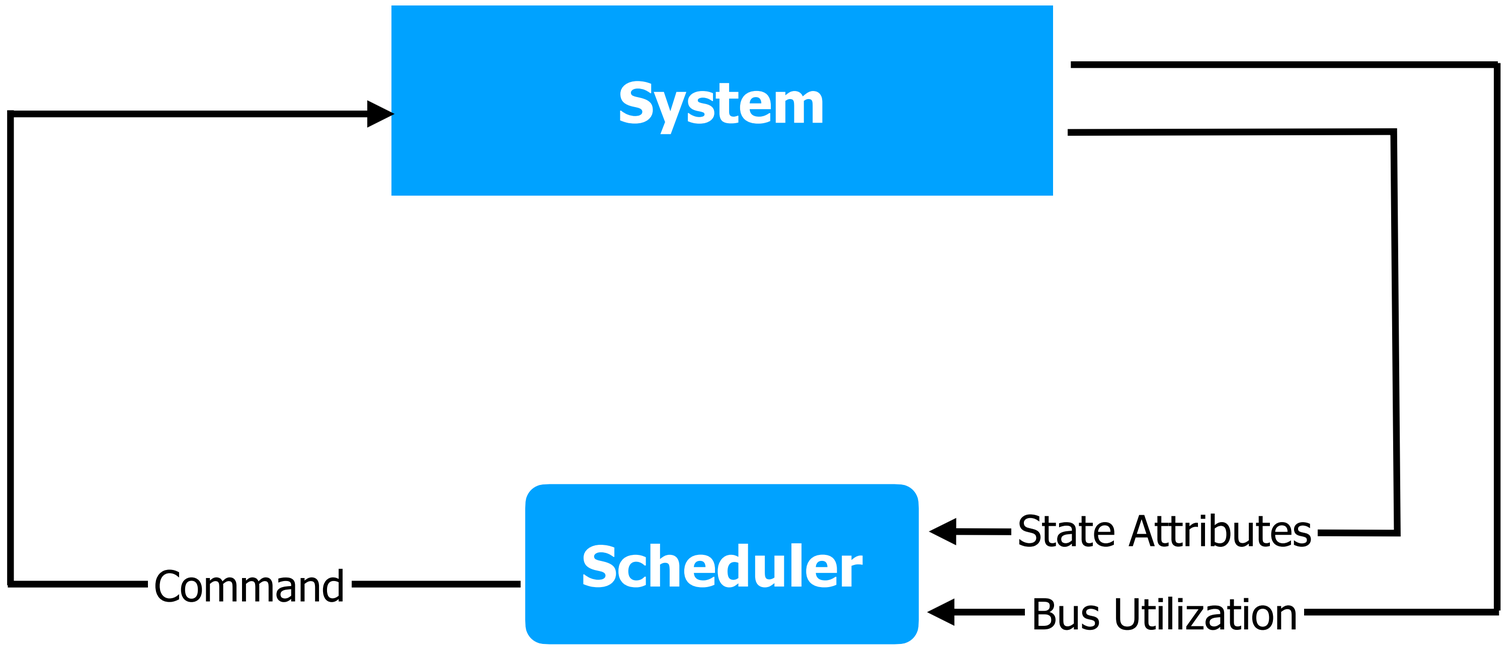

Challenges [1/2]

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Exploration vs Exploitation: Agent must explore the environment enough to be able to make good decisions (exploration), but also follow and exploit a found strategy (exploitation)

Challenges [1/2]

Temporal Credit Assignment: Agent must be able to anticipate long-term consequences of its actions

Exploration vs Exploitation: Agent must explore the environment enough to be able to make good decisions (exploration), but also follow and exploit a found strategy (exploitation)

Generalization: Agent must be able to generalize to act on such a big space of possible configurations

Challenges [2/2]

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Proposed Solution: Use dedicated hardware

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First to apply Machine Learning in memory controllers

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Current Bus Utilization is the reward for this agent

Feature Selection

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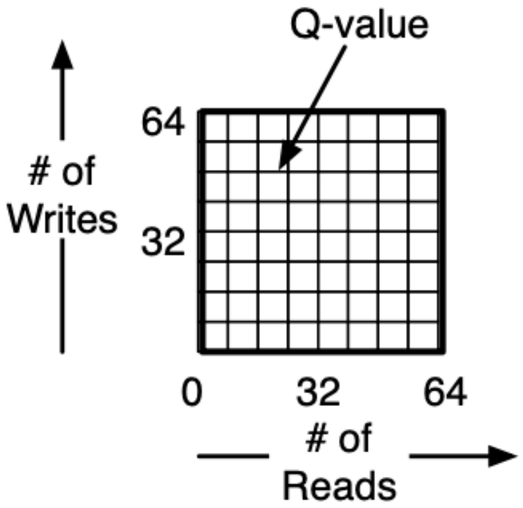
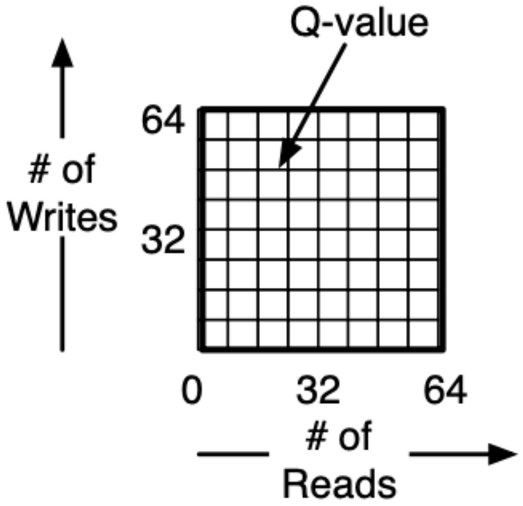
Features were selected through an automated feature selection process

Q-Values



Q-Values

Q-values approximate the cumulative long-term reward for each state action pair



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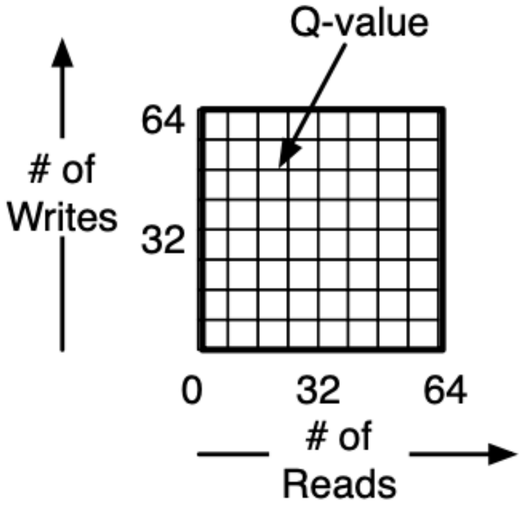

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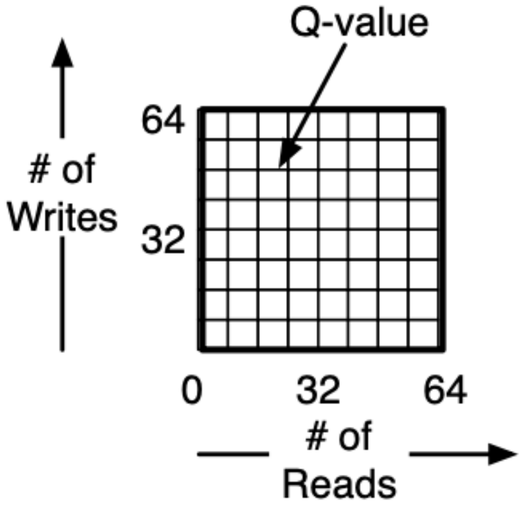

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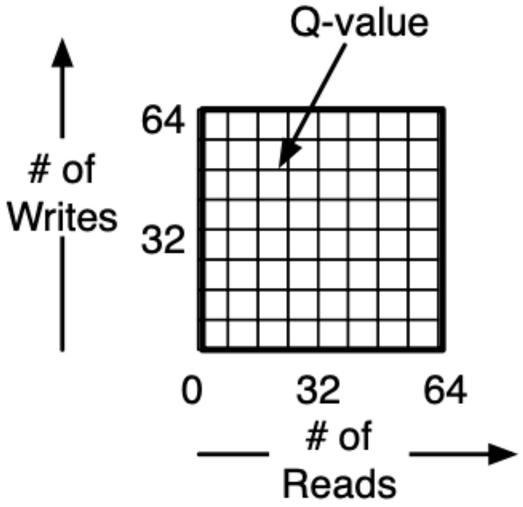

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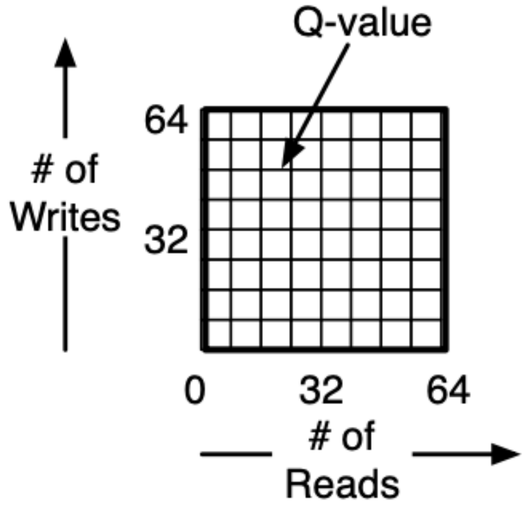

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CMAC representation is used for generalization and resolution:
Using overlapping coarse grained tables for adaptive resolution

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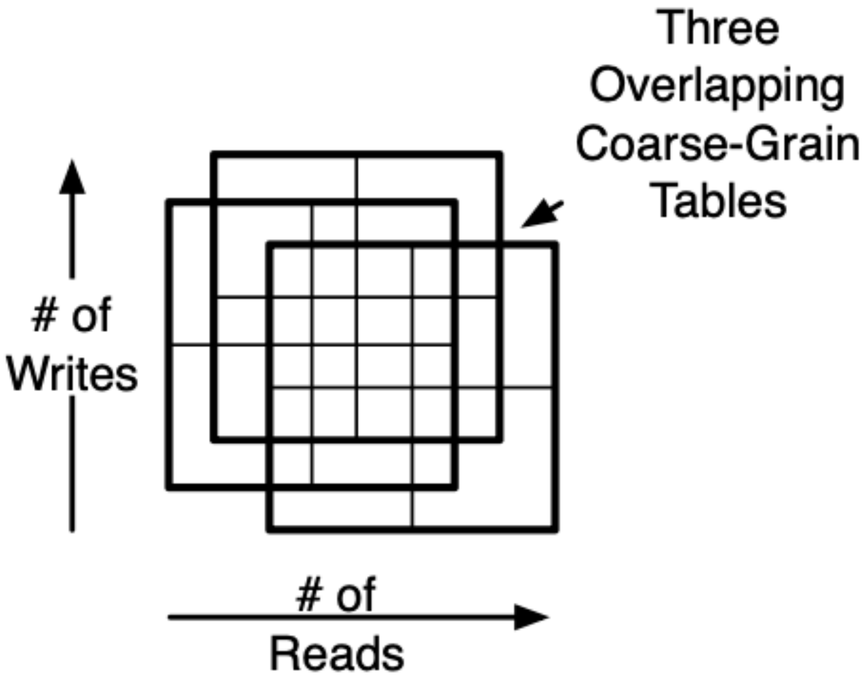

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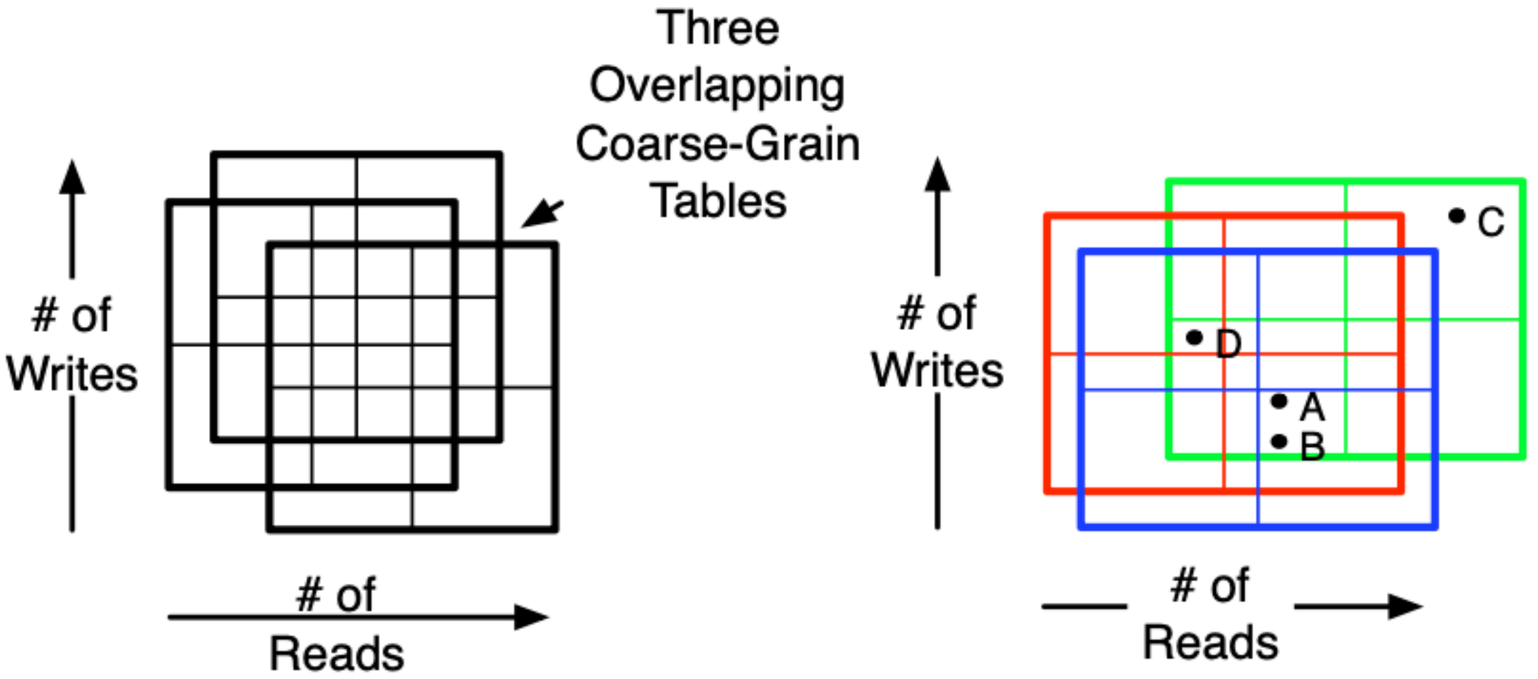

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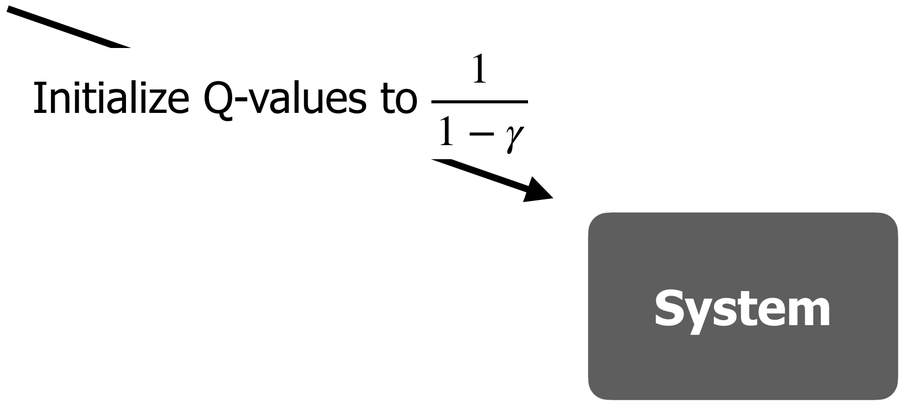

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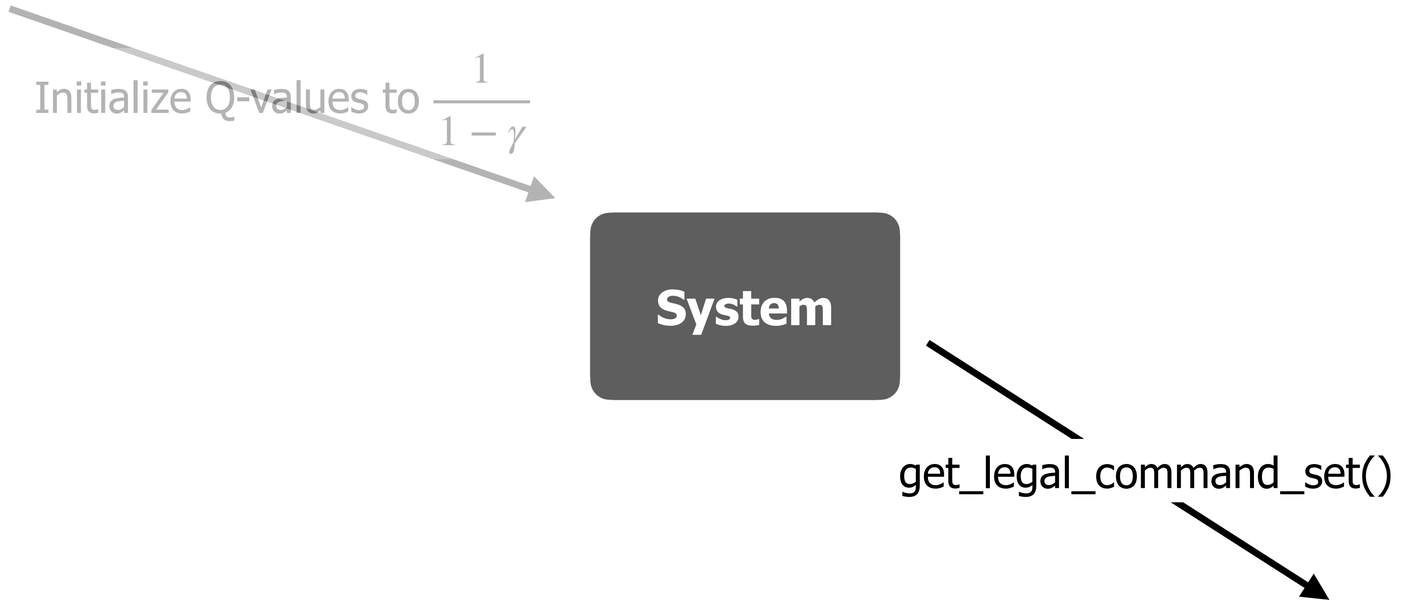

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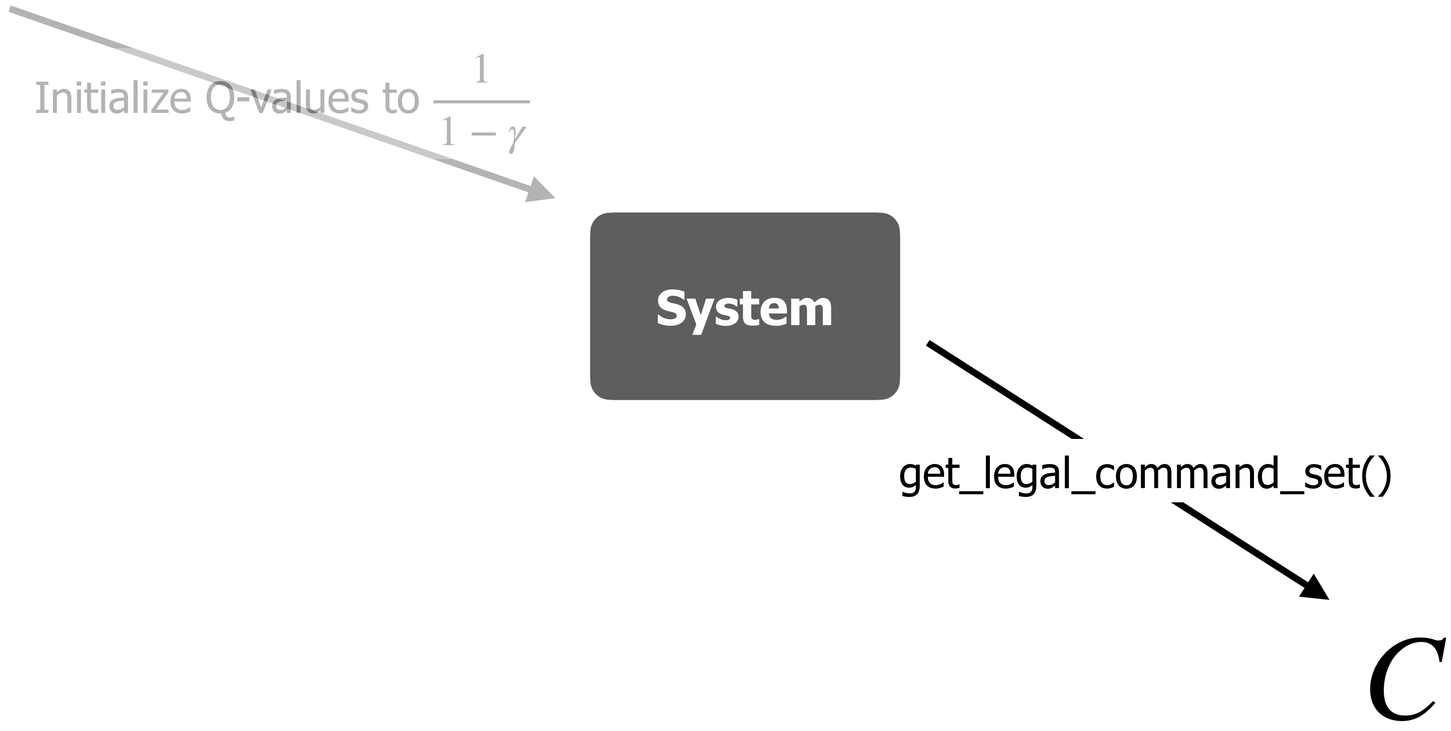

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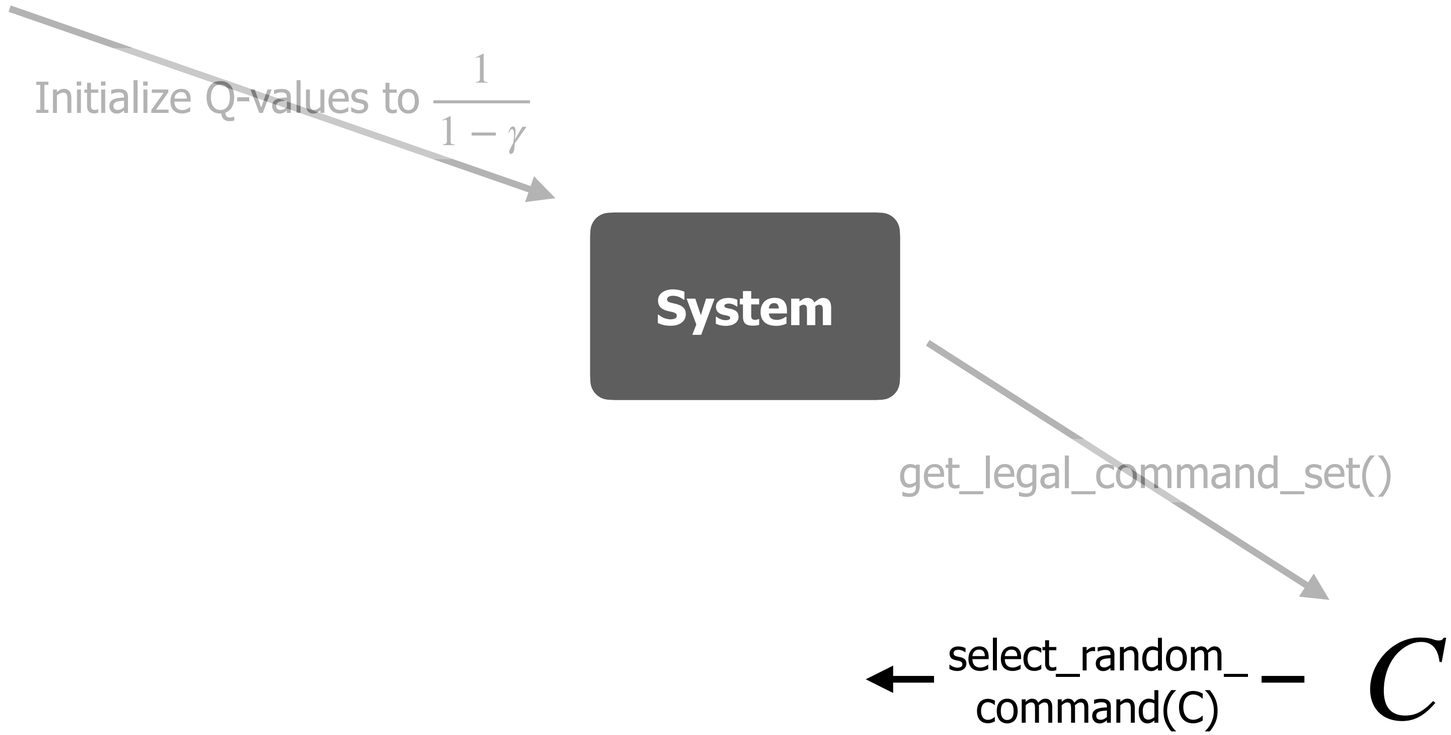

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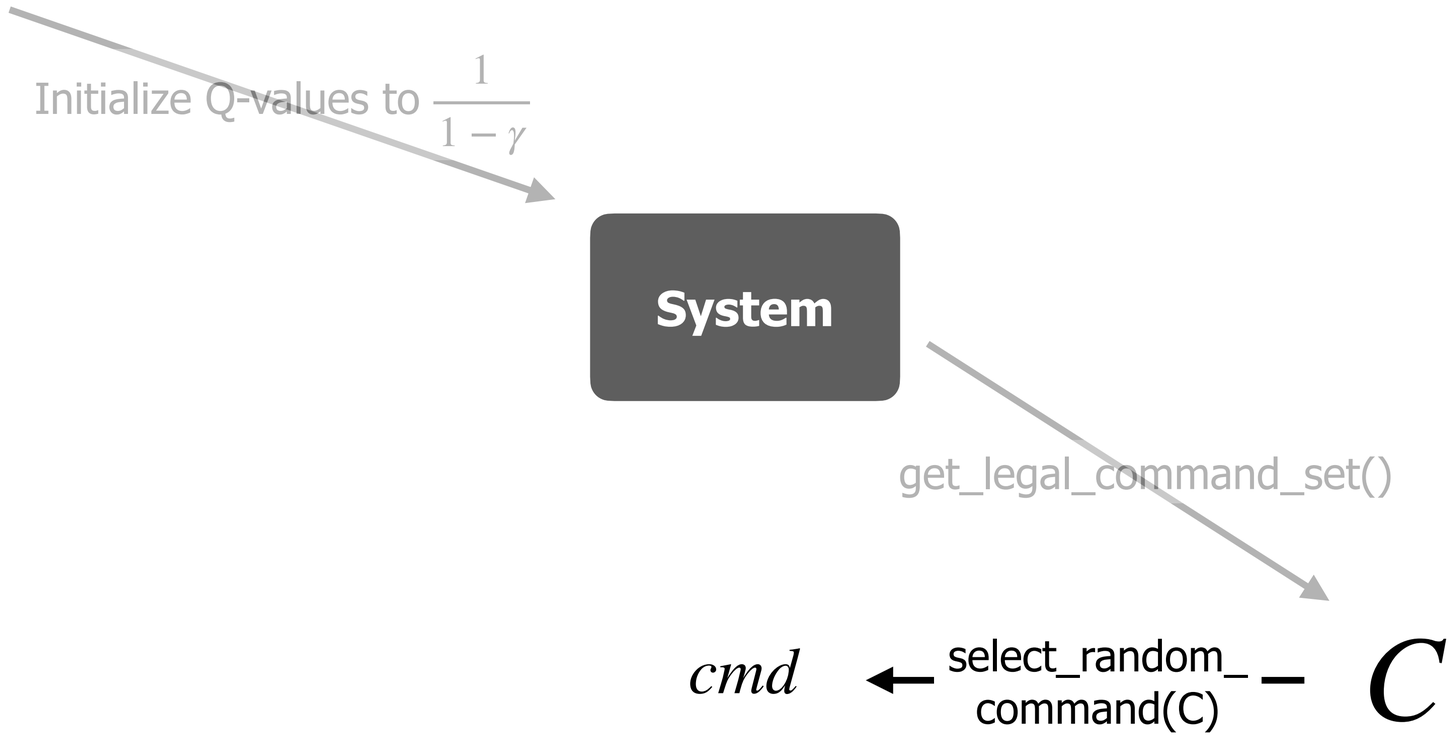

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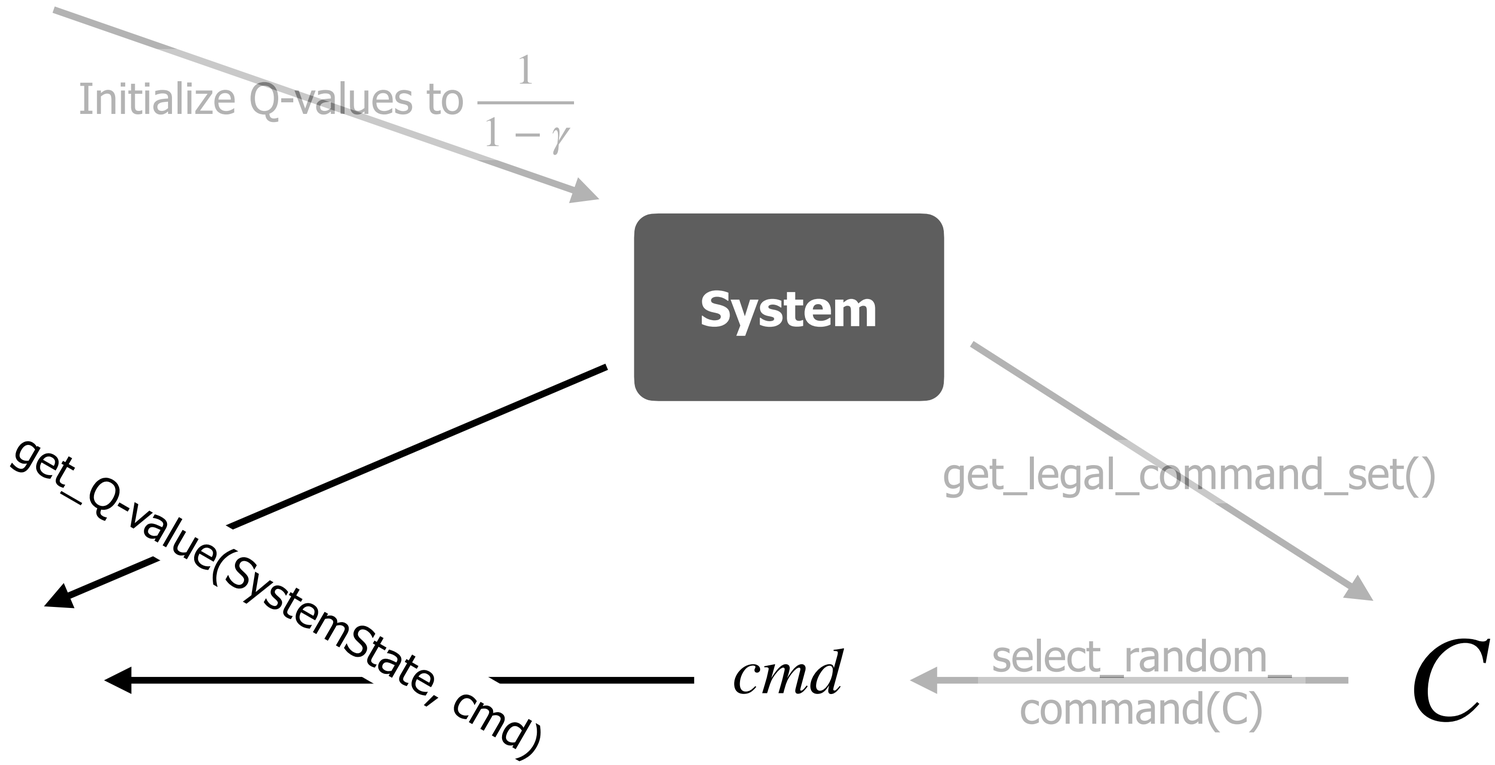

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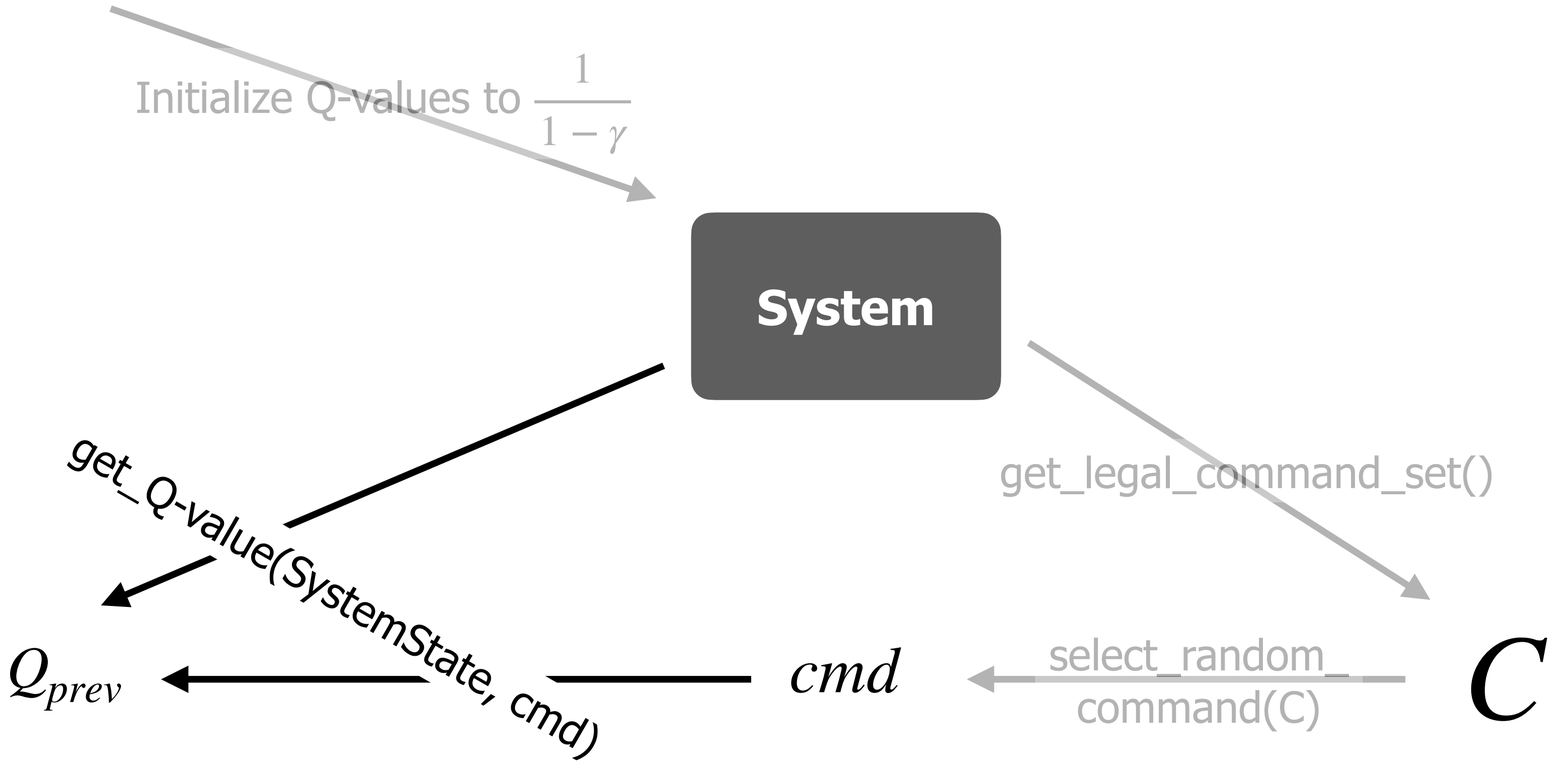

Algorithm

for all DRAM cycles

System

Q_{prev} cmd C

Algorithm

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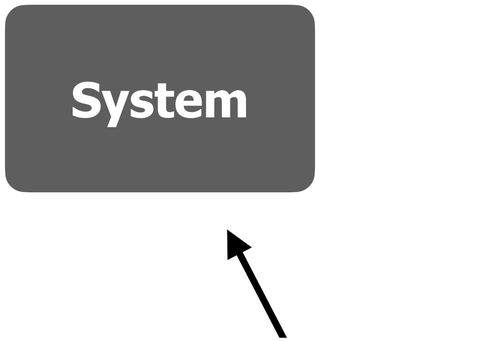

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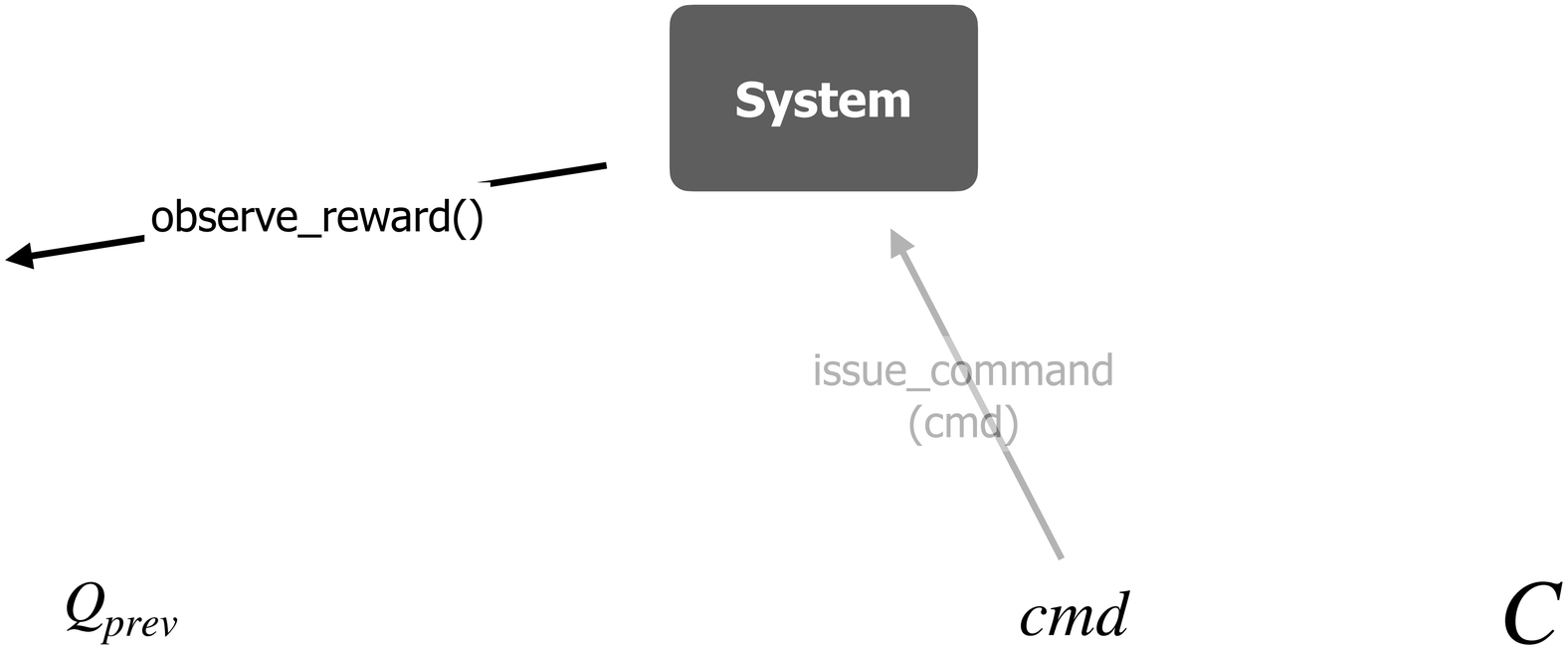

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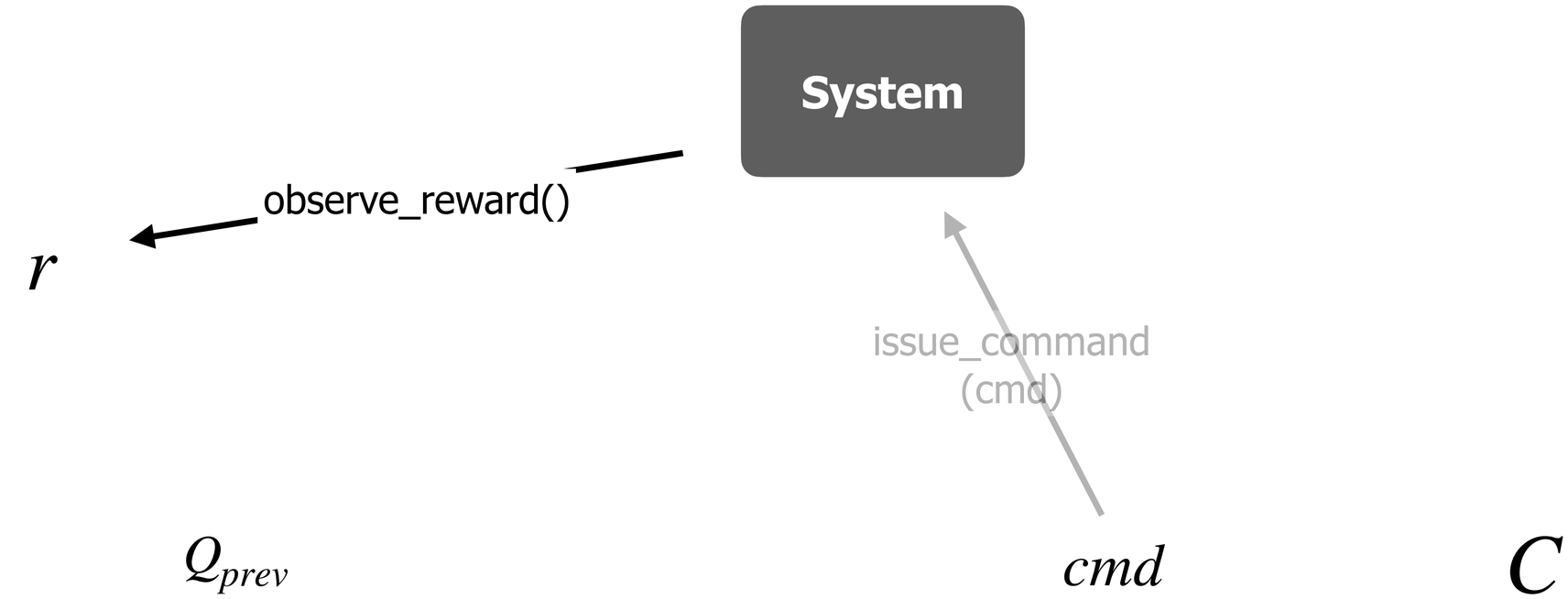

r

Q_{prev}

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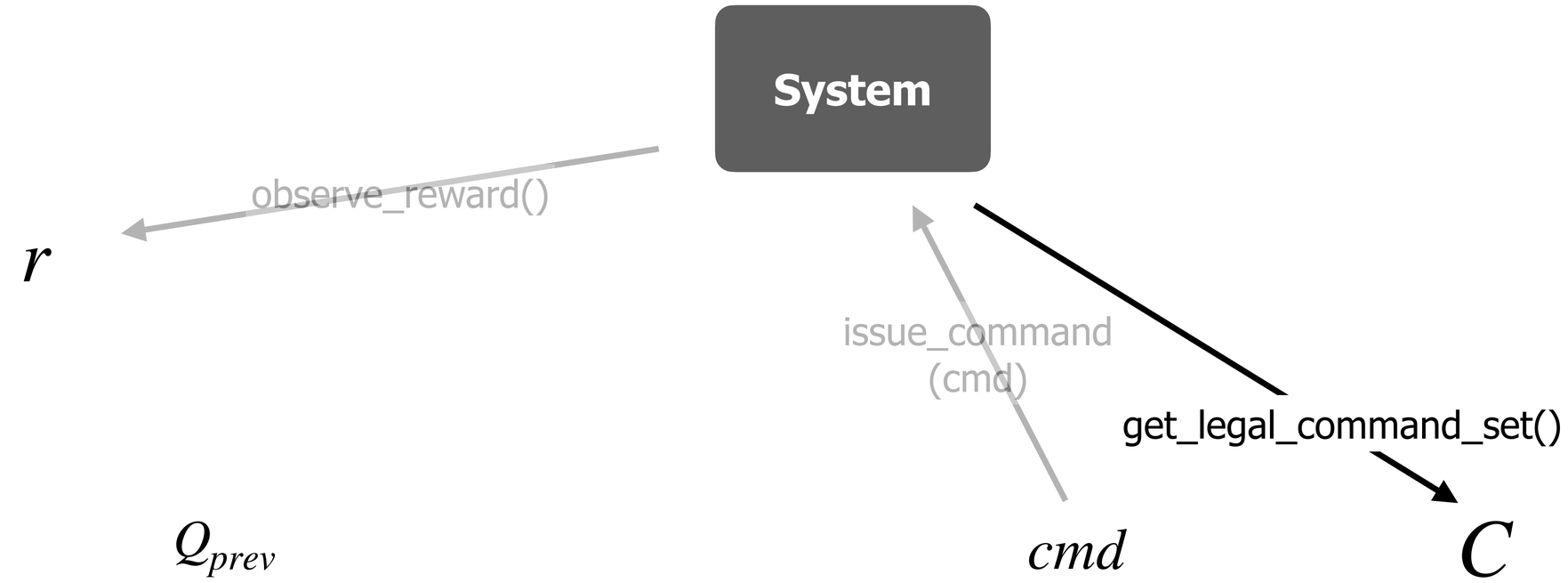

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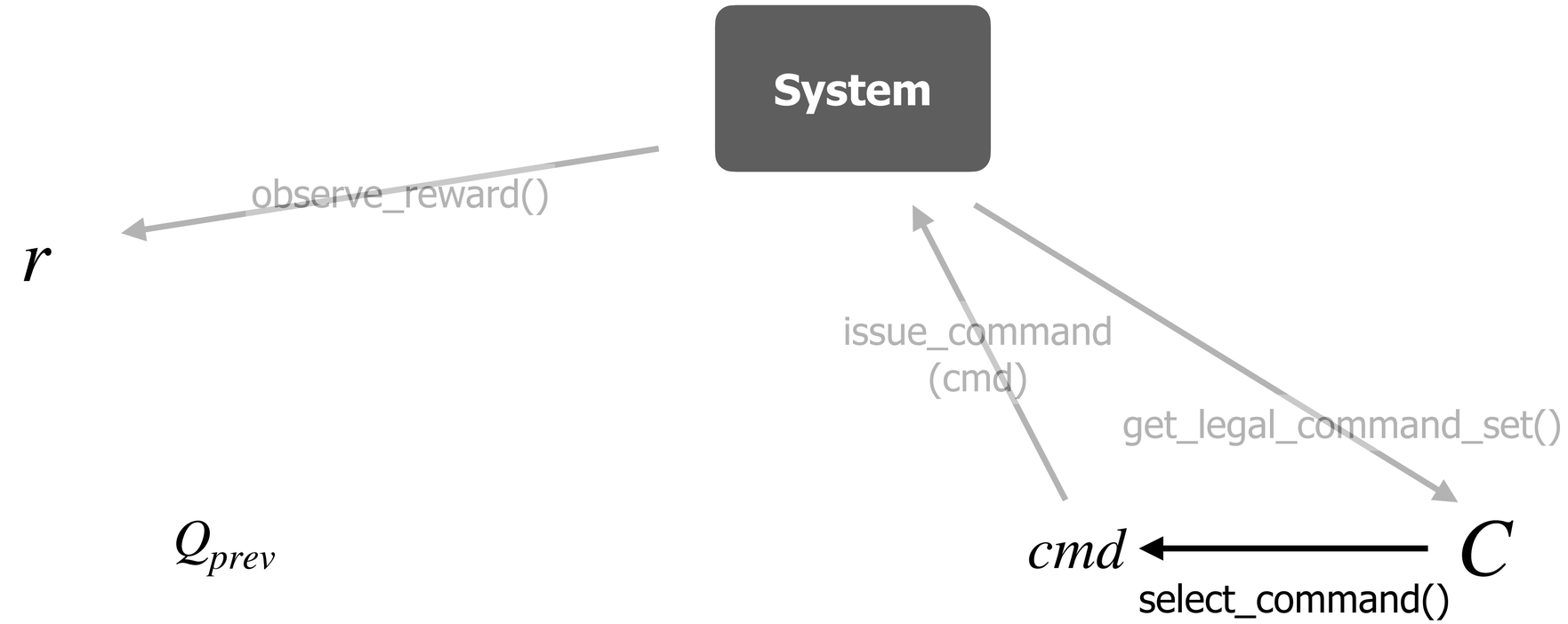

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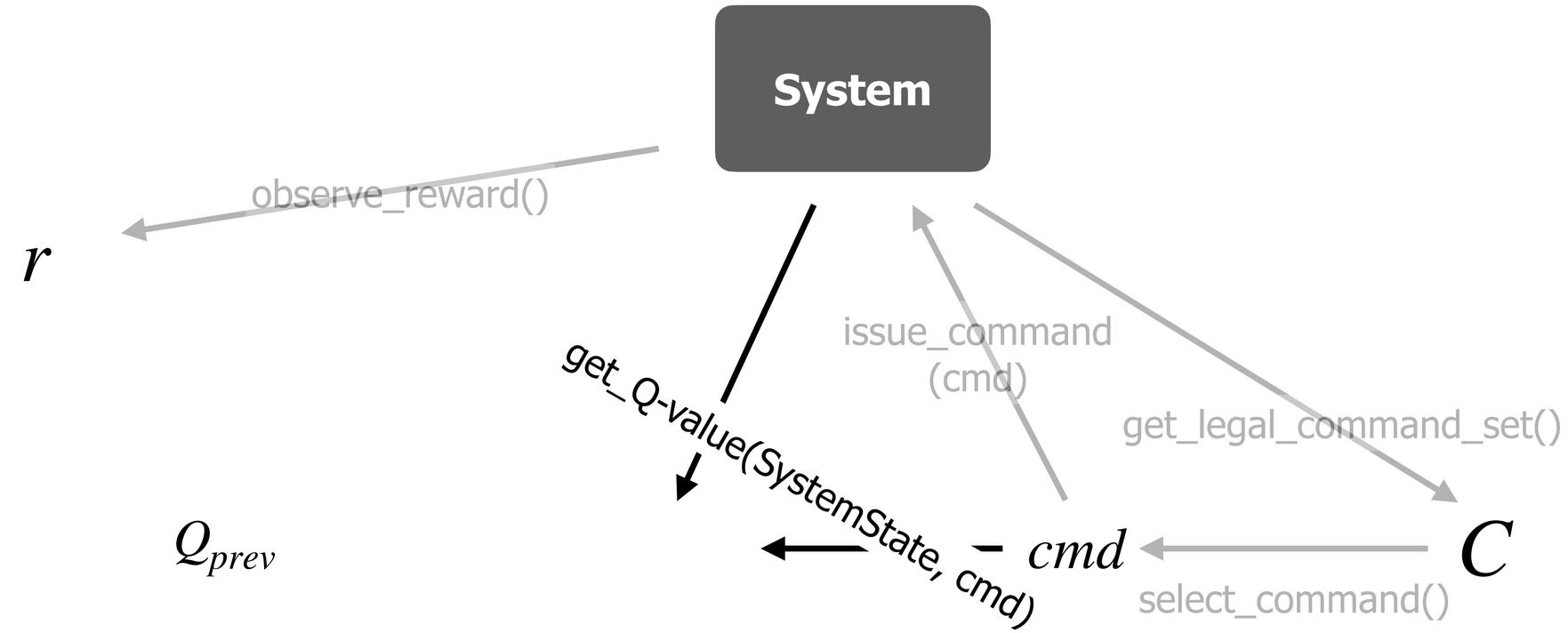

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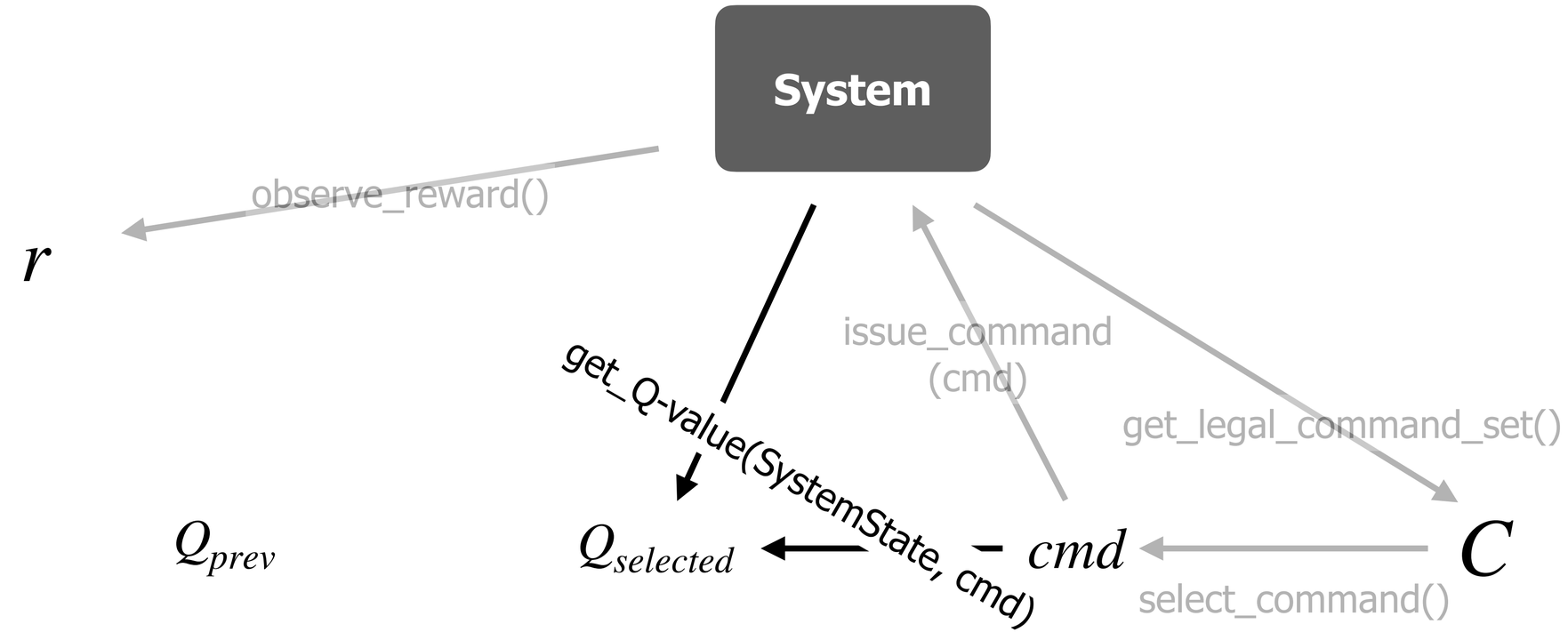

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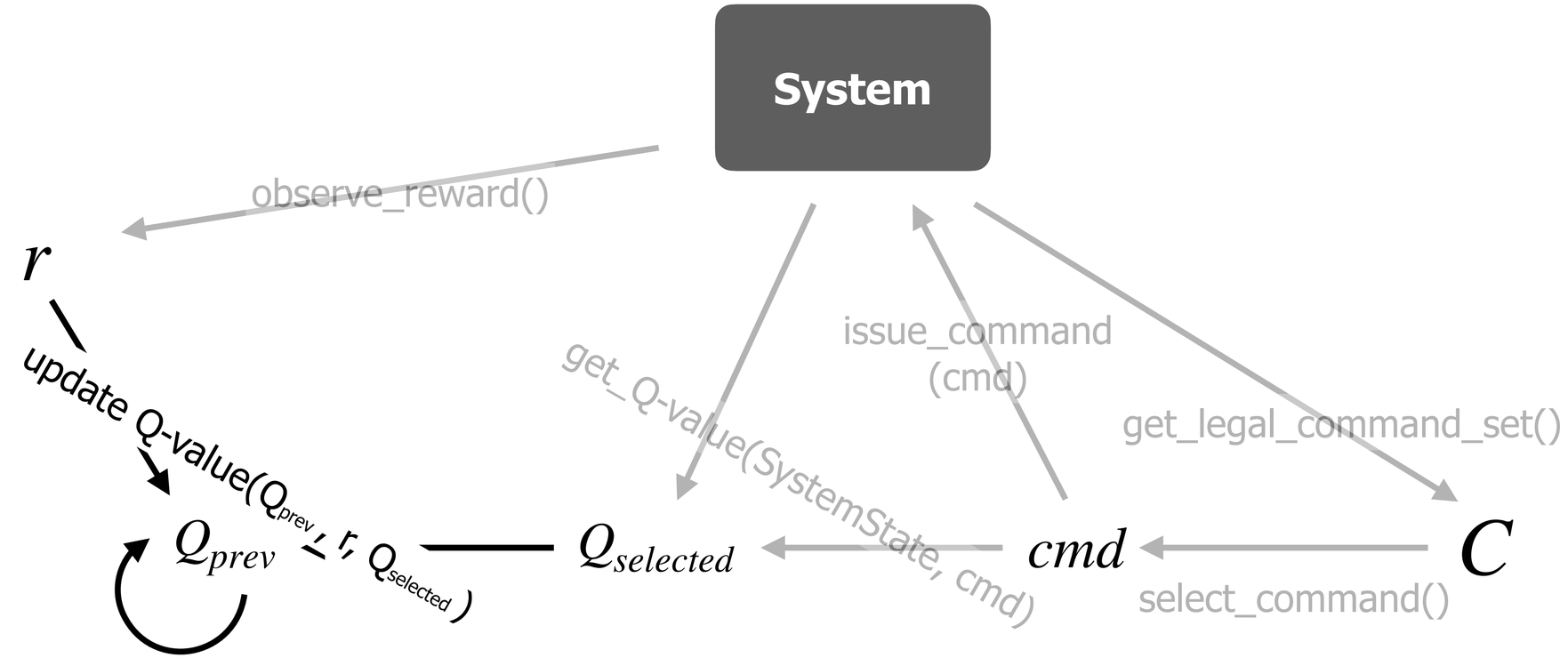

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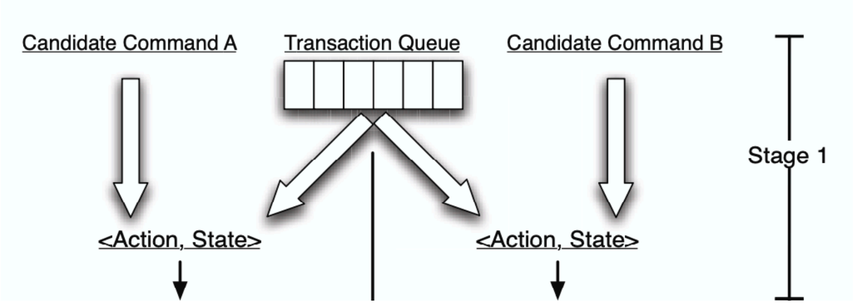

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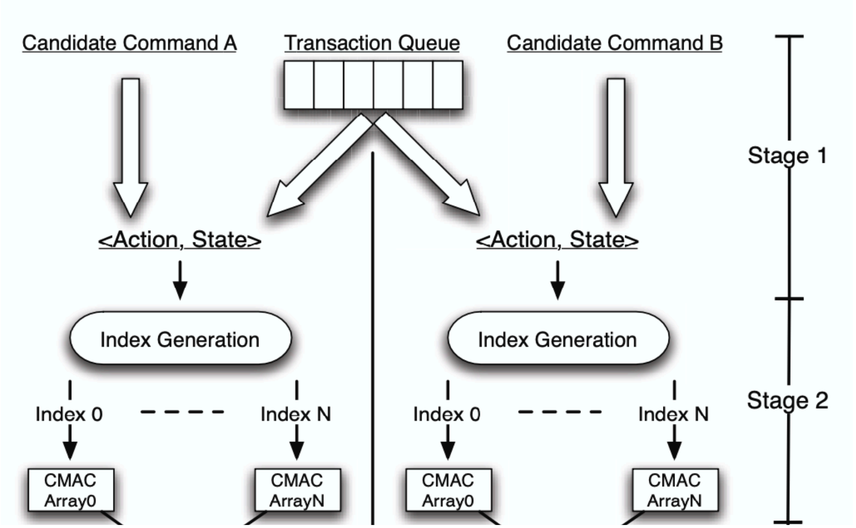

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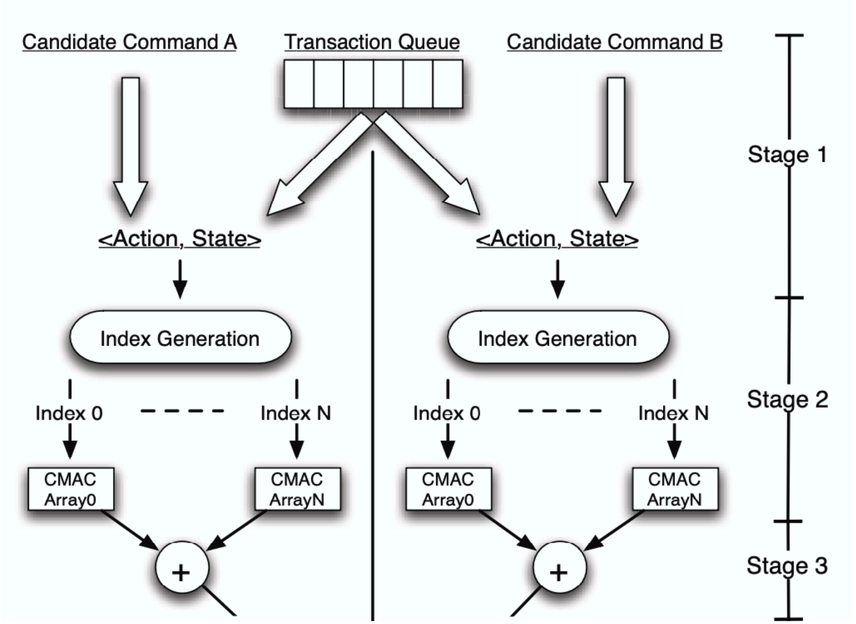

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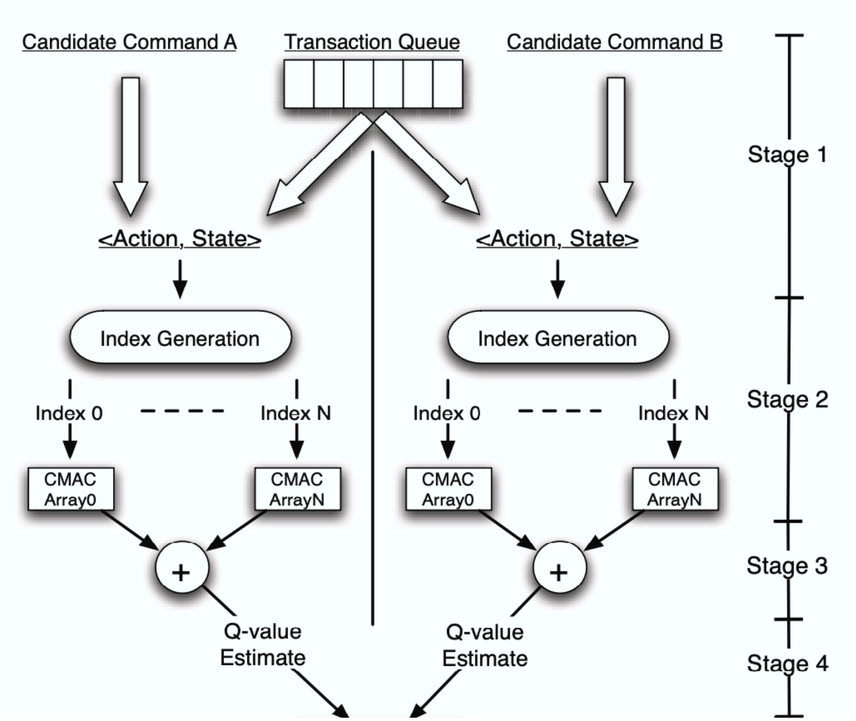

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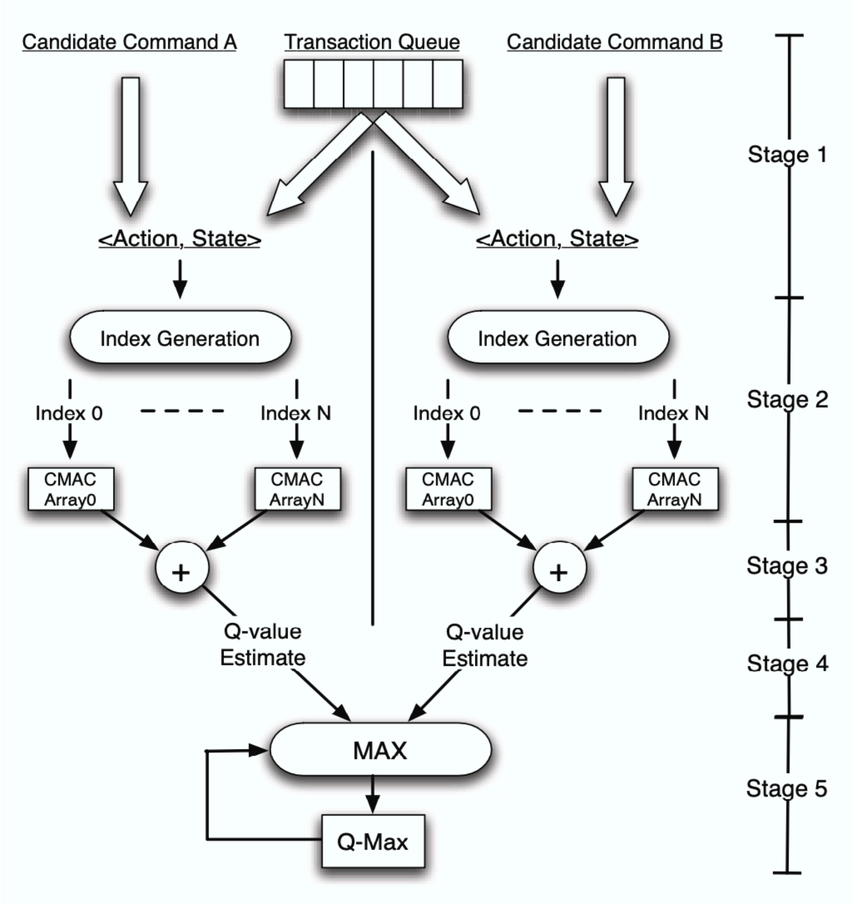

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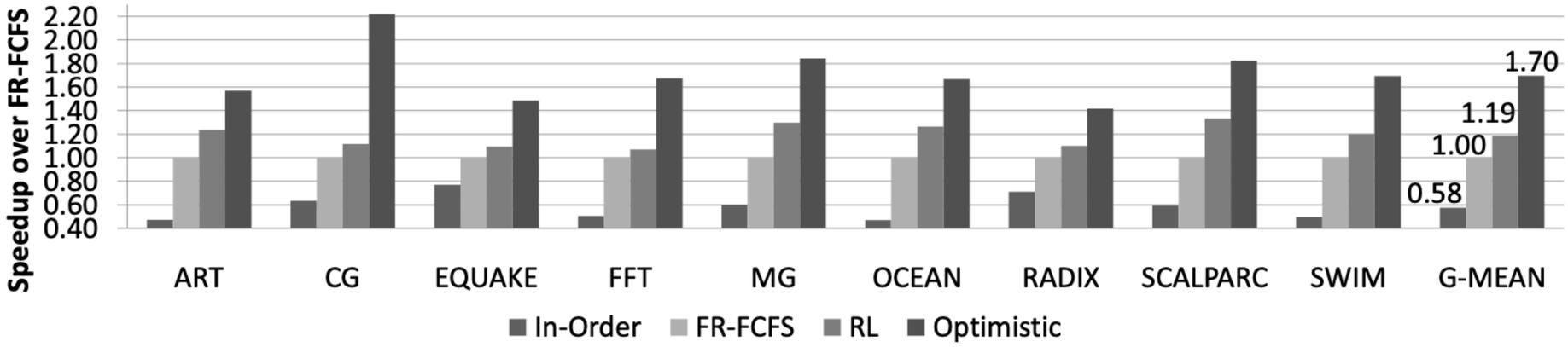
The parallel workloads were simulated on a CMP with four two-way simultaneously multithreaded (SMT) cores, 4MB of L2 cache, and a DDR2-800 memory system

Evaluation: Speedup



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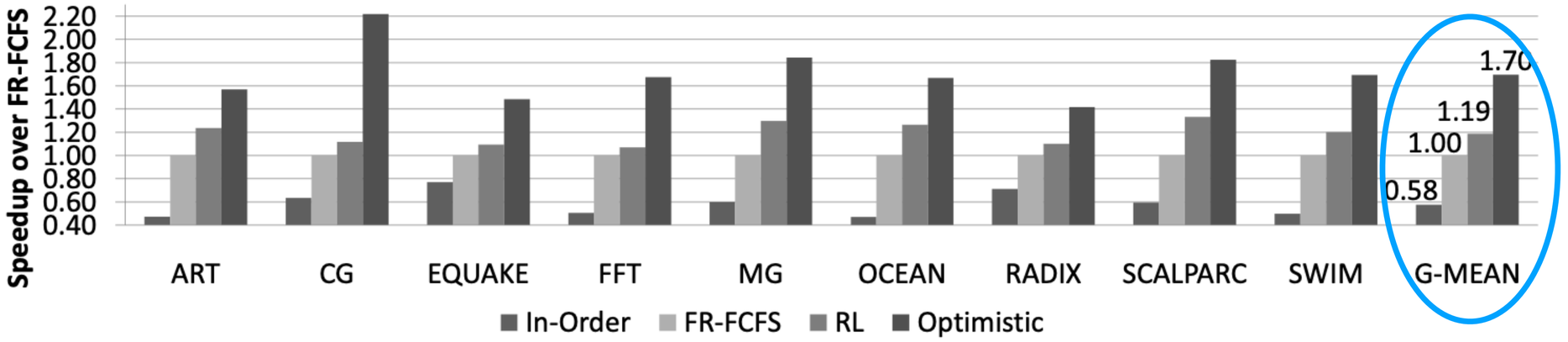

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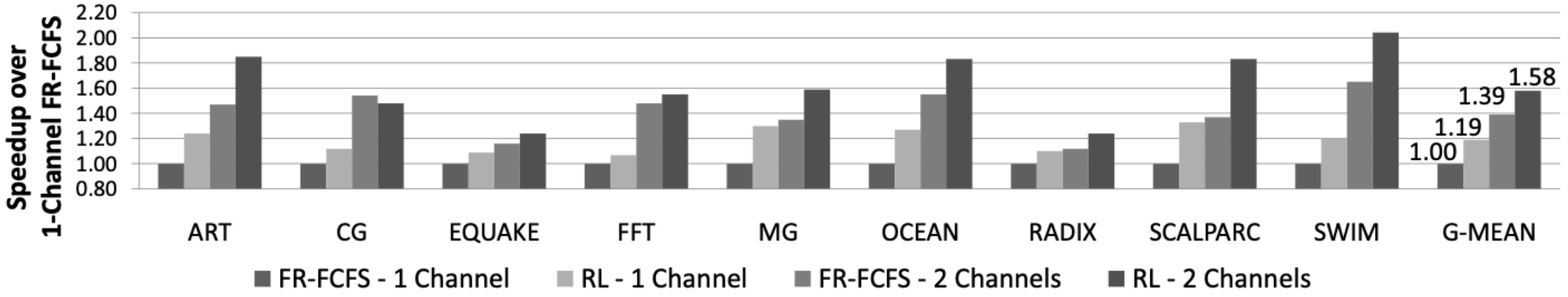

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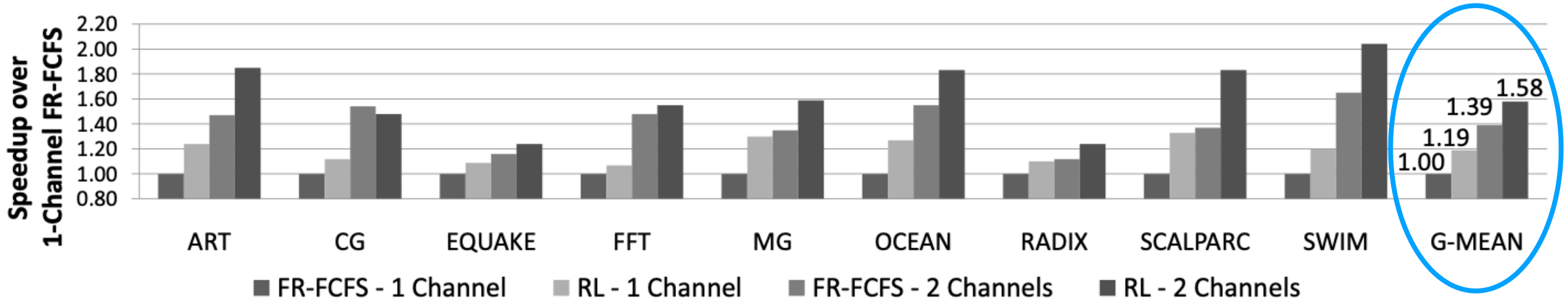
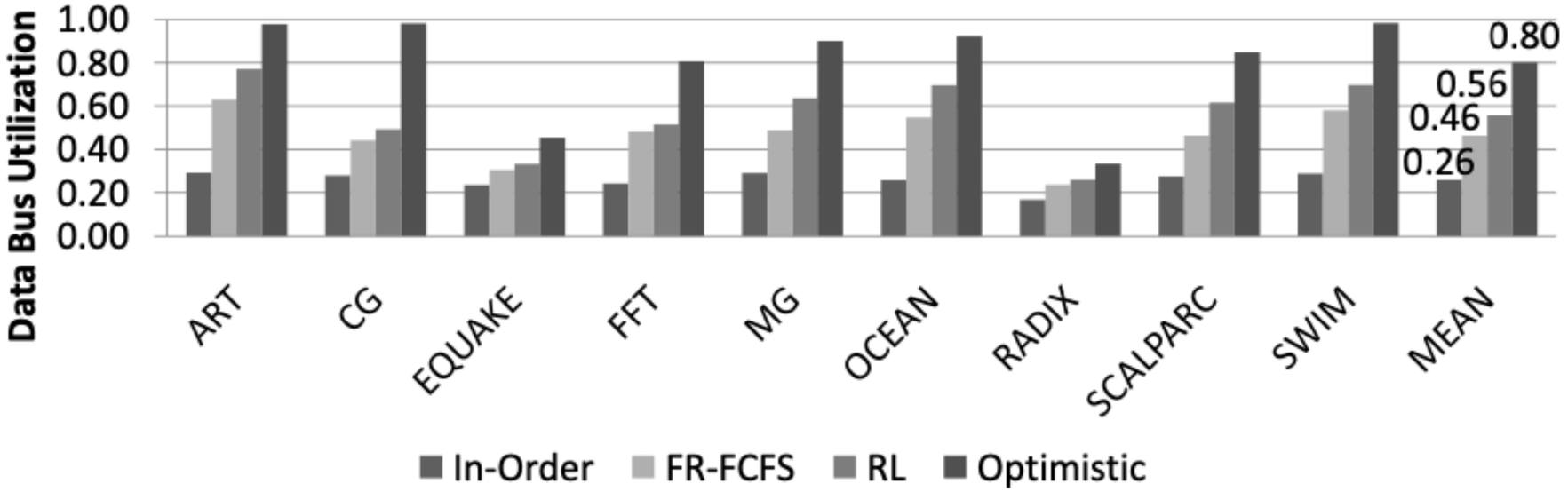


Evaluation: Data Bus Utilization



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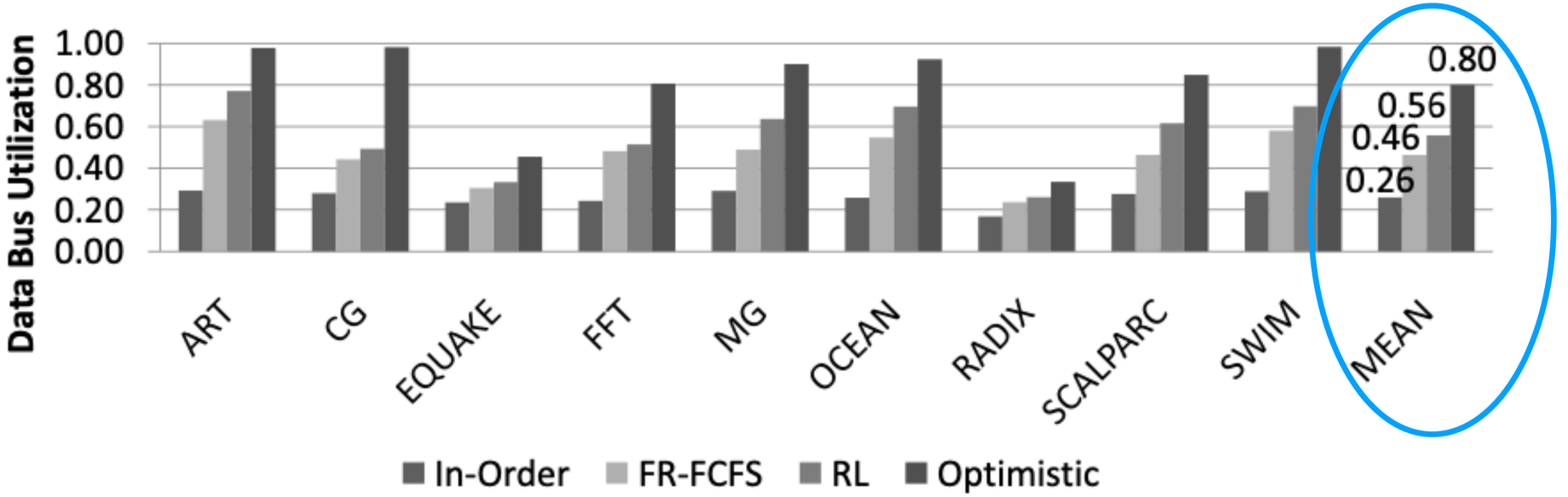

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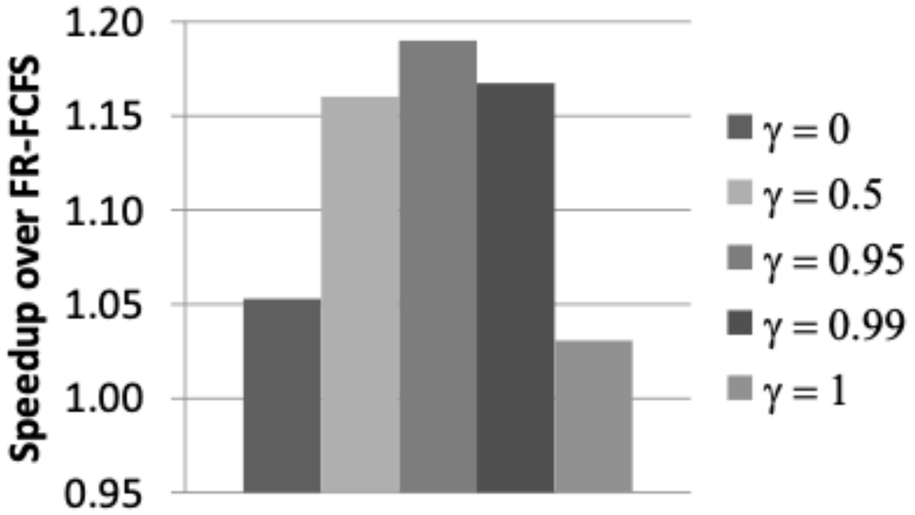

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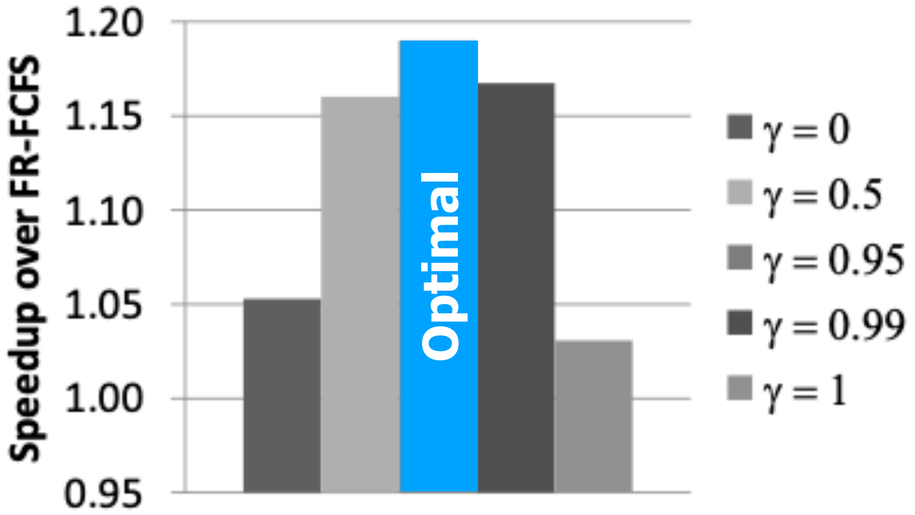

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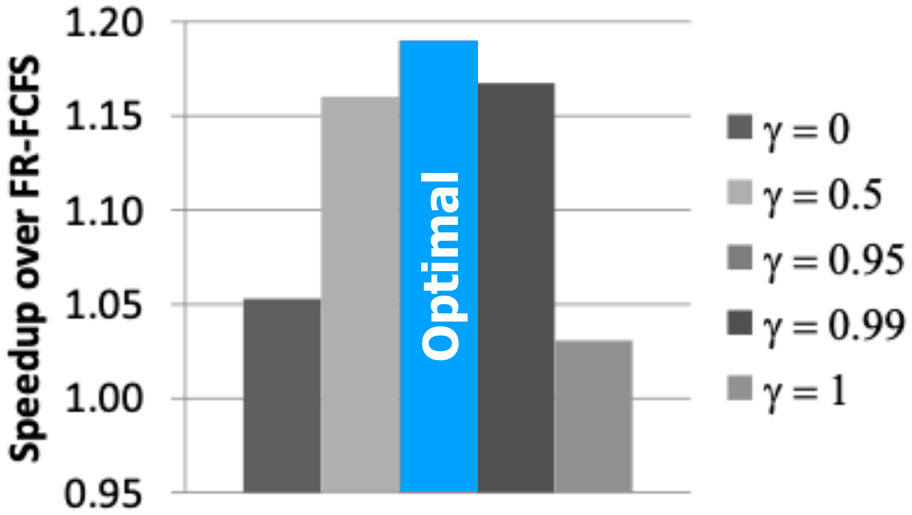

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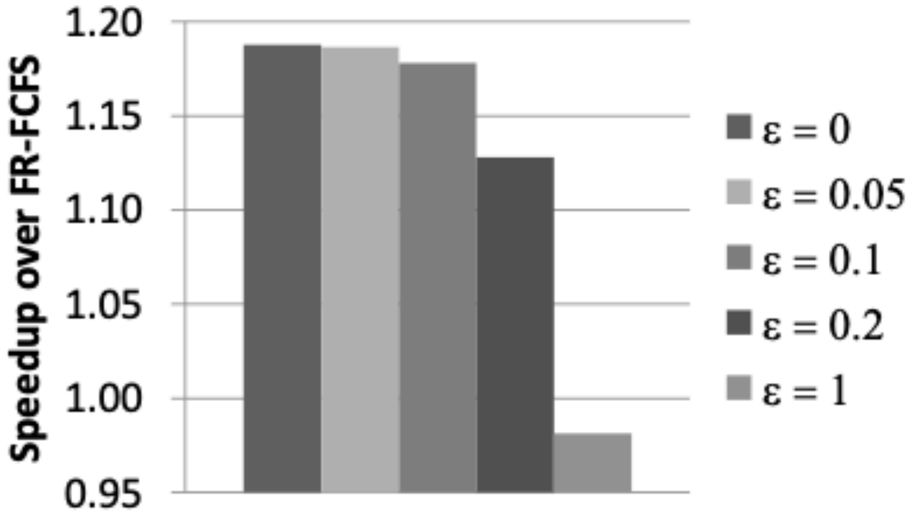

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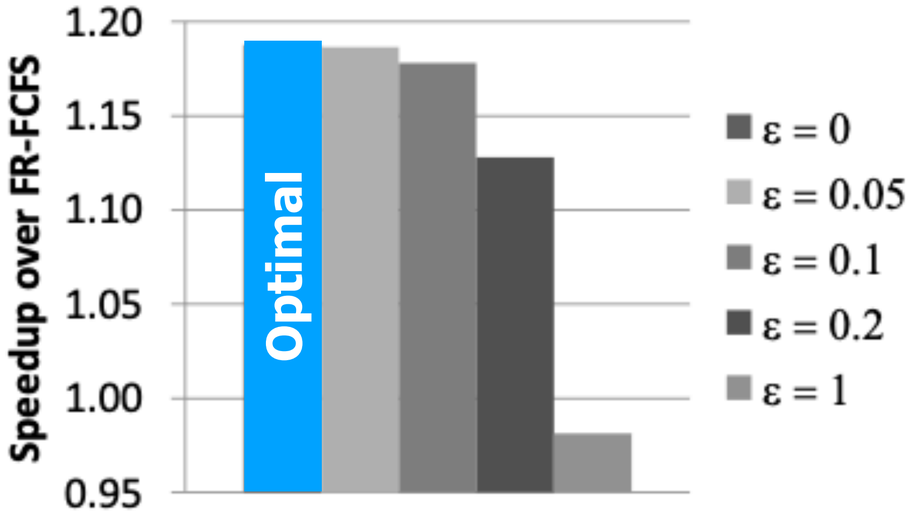

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Critique & Discussion

Strengths

Weaknesses

Thoughts

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3. The paper limits itself to a scope and does not fully consider what could be done outside of the assumed constraints

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Discussion

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What are potential reasons for or against implementing this in a real-world system?

Discussion

Are there other applications similar to this, which you can see in other Computer Architecture designs?

Discussion

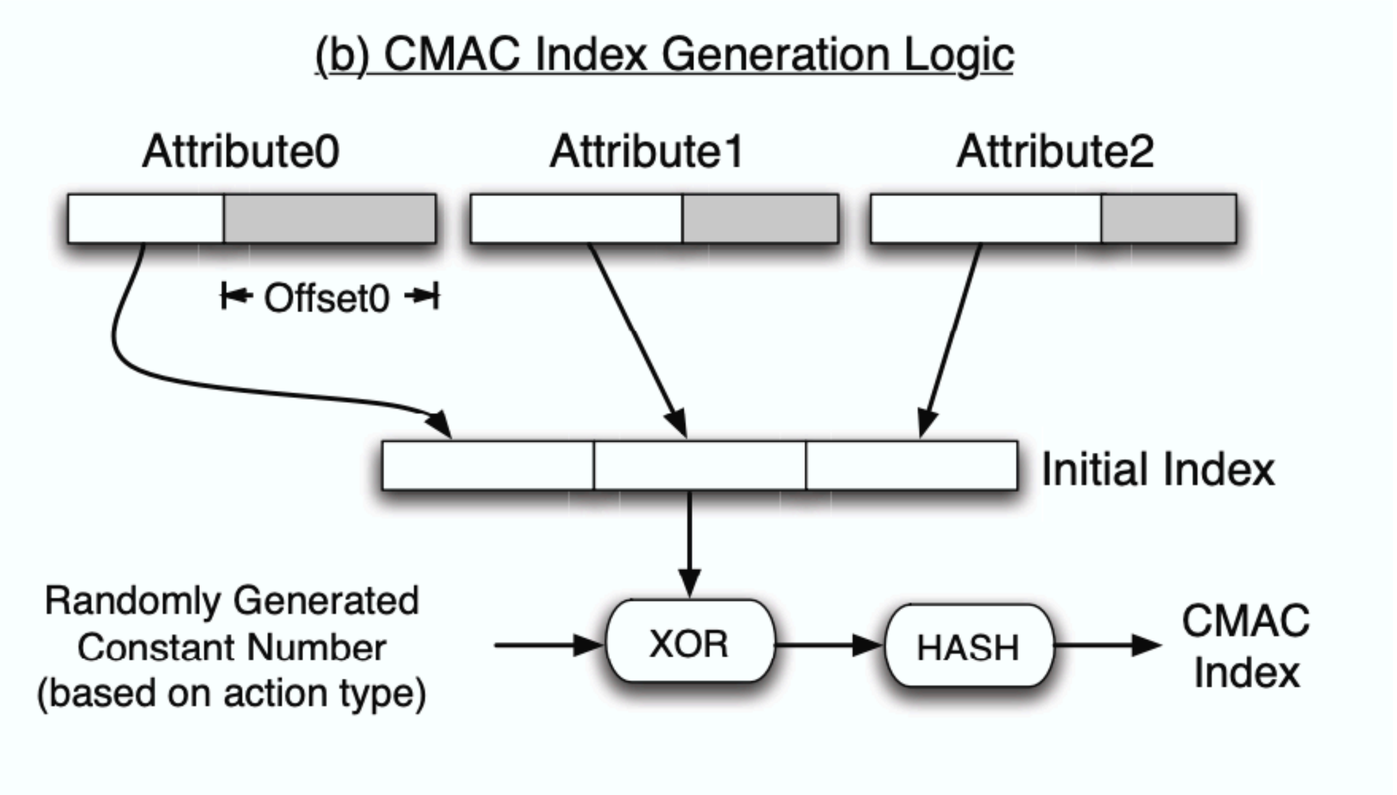
Is this worth exploring further now 13 years after the publishing of this paper?

Discussion

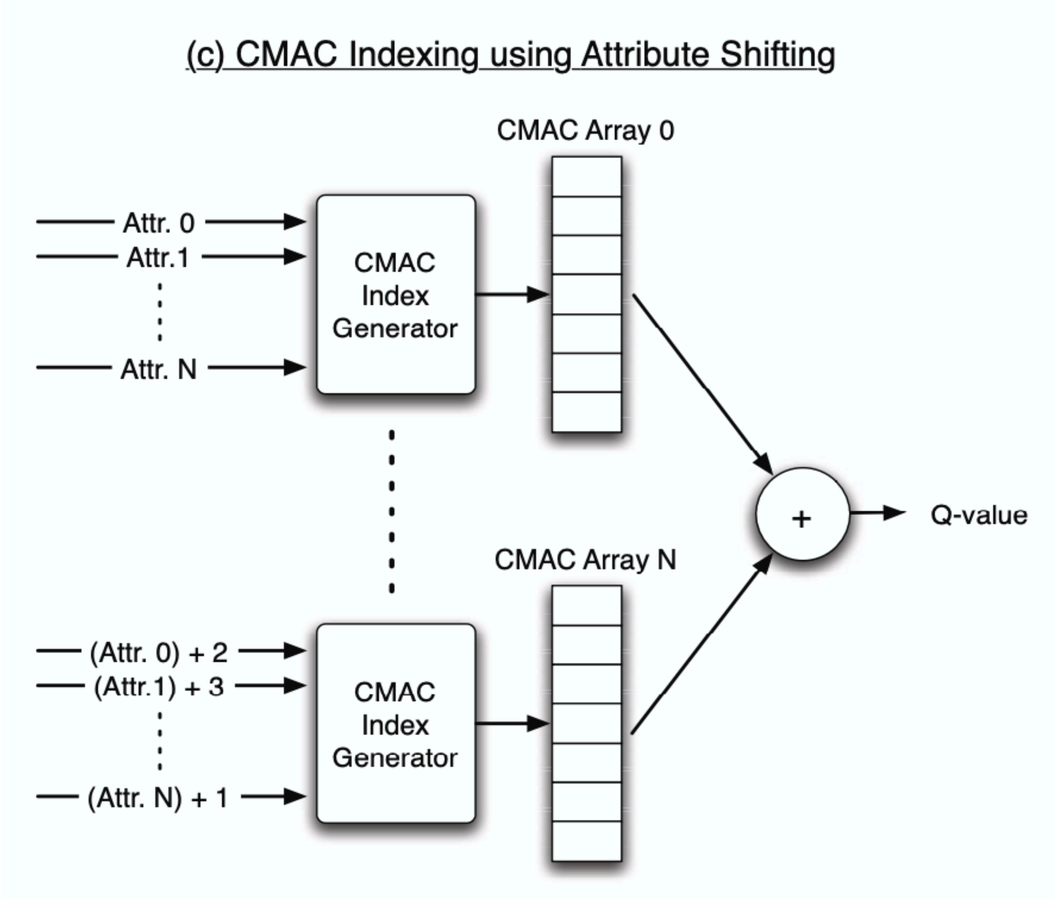
Can you see other criteria, other than only latency overhead, which could also be considered for an implementation of this technology?

Backup sildes

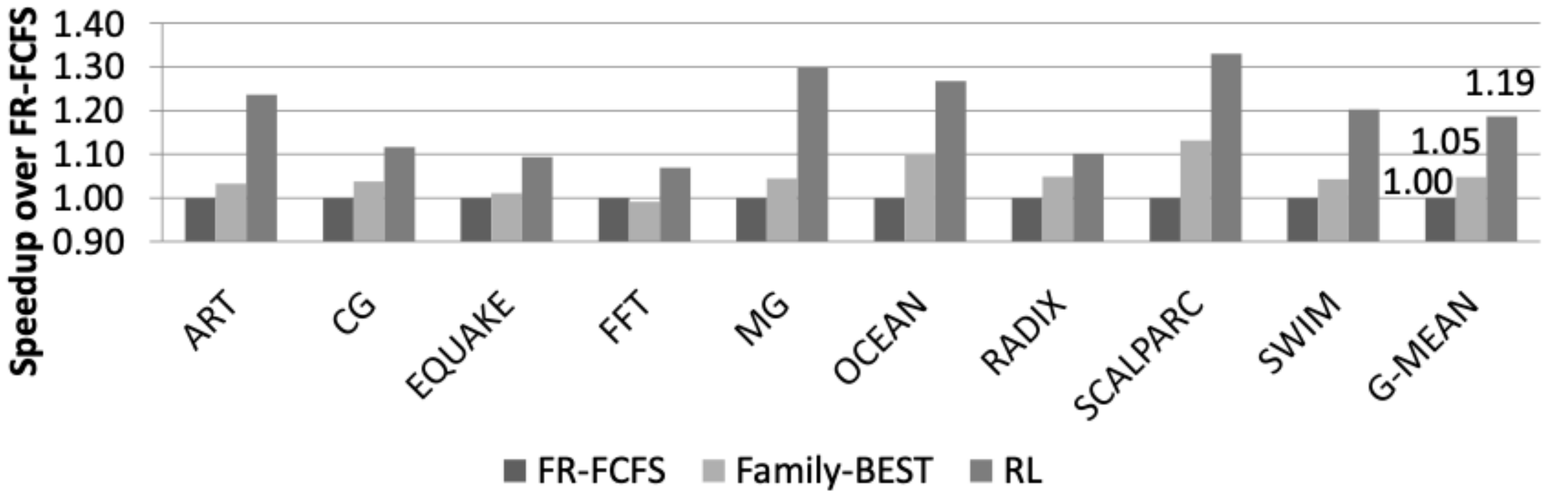
Implementation



Implementation

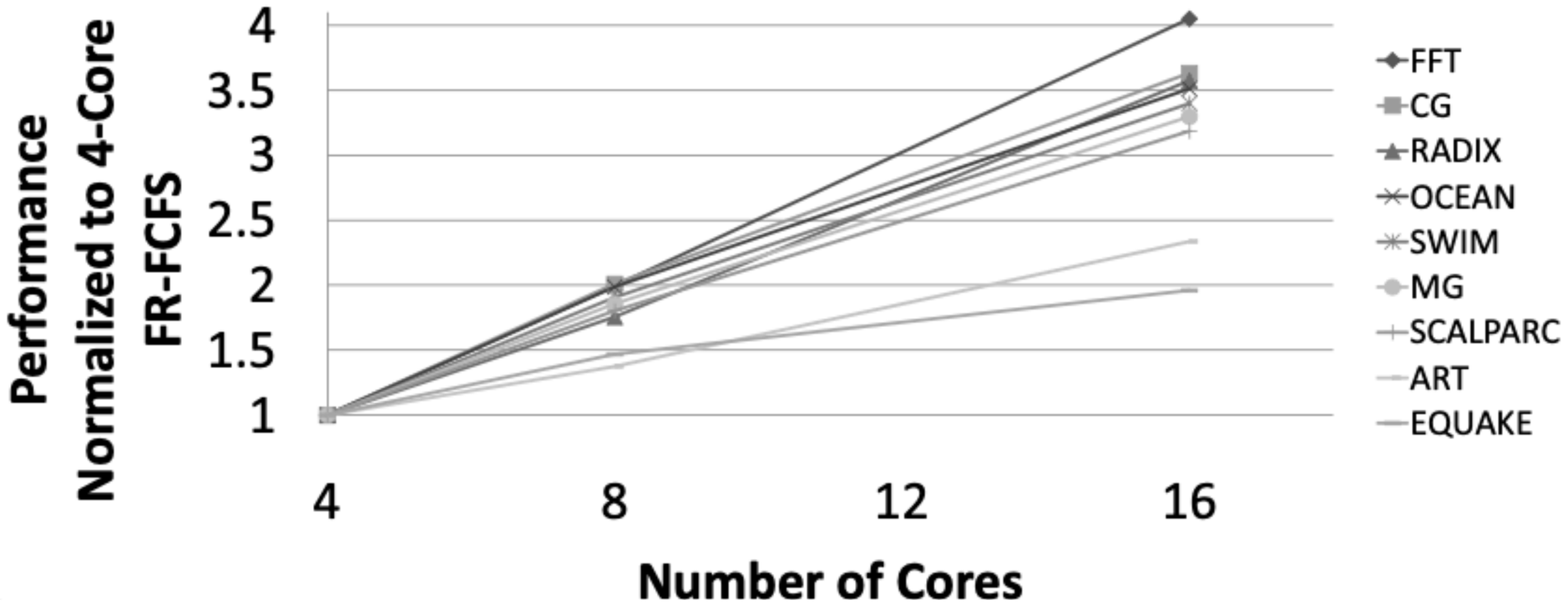


Evaluation: Speedup

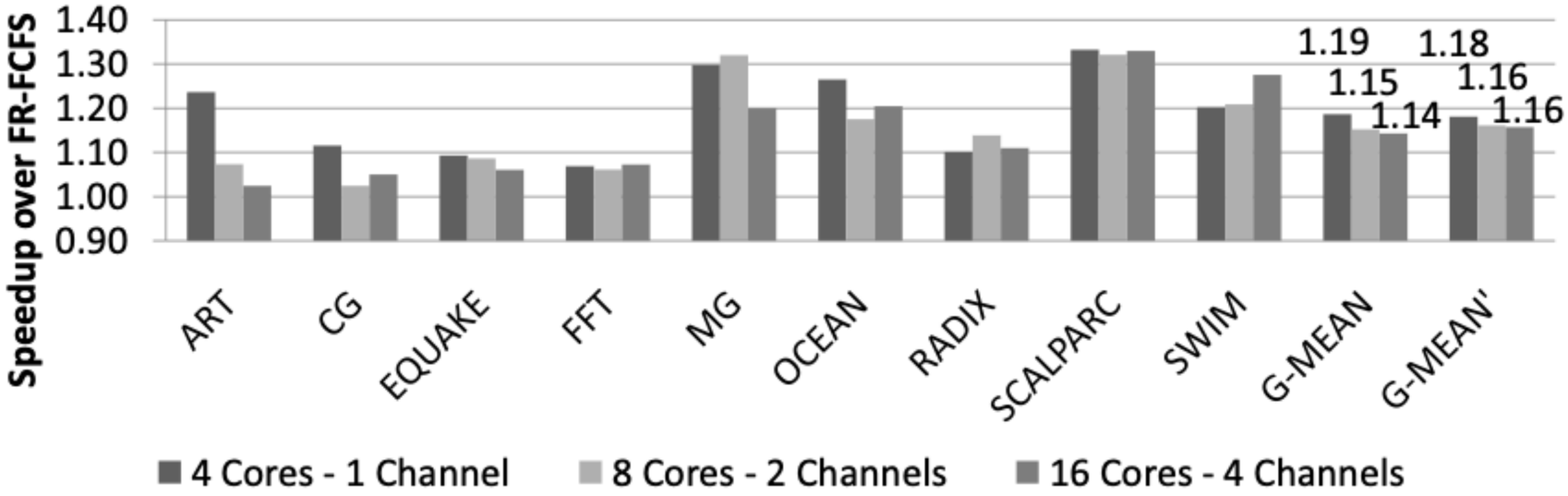


Same information is given to the FR-FCFS memory scheduler

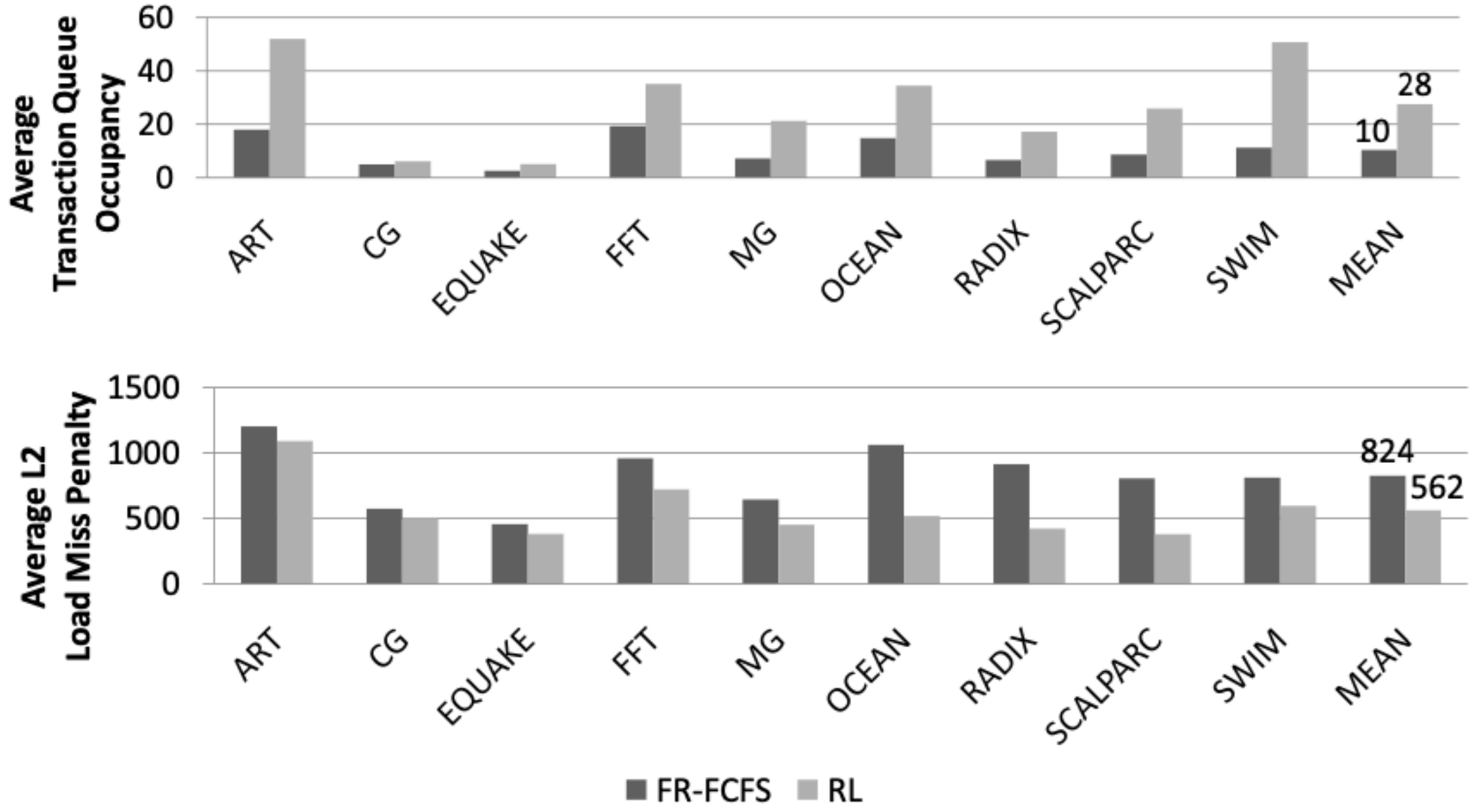
Evaluation: Performance



Evaluation: Speedup



Evaluation: System



Evaluation: static vs. dynamic