Multiscalar Processors

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Presented by Benjamin Gundersen

Outline

Executive Summary

Instruction-level Parallelism

Goal

Multiscalar Paradigm

Multiscalar Hardware

Analyzing CPU cycles

Comparison to other ILPs

Performance Evaluation

Strengths and Weaknesses

Inspired Work

Discussion

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- **Mechanism:** Each task is distributed to one of many parallel processing units while using one logical register file.
- **Result:** Multiscalar processor greatly improve performance in parallelisable workloads.

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- **Dataflow:** Instructions execute once input is available.

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- Previous mechanisms focused on increasing ILP, like VLIW or Superscalar exhibit a **key constraint:** stall instructions until all previous control dependencies have been resolved.

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- Increase ILP without the constraint of stalling until all previous control dependencies have been resolved by proposing the **Multiscalar Paradigm**.

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- **Pass values** between processing units.
- Impose **sequential appearance** by constraining when instructions can be executed.

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- Possible Hardware Implementation

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Possible Hardware Implementation

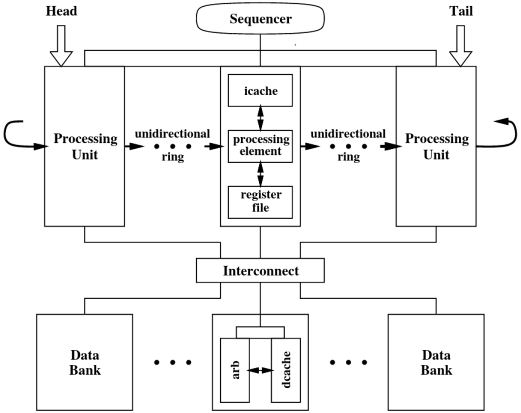
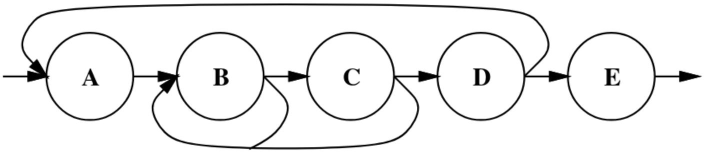


Figure: Example Hardware

Control Flow Graph (CFG)

- CFG consists of basic blocks (nodes) and control flow (edges).



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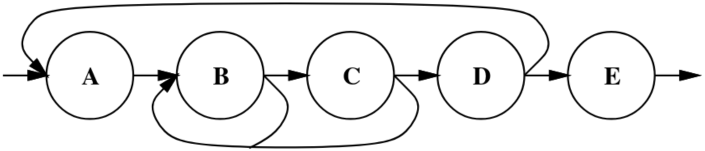

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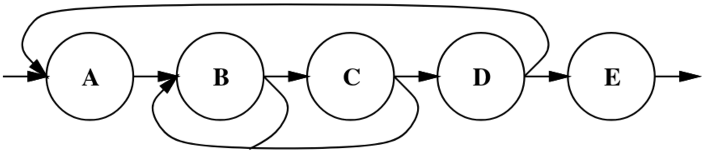

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- Tasks are not independent of each other.

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- **Speculative Tasks**
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- Head an tail pointers indicate which units are executing earliest and last of the current tasks.

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- **Solution:** Register and Memory synchronization.

Register synchronization

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- Consuming instructions have to **wait for all values it wants to consume**.

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- Multiscalar processors take the **aggressive approach**.

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- If a conflict occurs the task and all successors must be squashed.

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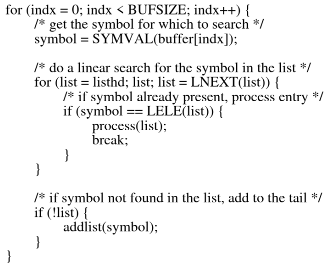
- Since values are forwarded earlier tasks must be retired in the order they were added.

Example Code



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for (indx = 0; indx < BUFSIZE; indx++) {
        /* get the symbol for which to search */
        symbol = SYMVAL(buffer[indx]);

        /* do a linear search for the symbol in the list */
        for (list = listhd; list; list = LNEXT(list)) {
                /* if symbol already present, process entry */
                if (symbol == LELE(list)) {
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                        break;
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Figure: Example Code Segment

- Take symbol from buffer and if it is in list process it. Otherwise add it to the list.

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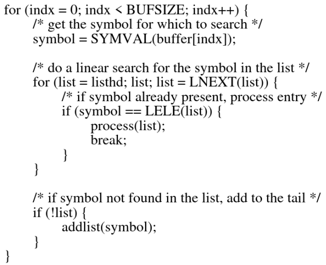

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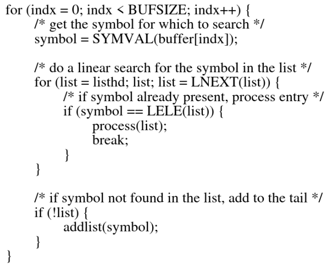

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- List not changing much means that many tasks can run independently from each other. Thus we get an execution of multiple instructions per cycle.

Multiscalar Paradigm; Next Steps

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- Only minimal changes have to be made to the ISA, thus an existing ISA can be used as basis.

Sequencer

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- **The compiler is our friend** and can solve these problems for us.

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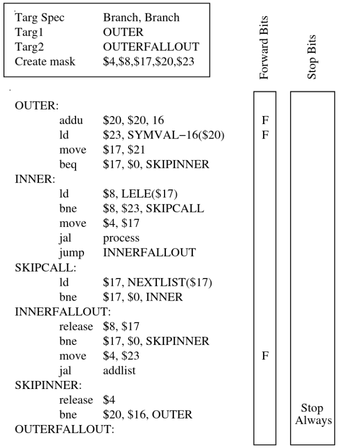

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Targ1           OUTER
Targ2           OUTERFALLOUT
Create mask     $4,$8,$17,$20,$23

OUTER:
        addu    $20, $20, 16
        ld      $23, SYMVAL−16($20)
        move    $17, $21
        beq     $17, $0, SKIPINNER
INNER:
        ld      $8, LELE($17)
        bne     $8, $23, SKIPCALL
        move    $4, $17
        jal     process
        jump    INNERFALLOUT
SKIPCALL:
        ld      $17, NEXTLIST($17)
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INNERFALLOUT:
        release $8, $17
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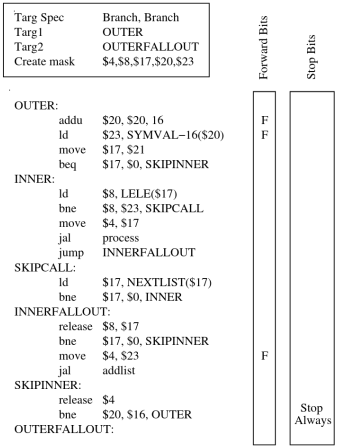

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- 18, 17 must be released after loop since they are repeatedly updated in the loop.

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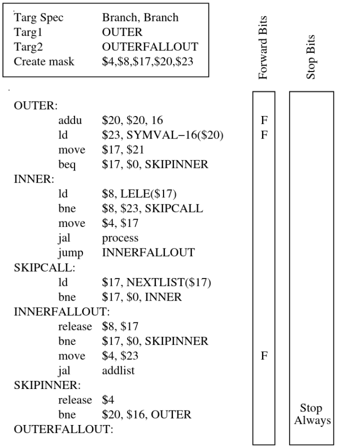

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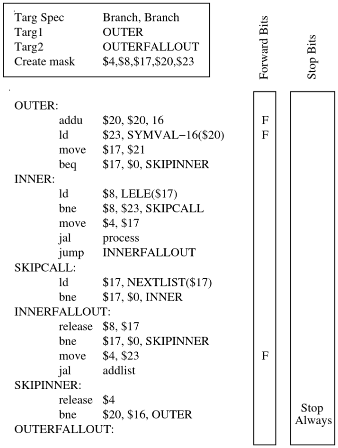

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OUTERFALLOUT:
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- Task creates values bound to registers: 4, 8, 17, 20, 23
- 18, 17 must be released after loop since they are repeatedly updated in the loop.
- The other values have forward bits.
- 4 is released if its update code is skipped.

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- Possible for non multiscalar and multiscalar binaries.
- Allows to change multiscalar interface by augmenting a binary.

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Multiscalar Hardware

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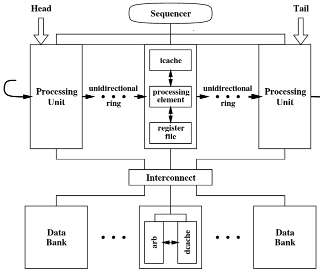

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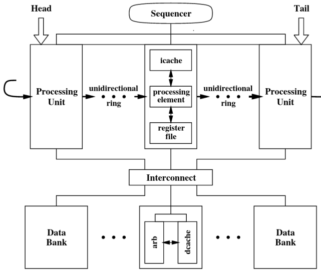

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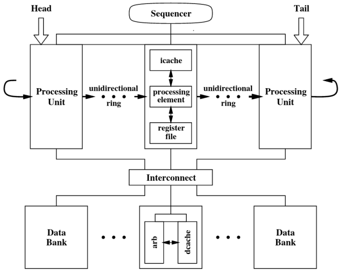

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- Given task descriptor determine / predict next task.

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- Through the unidirectional ring which connects all processing units information is forwarded.

Data Bank

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- **Non-useful computation** because it will be squashed later.
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- Remains **idle** since head is not finished but predecessor task has finished executing all instructions.

How to avoid

- **Non-useful computation:** Synchronization of scalars and globals

How to avoid

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How to avoid

- **Non-useful computation:** Synchronization of scalars and globals
- **No computation:** Early Validation of Prediction
- **Idle:** Reduce inter-task dependencies and balance the load.

Non-useful Computation: Synchronization

- **Experience:** Squashes because of memory conflict are usually caused by updates of **global scalars and structures**.

Non-useful Computation: Synchronization

- **Experience:** Squashes because of memory conflict are usually caused by updates of **global scalars and structures**.
- Thus these accesses should be **synchronized**.

No Computation: Early Validation of Prediction

- Catching false prediction **lowers time spent on non-computation cycles significantly**.

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- Could change structure of loops such that loop exit test is performed at the beginning.
- Could add explicit prediction validation instructions.

Idle: Reduce Inter-Task Dependencies

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- Consider: Induction variable updated as last instruction in a loop versus induction variable updated at beginning of a loop and copy kept for current task.

Idle: Load Balancing

- Some tasks may have a lot less work than others and thus are waiting for previous ones with more work.

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- Some tasks may have a lot less work than others and thus are waiting for previous ones with more work.
- Thus must be flexible in choice of grain size of a task.

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- Multiscalar processors do not have to check for conflicts when issuing loads and stores.
- Multiscalar hardware is less complex than superscalar hardware.

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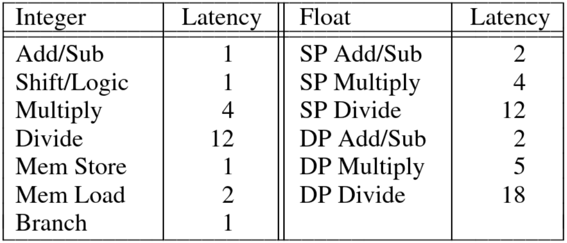

Integer	Latency	Float	Latency
Add/Sub	1	SP Add/Sub	2
Shift/Logic	1	SP Multiply	4
Multiply	4	SP Divide	12
Divide	12	DP Add/Sub	2
Mem Store	1	DP Multiply	5
Mem Load	2	DP Divide	18
Branch	1		

Figure: Functional Unit latencies

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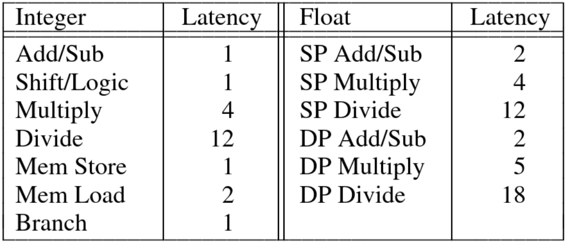

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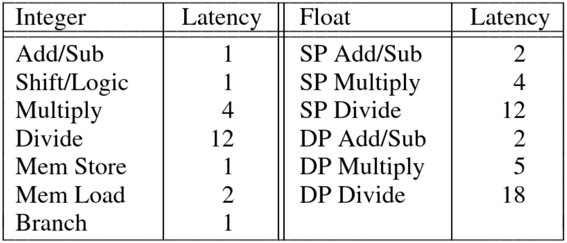

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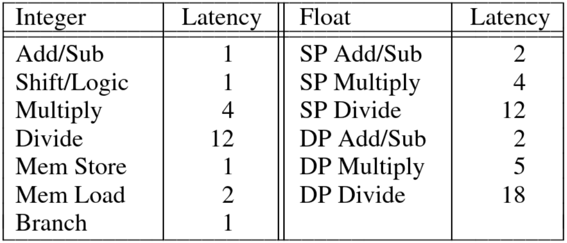

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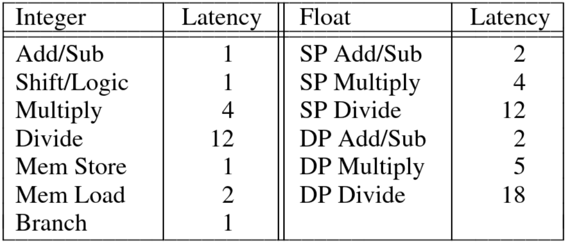
- 1 or 2 simple integer, 1 complex integer, 1 floating point, 1 branch and 1 memory FU.
- Unidirectional ring adds 1 cycle communication latency.



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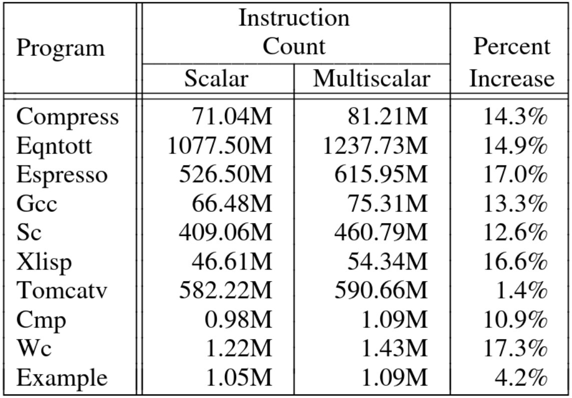
Benchmarks

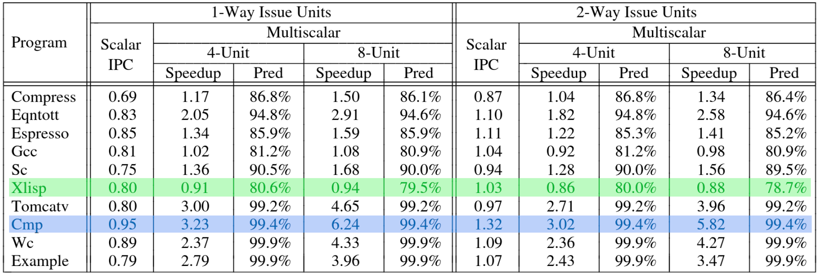


Program	Instruction Count		Percent
	Scalar	Multiscalar	Increase
Compress	71.04M	81.21M	14.3%
Eqntott	1077.50M	1237.73M	14.9%
Espresso	526.50M	615.95M	17.0%
Gcc	66.48M	75.31M	13.3%
Sc	409.06M	460.79M	12.6%
Xlisp	46.61M	54.34M	16.6%
Tomcatv	582.22M	590.66M	1.4%
Cmp	0.98M	1.09M	10.9%
Wc	1.22M	1.43M	17.3%
Example	1.05M	1.09M	4.2%

Figure: Benchmark Instruction Count

- Number of dynamic instructions listed. More in Multiscalar because of additional multiscalar instructions.

In-Order



Program	1-Way Issue Units					2-Way Issue Units				
	Scalar IPC	Multiscalar				Scalar IPC	Multiscalar			
		4-Unit		8-Unit			4-Unit		8-Unit	
		Speedup	Pred	Speedup	Pred		Speedup	Pred	Speedup	Pred
Compress	0.69	1.17	86.8%	1.50	86.1%	0.87	1.04	86.8%	1.34	86.4%
Eqntott	0.83	2.05	94.8%	2.91	94.6%	1.10	1.82	94.8%	2.58	94.6%
Espresso	0.85	1.34	85.9%	1.59	85.9%	1.11	1.22	85.3%	1.41	85.2%
Gcc	0.81	1.02	81.2%	1.08	80.9%	1.04	0.92	81.2%	0.98	80.9%
Sc	0.75	1.36	90.5%	1.68	90.0%	0.94	1.28	90.0%	1.56	89.5%
Xlisp	0.80	0.91	80.6%	0.94	79.5%	1.03	0.86	80.0%	0.88	78.7%
Tomcatv	0.80	3.00	99.2%	4.65	99.2%	0.97	2.71	99.2%	3.96	99.2%
Cmp	0.95	3.23	99.4%	6.24	99.4%	1.32	3.02	99.4%	5.82	99.4%
Wc	0.89	2.37	99.9%	4.33	99.9%	1.09	2.36	99.9%	4.27	99.9%
Example	0.79	2.79	99.9%	3.96	99.9%	1.07	2.43	99.9%	3.47	99.9%

Figure: In-Order Issue Processing Units.

In-Order

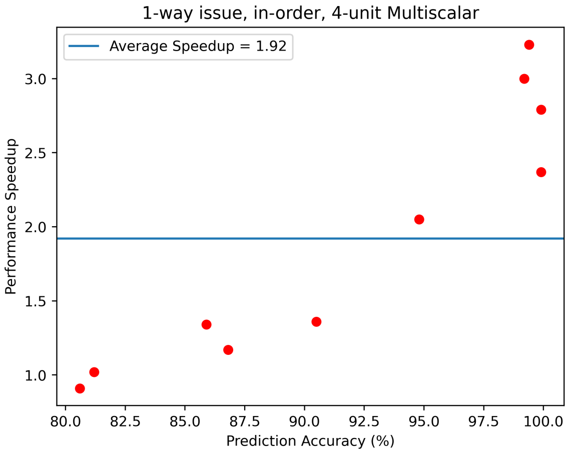


Figure: 1-way issue, in-order, 4-unit Multiscalar

In-Order

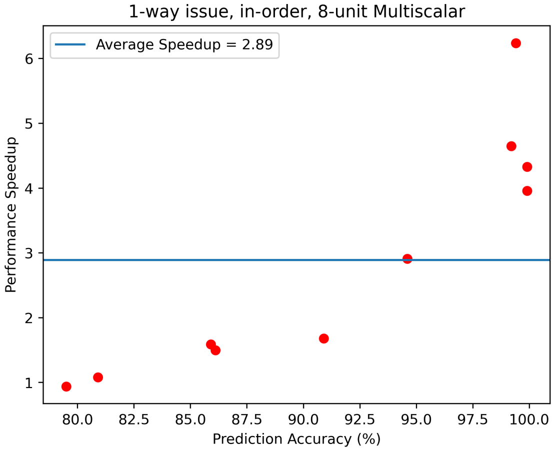


Figure: 1-way issue, in-order, 8-unit Multiscalar

In-Order

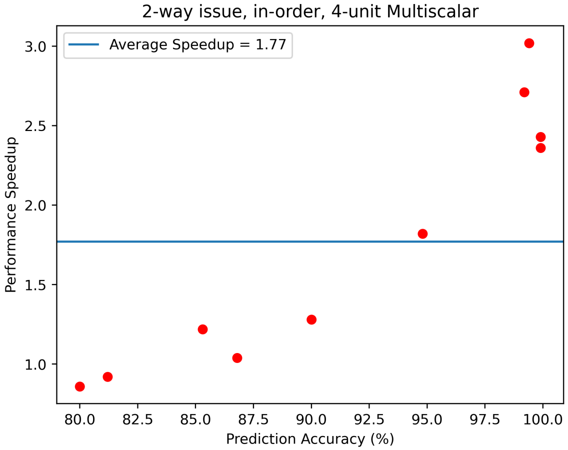


Figure: 2-way issue, in-order, 4-unit Multiscalar

In-Order

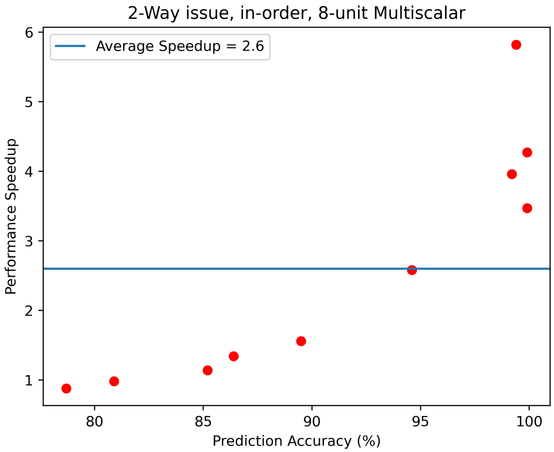
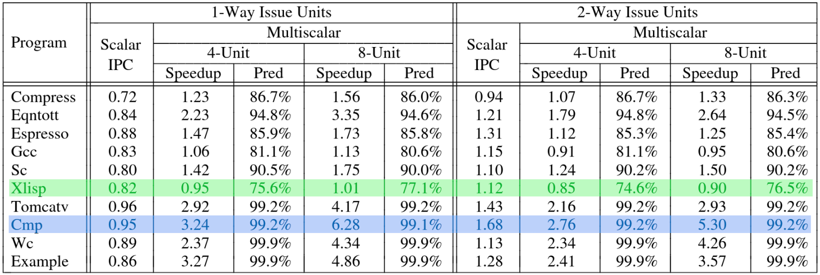


Figure: 2-way issue, in-order, 8-unit Multiscalar

Out-Order



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	Scalar IPC	Multiscalar				Scalar IPC	Multiscalar			
		4-Unit		8-Unit			4-Unit		8-Unit	
		Speedup	Pred	Speedup	Pred		Speedup	Pred	Speedup	Pred
Compress	0.72	1.23	86.7%	1.56	86.0%	0.94	1.07	86.7%	1.33	86.3%
Eqntott	0.84	2.23	94.8%	3.35	94.6%	1.21	1.79	94.8%	2.64	94.5%
Espresso	0.88	1.47	85.9%	1.73	85.8%	1.31	1.12	85.3%	1.25	85.4%
Gcc	0.83	1.06	81.1%	1.13	80.6%	1.15	0.91	81.1%	0.95	80.6%
Sc	0.80	1.42	90.5%	1.75	90.0%	1.10	1.24	90.2%	1.50	90.2%
Xlisp	0.82	0.95	75.6%	1.01	77.1%	1.12	0.85	74.6%	0.90	76.5%
Tomcatv	0.96	2.92	99.2%	4.17	99.2%	1.43	2.16	99.2%	2.93	99.2%
Cmp	0.95	3.24	99.2%	6.28	99.1%	1.68	2.76	99.2%	5.30	99.2%
Wc	0.89	2.37	99.9%	4.34	99.9%	1.13	2.34	99.9%	4.26	99.9%
Example	0.86	3.27	99.9%	4.86	99.9%	1.28	2.41	99.9%	3.57	99.9%

Figure: Out-Of-Order Issue Processing Units.

Out-Order

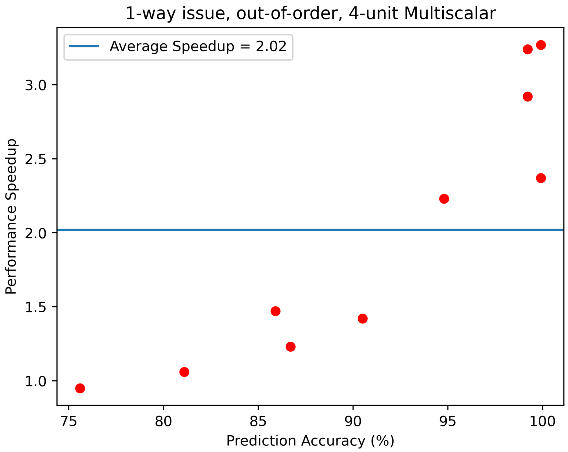

Figure: 1-way issue, out-of-order, 4-unit Multiscalar

Out-Order

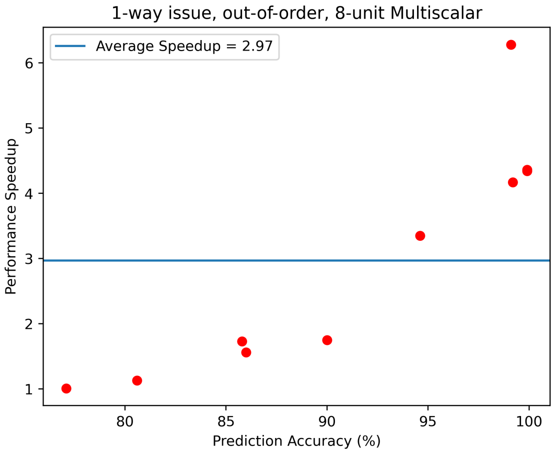

Figure: 1-way issue, out-of-order, 8-unit Multiscalar

Out-Order

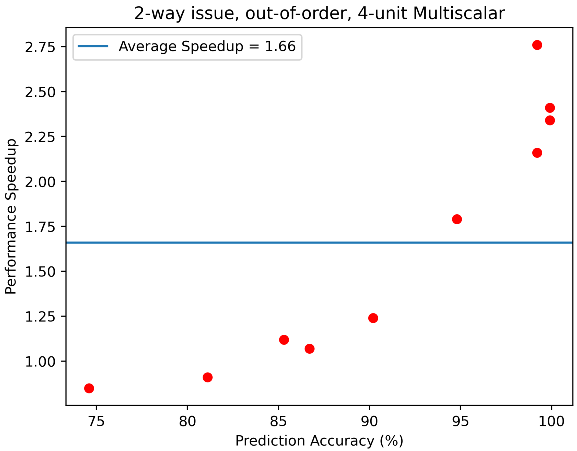

Figure: 2-way issue, out-of-order, 4-unit Multiscalar

Out-Order

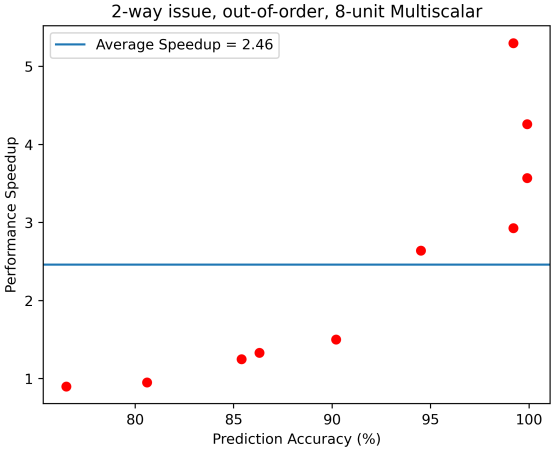

Figure: 2-way issue, out-of-order, 8-unit Multiscalar

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- With high prediction accuracy come large speedups.
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- ISA needs to be (minimally) changed.
- Speedup does not appear to be capped at 8-units for highly predictable tasks, would have been interesting to see how the speedup behaves with 16-units on highly predictable executions.

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Inspired Work: Slipstream processors

- **Slipstream processors:** Create shorter but equivalent by removing ineffectual computation and computation related to highly-predictable control flow. Concurrently run original and short program. Shorter program speculatively runs ahead of original program and supplies original program with control and data flow outcomes. The full program then uses that information to execute more efficiently and validates the speculative, shorer program.

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- *Purser, Zach, Karthik Sundaramoorthy, and Eric Rotenberg. "A study of slipstream processors." Proceedings of the 33rd annual ACM/IEEE International Symposium on Microarchitecture. 2000.*

Inspired Work: Thread level speculation

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- *Steffan, J. Greggory, et al. ”A scalable approach to thread-level speculation.” ACM SIGARCH Computer Architecture News 28.2 (2000): 1-12.*

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Optimizing Forwarding of Values

What can be done to potentially reduce the number of values which have to be forwarded?

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- *Exploiting Dead Value Information Milo M. Martin, Amir Roth, Charles N. Fischer 30th Annual international Symposium on Microarchitecture (MICRO-30), Dec 1997.*

Microarchitecture changes

How can the microarchitecture be changed to improve certain metrics like space and latency?

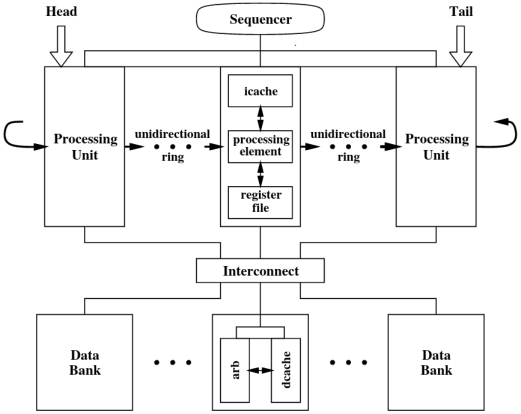

Figure: Example Hardware

Microarchitecture changes

- **Space**: Processing units share functional units like floating point units. Negative: May have to wait for other processing units to finish using parts of hardware.

Microarchitecture changes

- **Space**: Processing units share functional units like floating point units. Negative: May have to wait for other processing units to finish using parts of hardware.
- **Latency**: Move data bank directly next to processing units. Negative: Need to handle inconsistent caches and buffers and forward information.

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- *Register Integration: A Simple and Efficient Implementation of Squash Reuse Amir Roth and Gurindar S. Sohi 33rd International Symposium on Microarchitecture (MICRO-33), Dec. 10-13, 2000.*

Task selection

- Which heuristics could be helpful in determining the task boundaries?

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- Should we reorder instructions and how?

Task selection

- Use heuristics:

Task selection

- Use heuristics:
- **Task size**

Task selection

- Use heuristics:
- **Task size**
- **Control Flow**

Task selection

- Use heuristics:
- **Task size**
- **Control Flow**
- **Data Dependence**

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- *T. N. Vijaykumar and G. S. Sohi, "Task selection for a multiscalar processor," Proceedings. 31st Annual ACM/IEEE International Symposium on Microarchitecture, 1998, pp. 81-92, doi: 10.1109/MICRO.1998.742771.*