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* ECE DEPARTMENT, UNIVERSITY OF HOUSTON
** HPC GROUP, PACIFIC NORTHWEST NATIONAL LAB (PNNL)
*** CAPITAL NORMAL UNIVERSITY BEIJING

PRESENTED AT: HPCA 2017

REVIEW: ANDREW DOBIS

# PROCESSING-IN-MEMORY ENABLED GRAPHICS PROCESSORS FOR 3D RENDERING

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  - Uses a **camera-angle threshold** for **performance/accuracy** ratio control.
- **Key results**: Evaluated on various 3D video-games.
  - Average **1.4x** rendering speedup over baseline.
  - Average **22% less** energy consumption compared to baseline.

# OUTLINE

- Background: Texture Filtering
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- Solutions:
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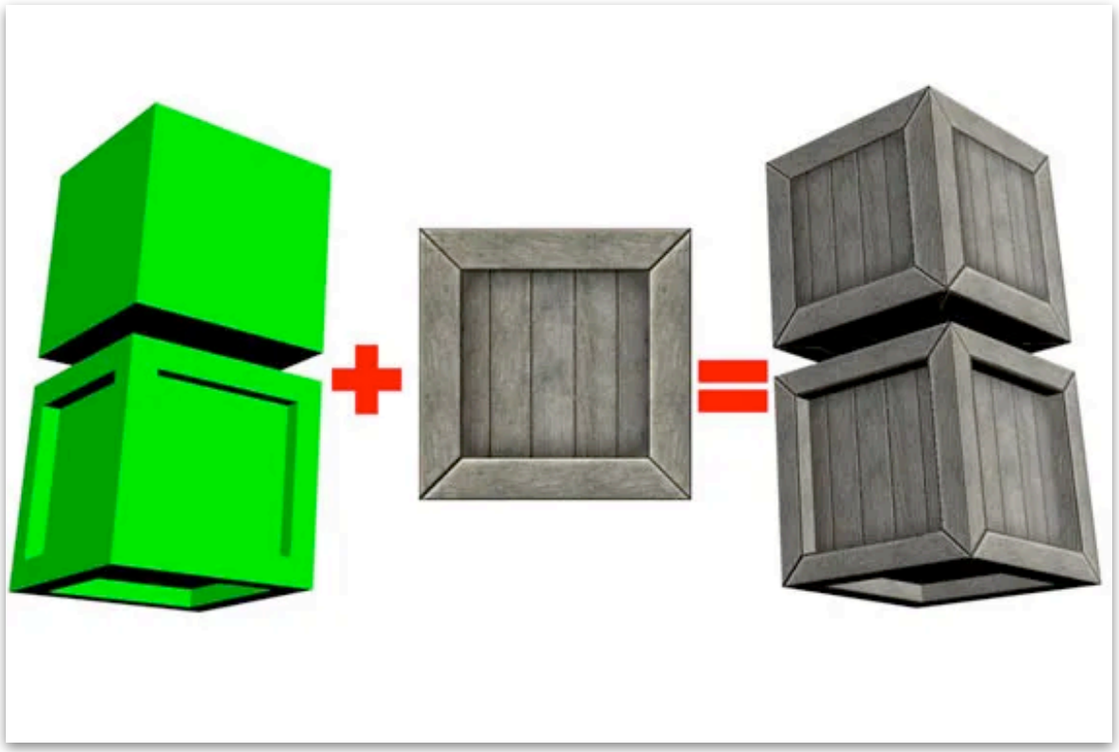
**Texturing Example**



*[1]: https://www.gamedeveloper.com/design/book-excerpt-3d-game-textures-create-professional-game-art-using-photoshop*

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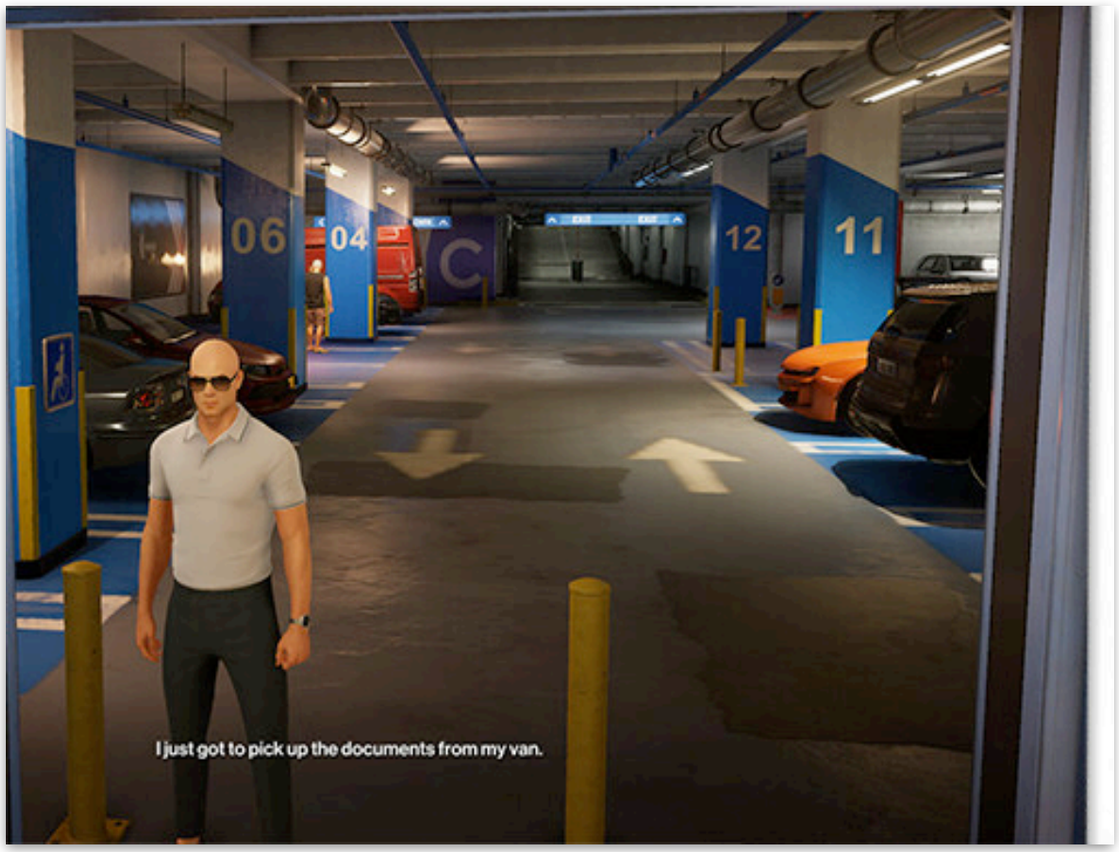


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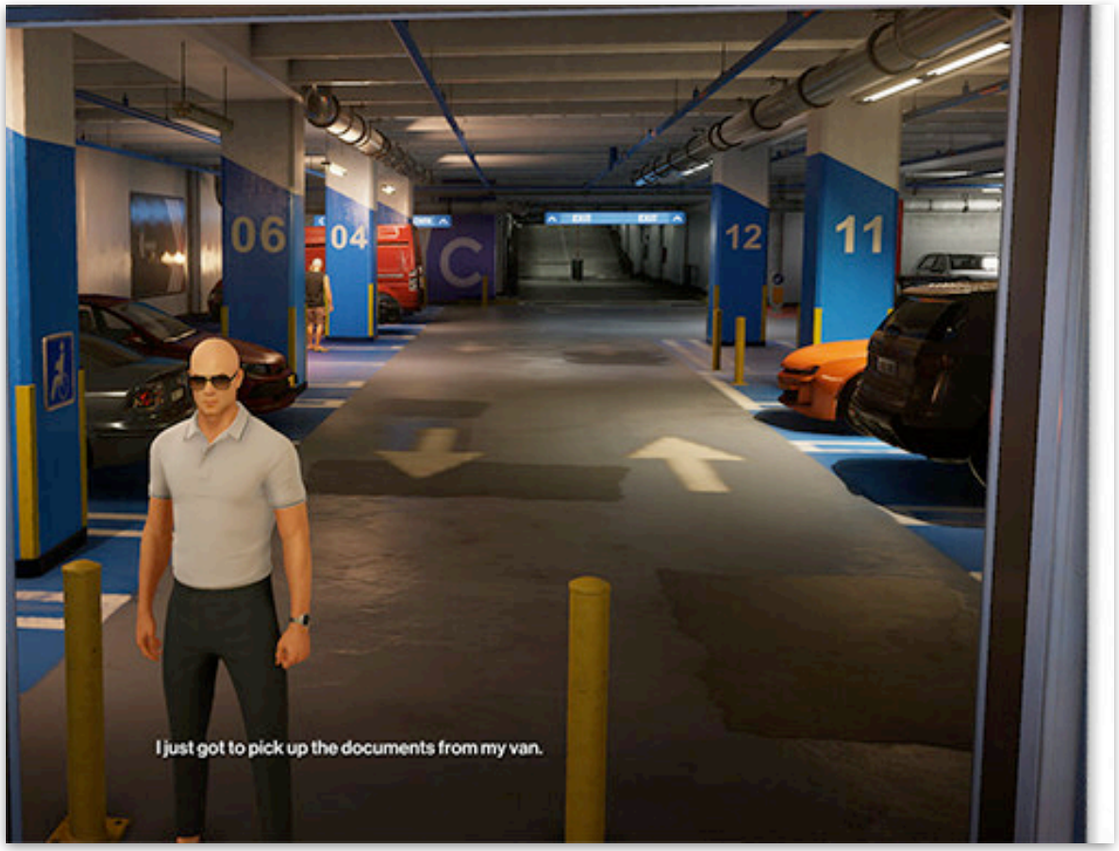


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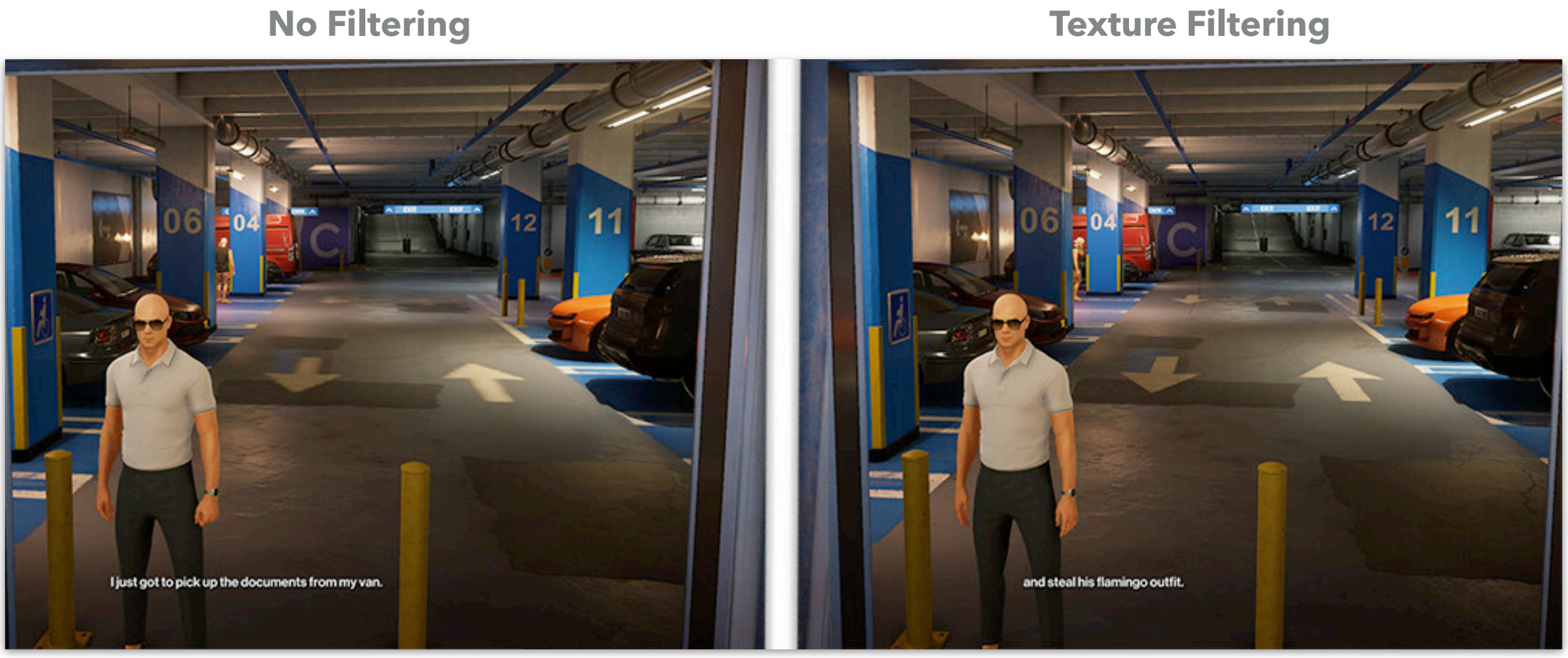


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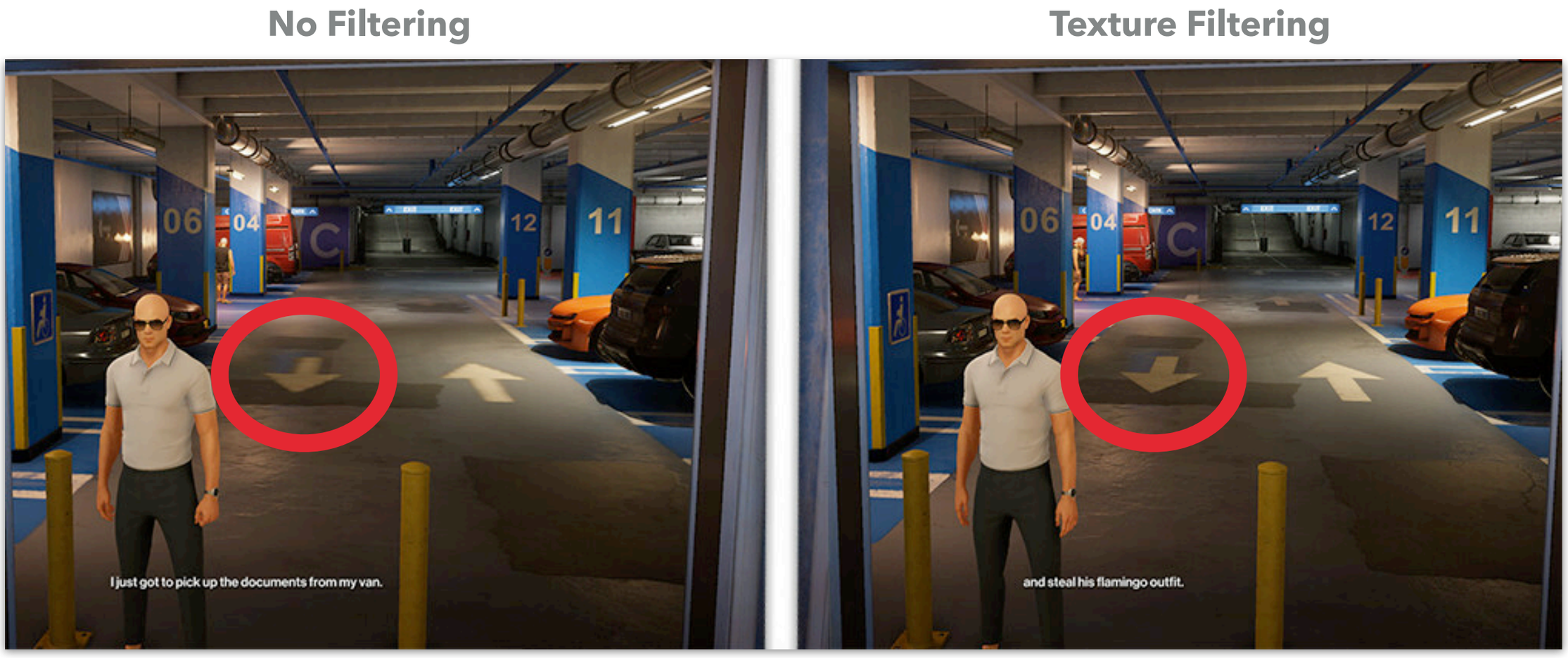


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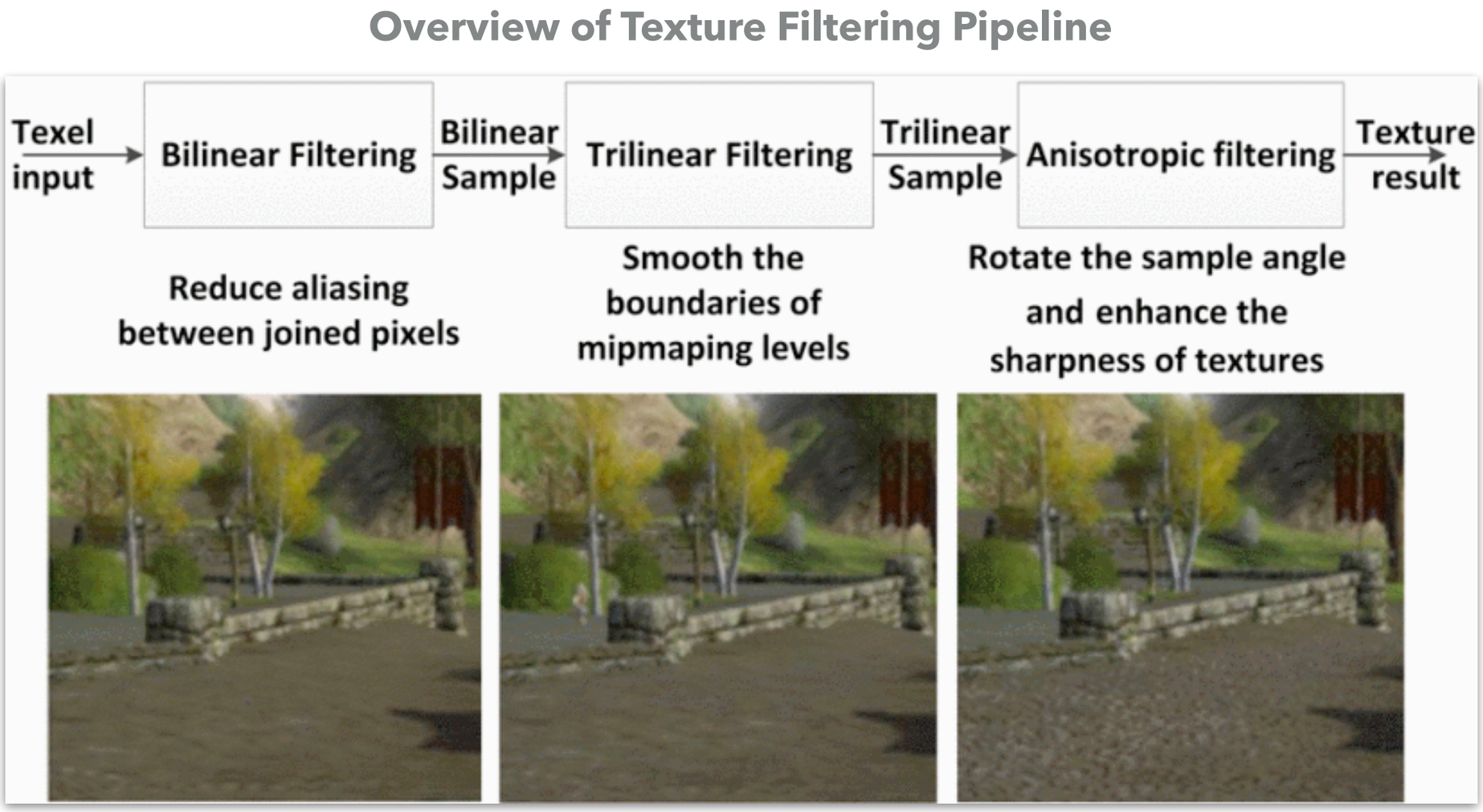
**Texture Filtering**

**Image is blurry when camera angle is low.**

# BACKGROUND: TEXTURE FILTERING

- Goal: Reduce blur from under-sampling textures



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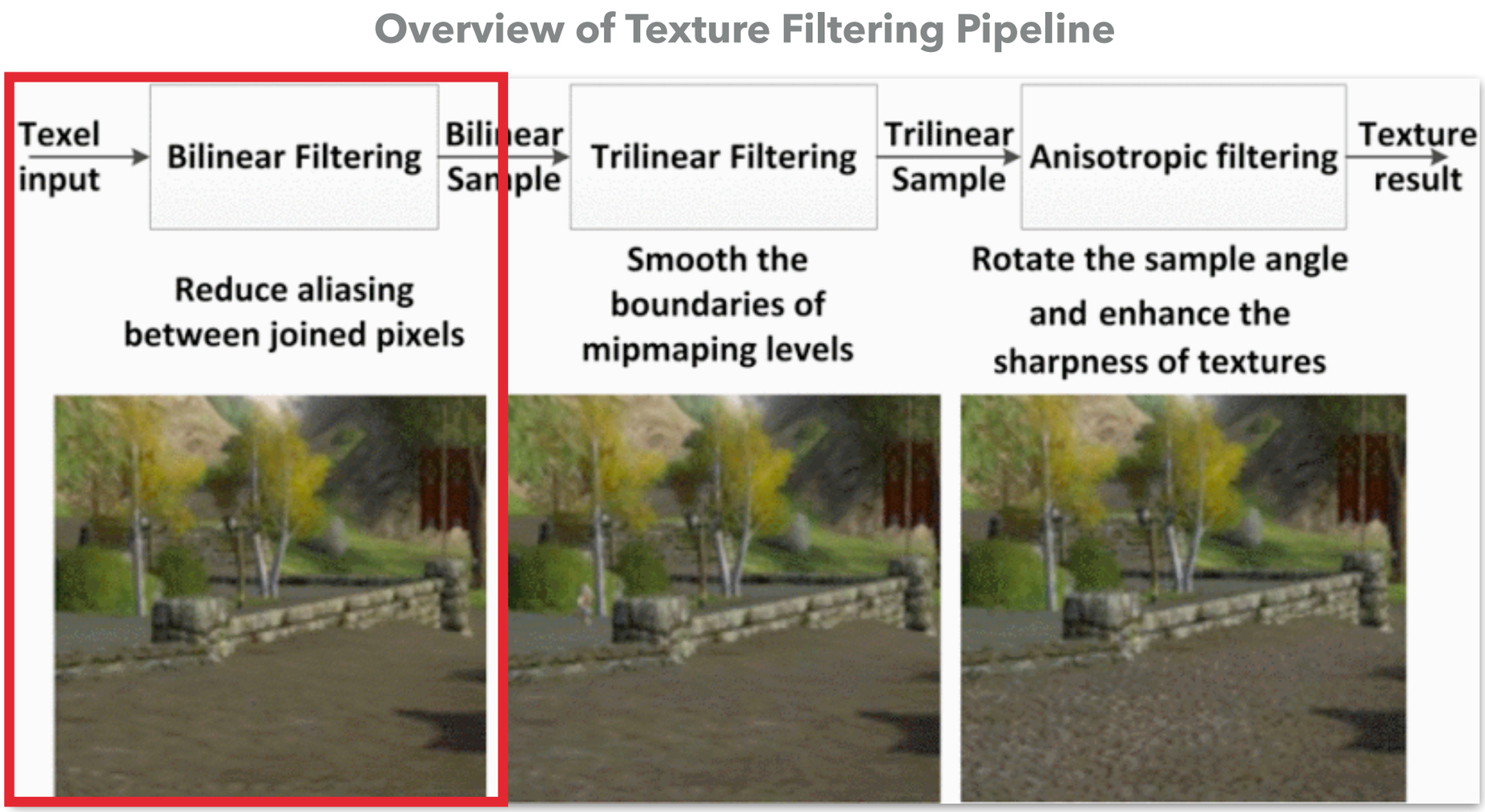

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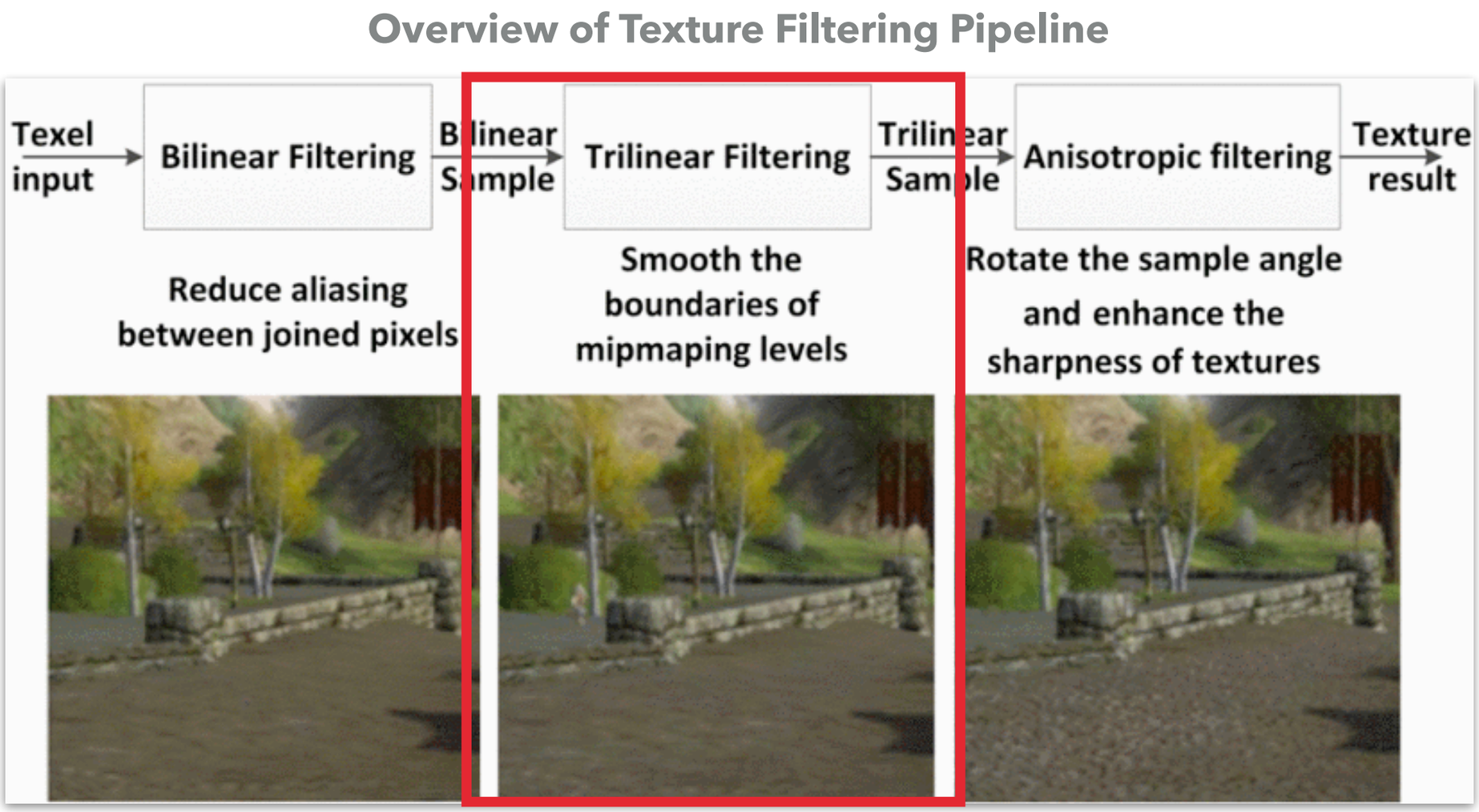

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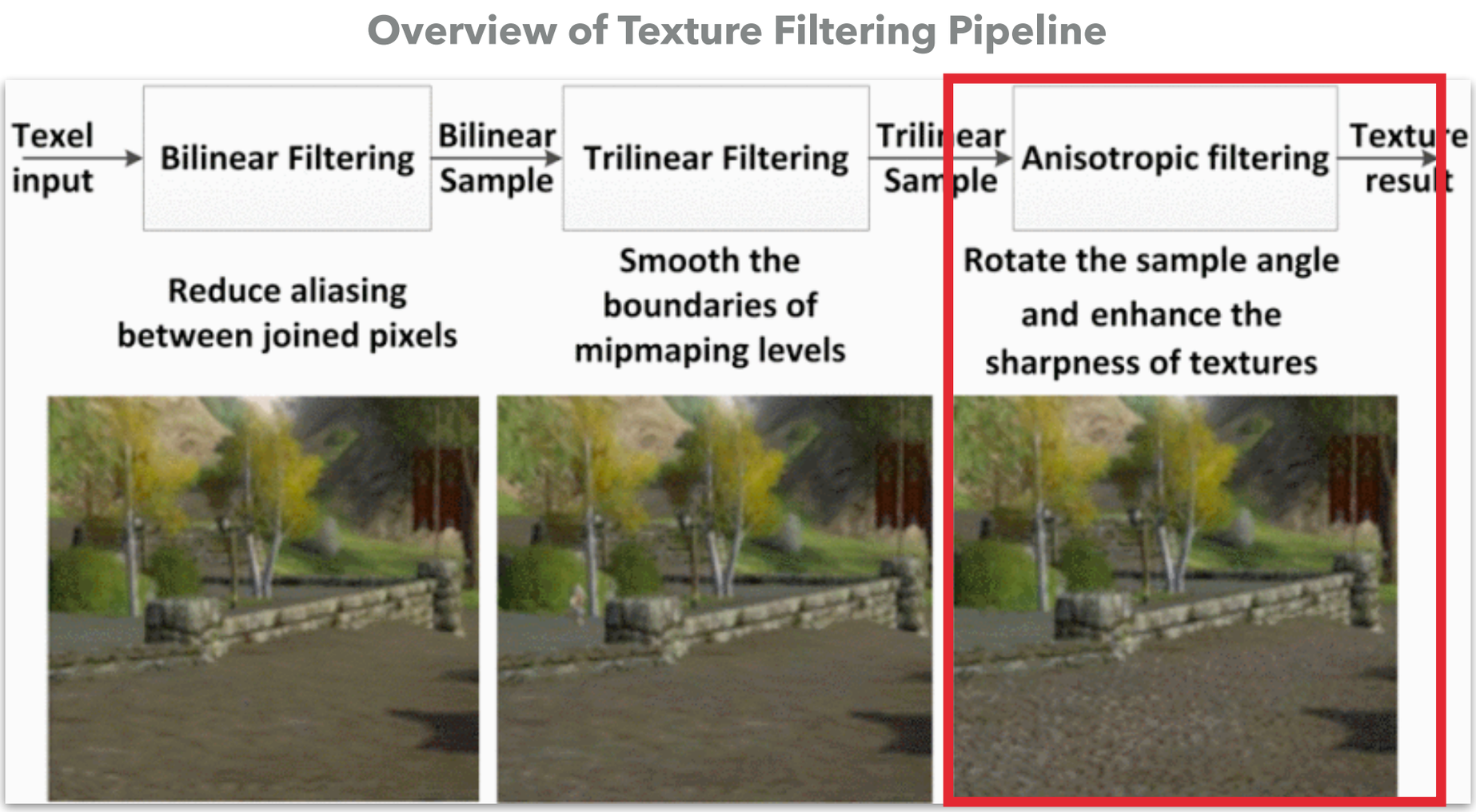

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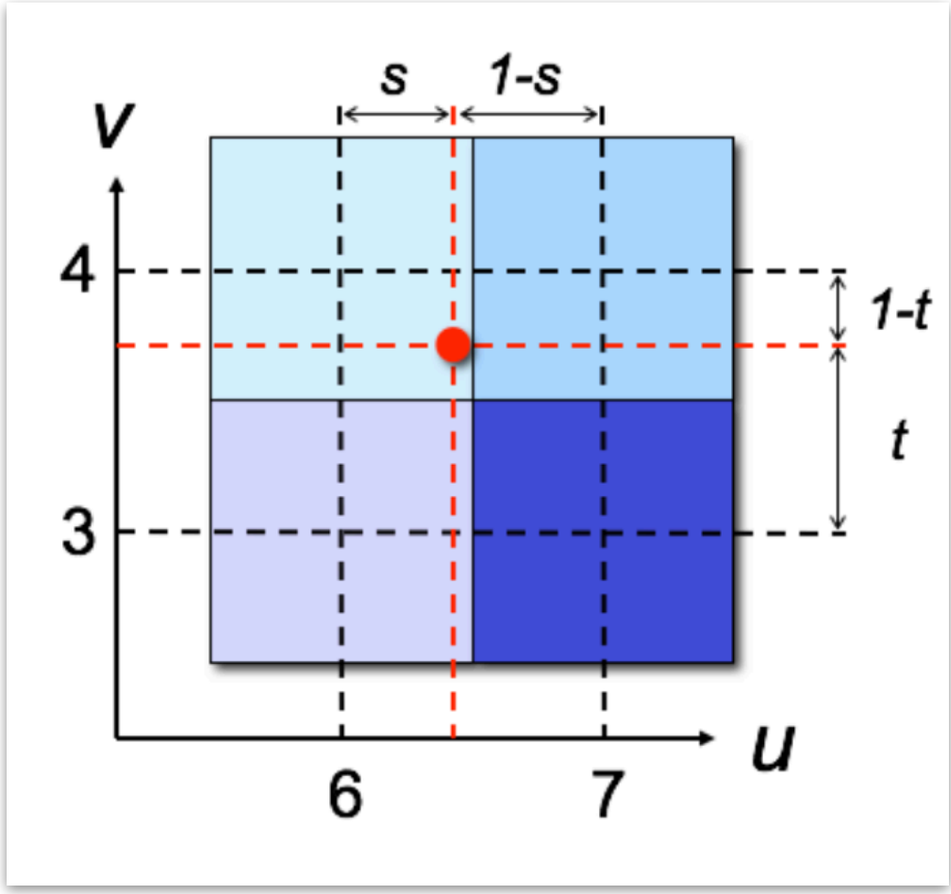
- Texture coordinates: (u,v) pair defines a texel coordinate.

**Example 2x2 texture being sampled**

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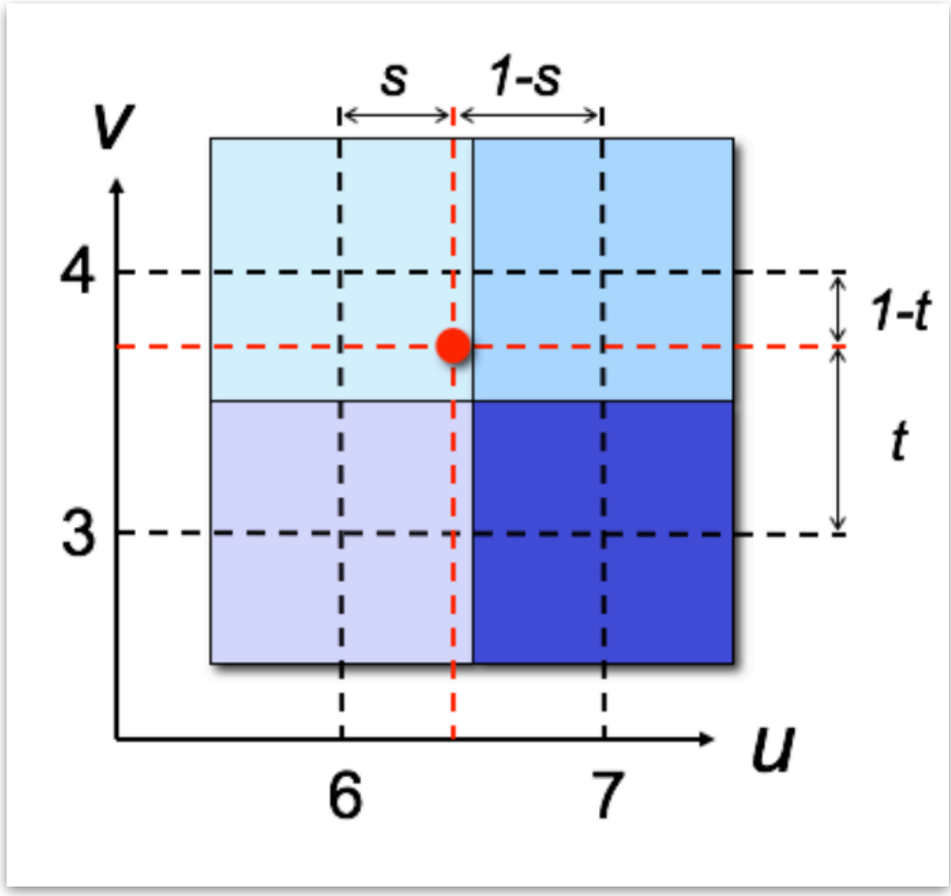


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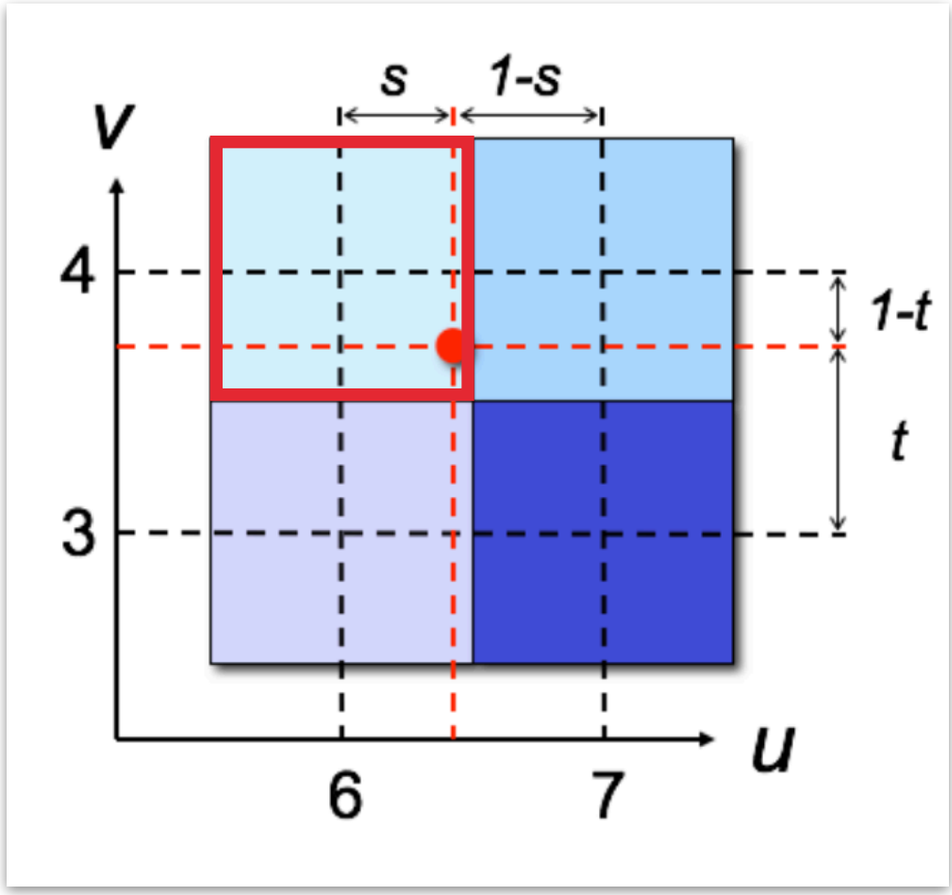


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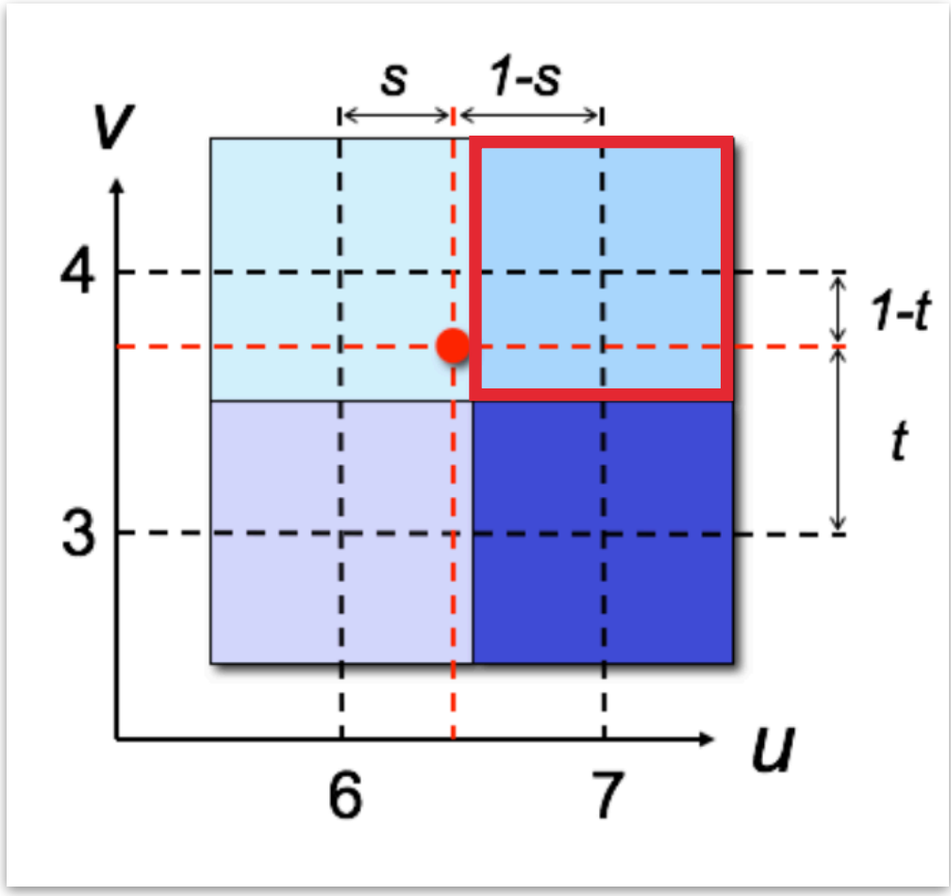


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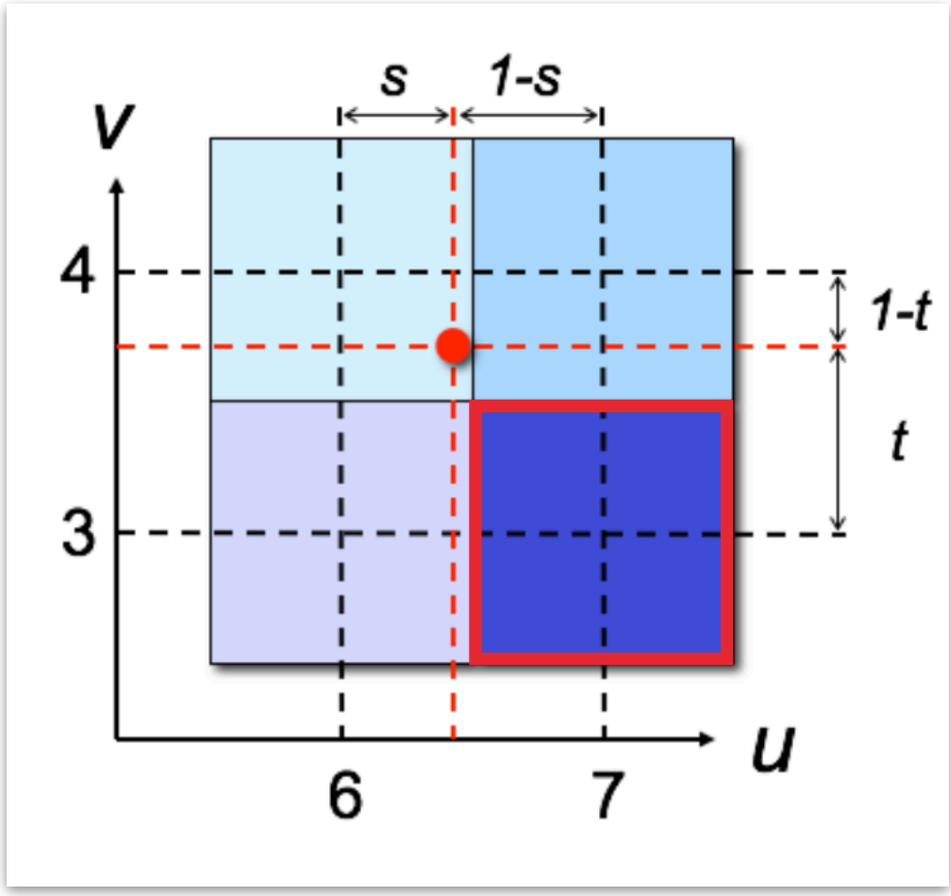


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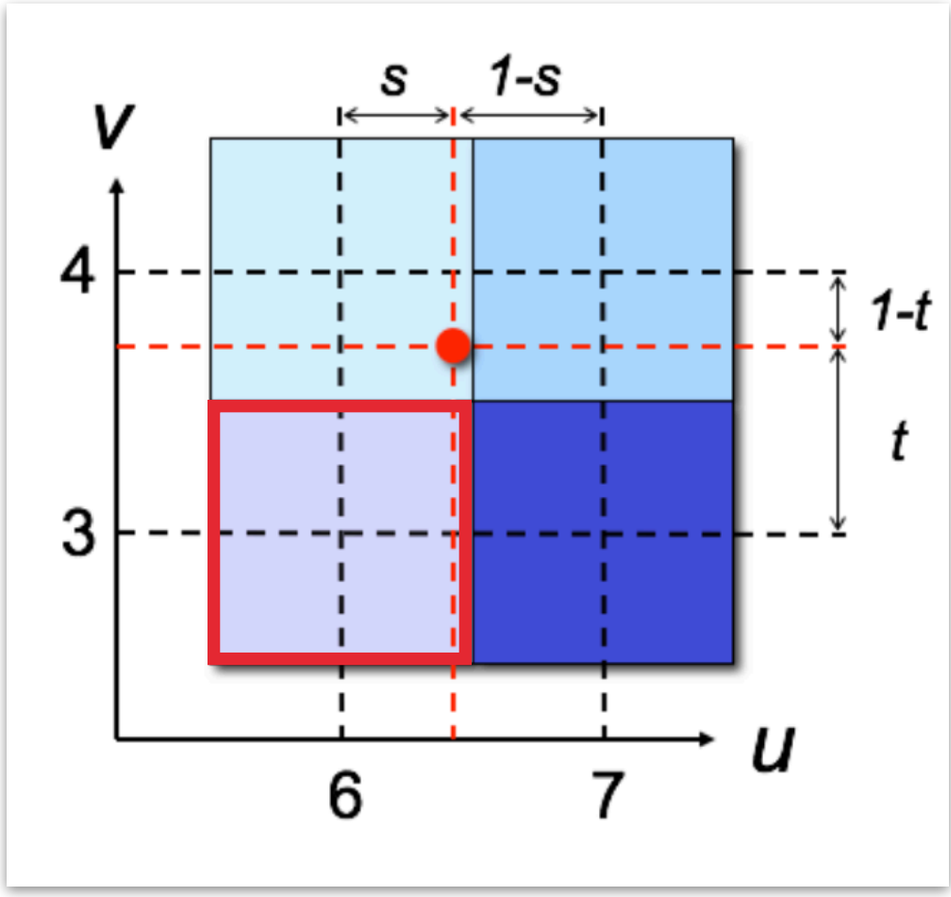


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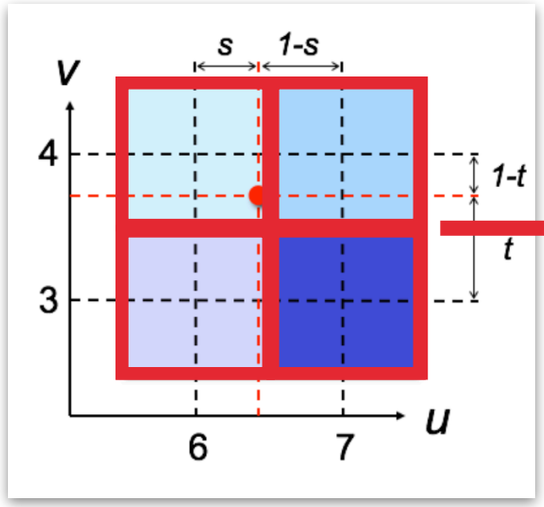
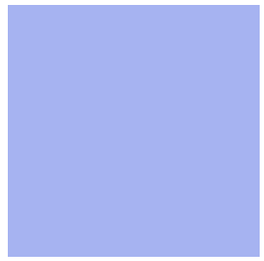



**Resulting Filtered Texel**



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- Every sample requires **at least 4 memory requests**.

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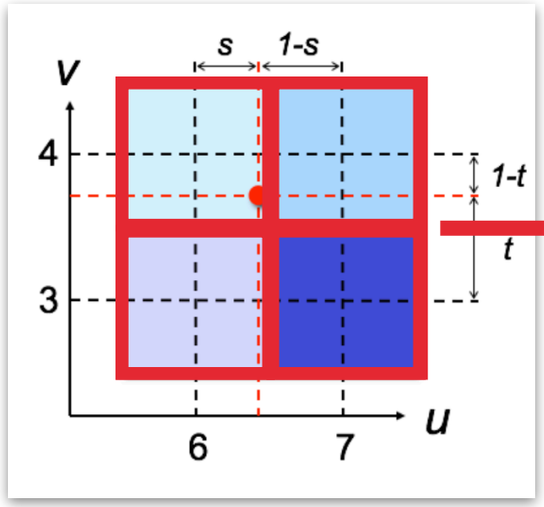


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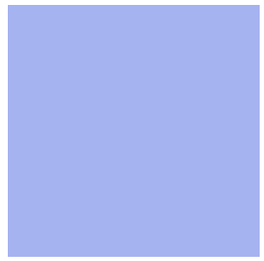

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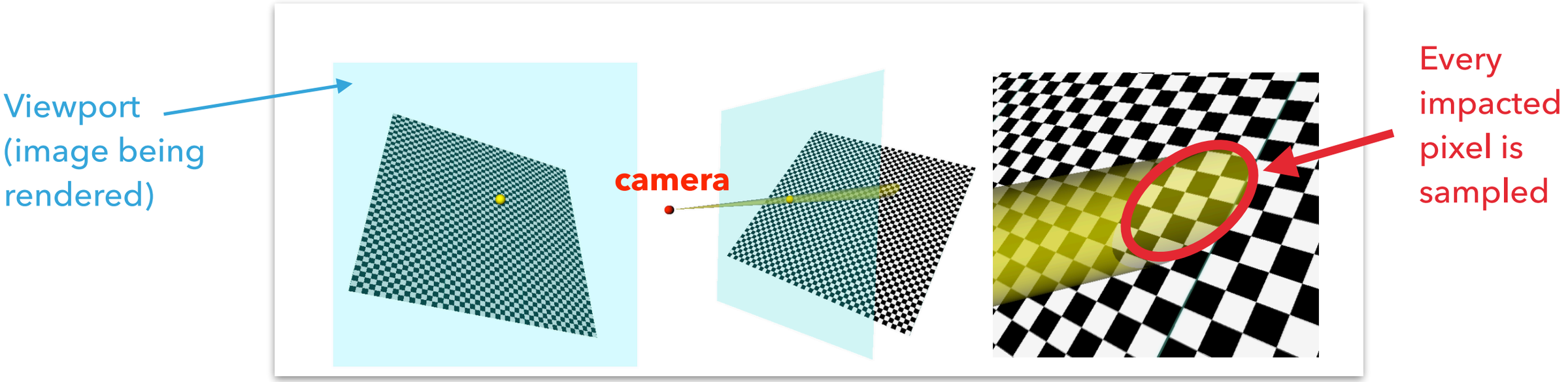


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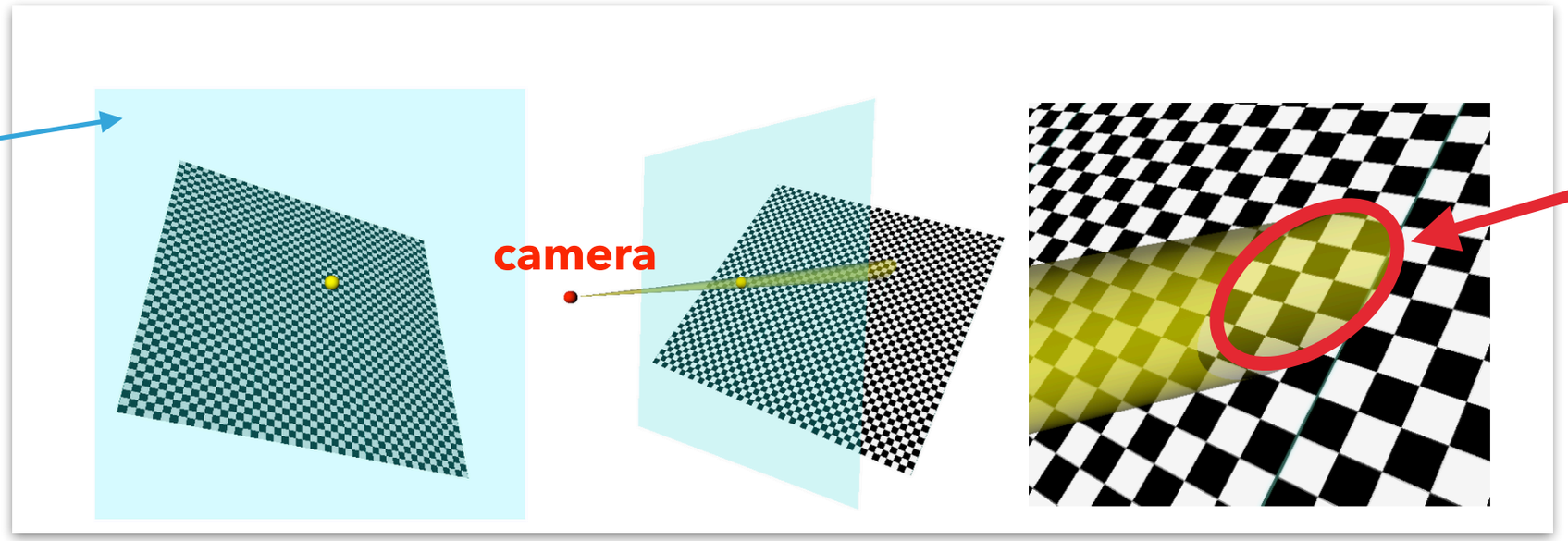


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- Ex: **16x anisotropic filtering:**
  - 16x2x4 = 128 texels ==> **32x bilinear filtering**.

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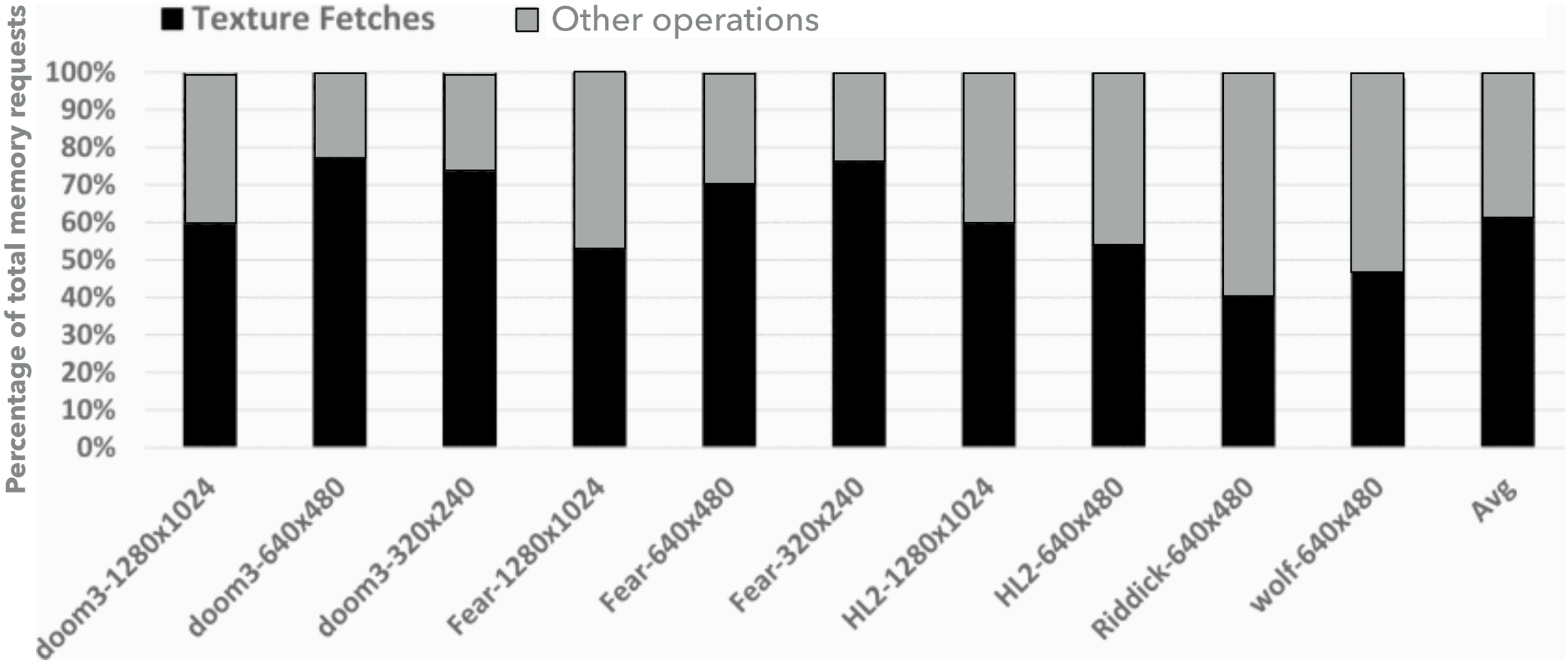
Texture Fetches
Other operations
Percentage of total memory requests
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
doom3-1280x1024
doom3-640x480
doom3-320x240
Fear-1280x1024
Fear-640x480
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HL2-1280x1024
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Riddick-640x480
wolf-640x480
Avg

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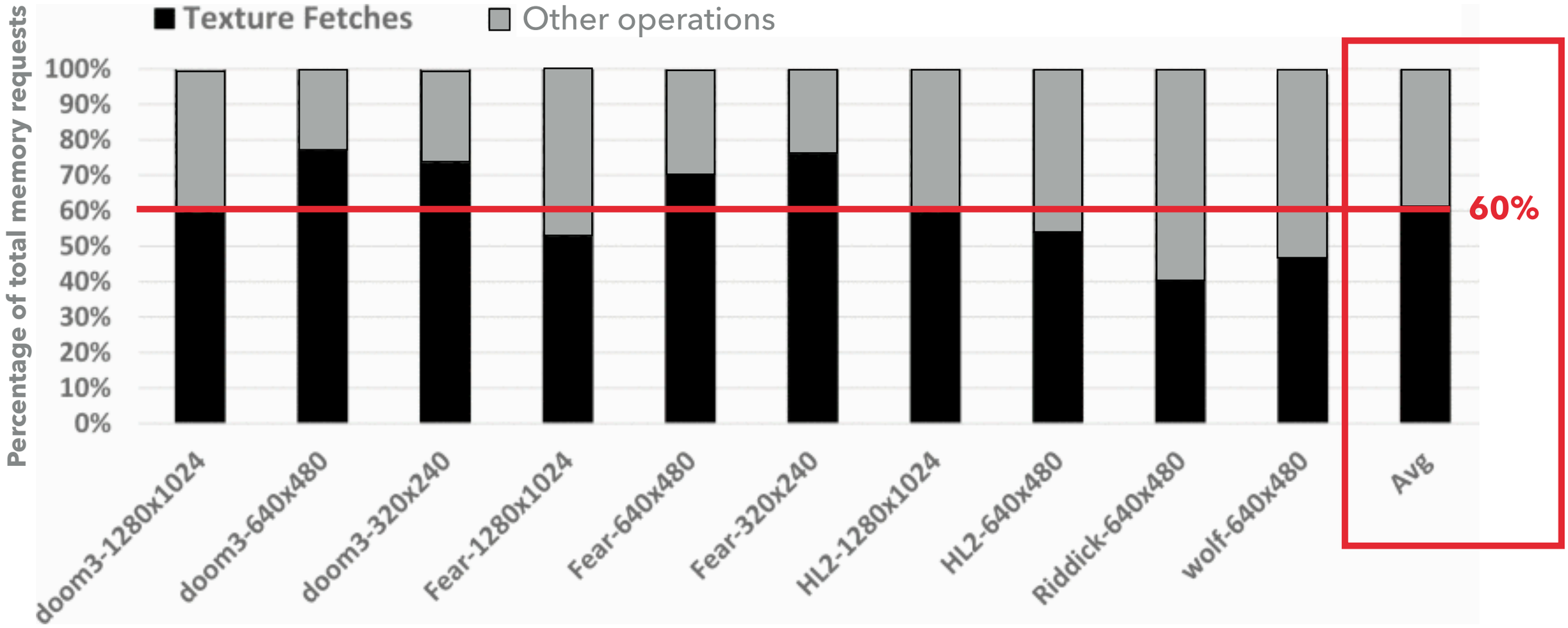


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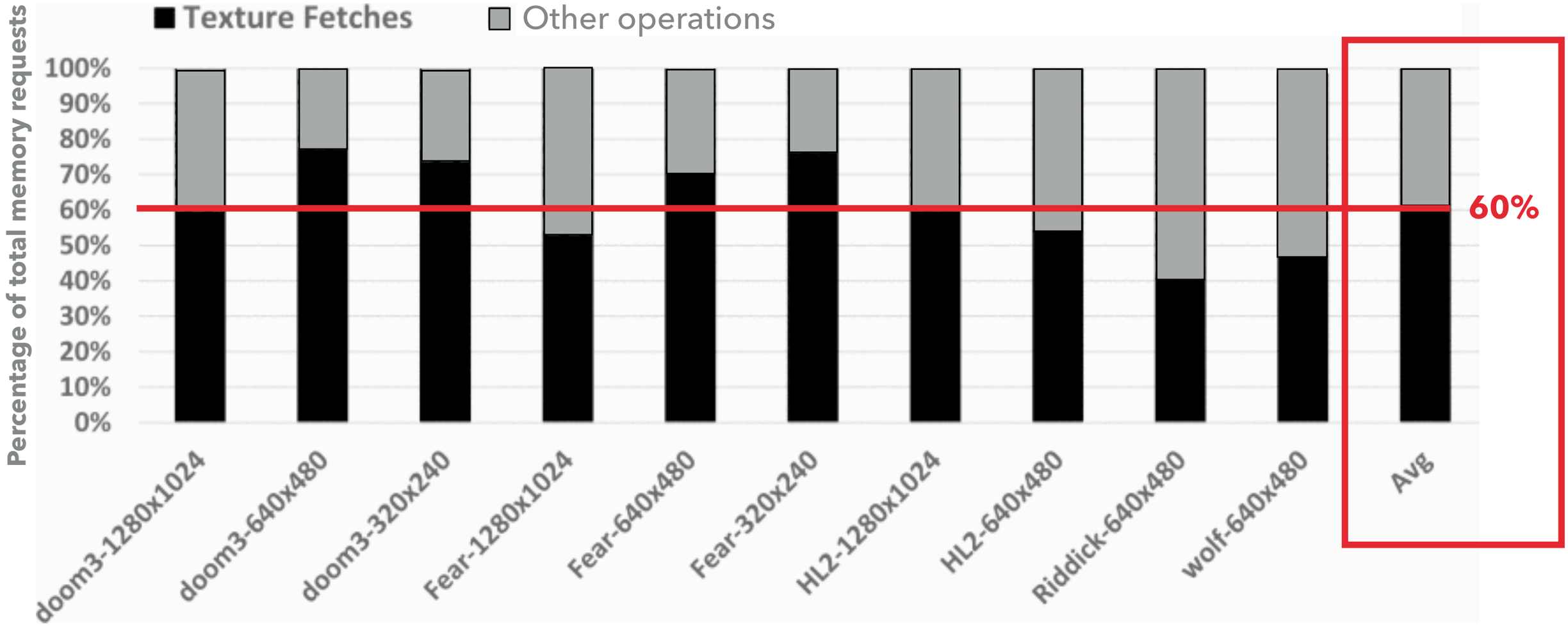


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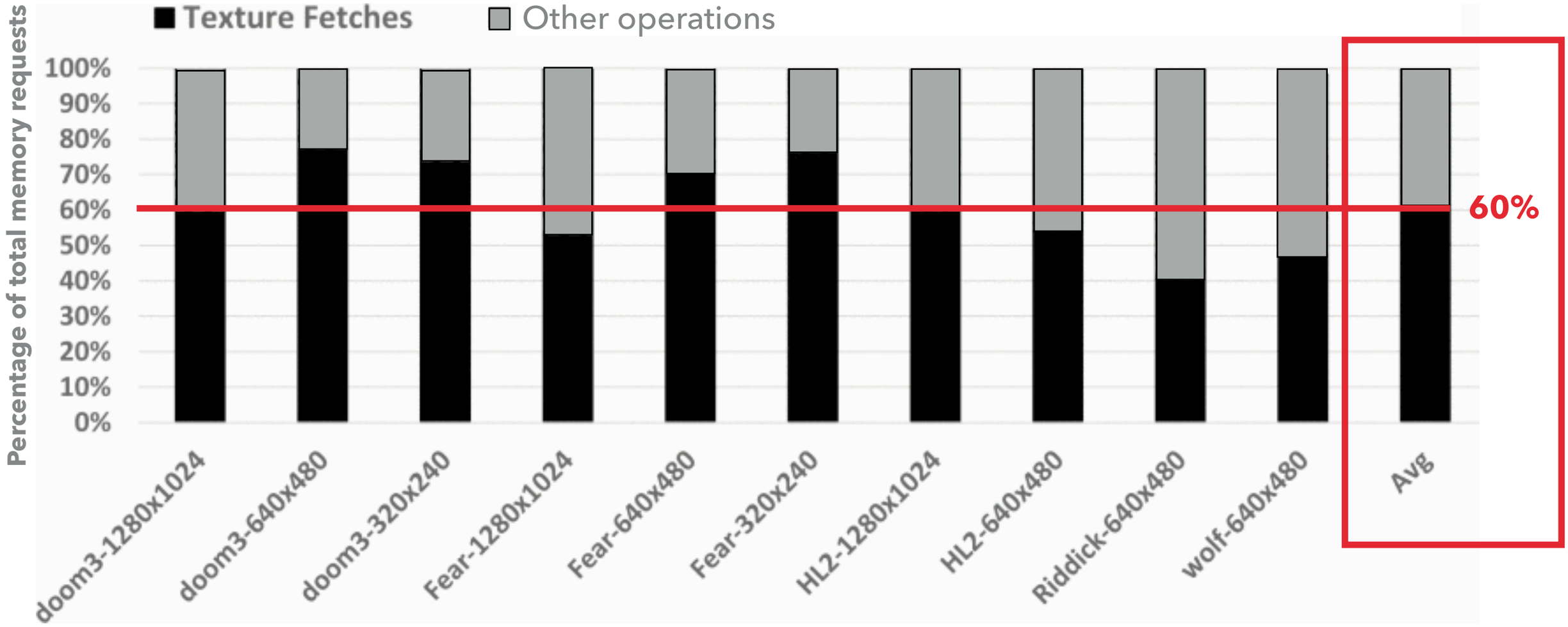


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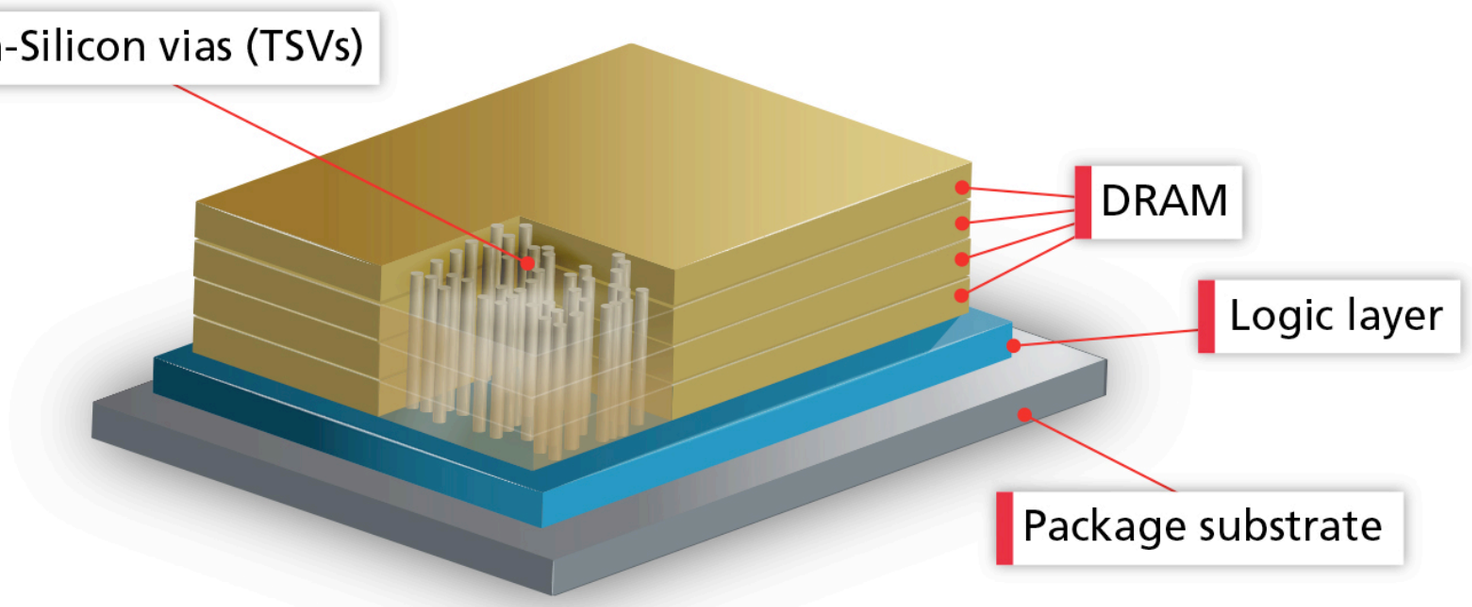
- Idea: Replace GPU memory with Hybrid Memory Cube.
- **Hybrid Memory Cube**: High bandwidth 3D stacked DRAM technology with a logic layer at the base.
- Vertical connection = **Through-Silicon Via** (TSV):
  - **Internal** bandwidth (connection to logic layer):
    - **512 GB/s**
  - **External** bandwidth (connection to host):
    - **320 GB/s**

*[2]: https://community.cadence.com/cadence_blogs_8/b/fv/posts/what-s-new-with-hybrid-memory-cube-hmc*




HMC Memory Chip Architecture

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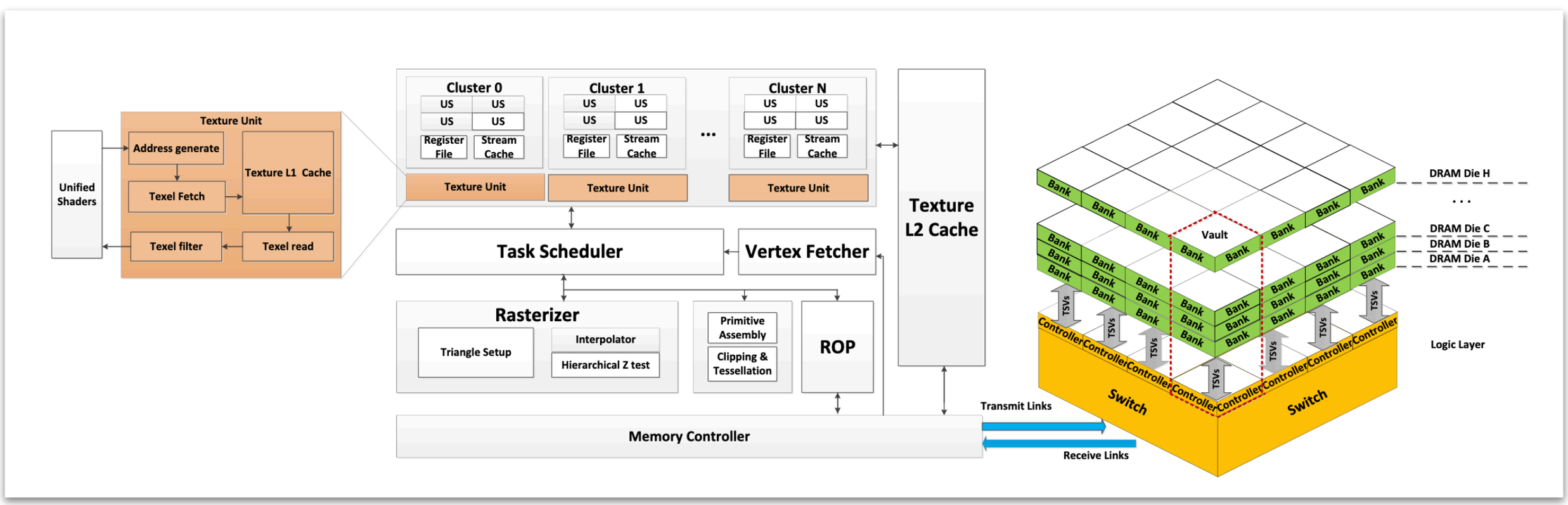

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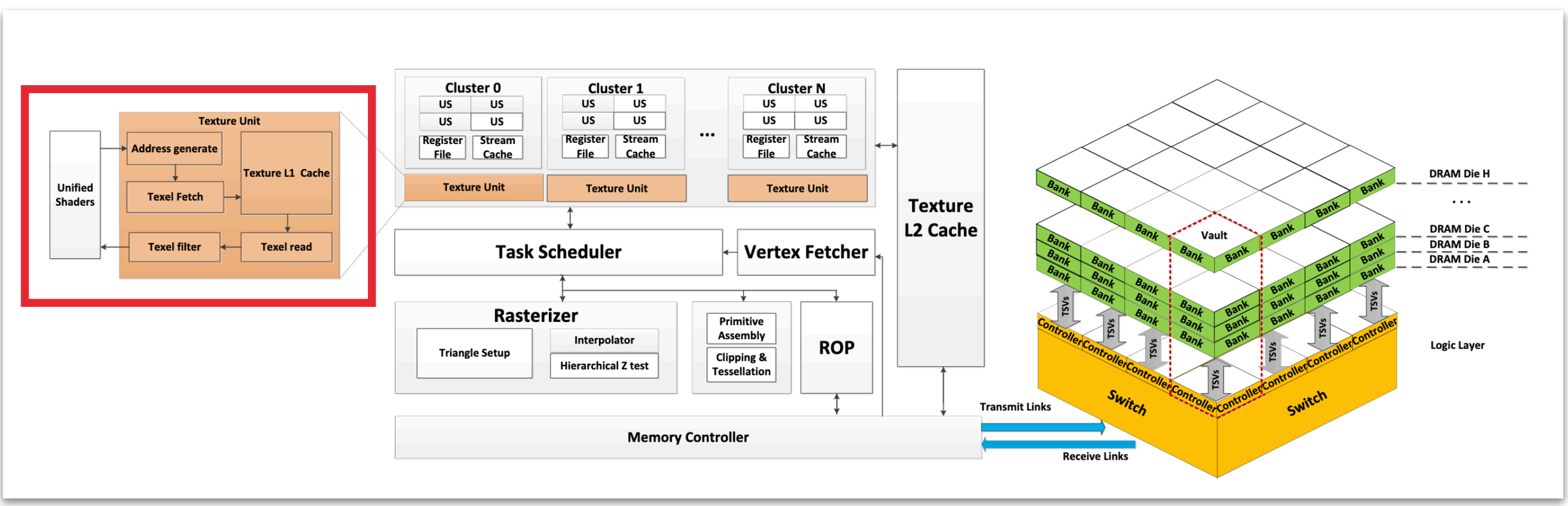

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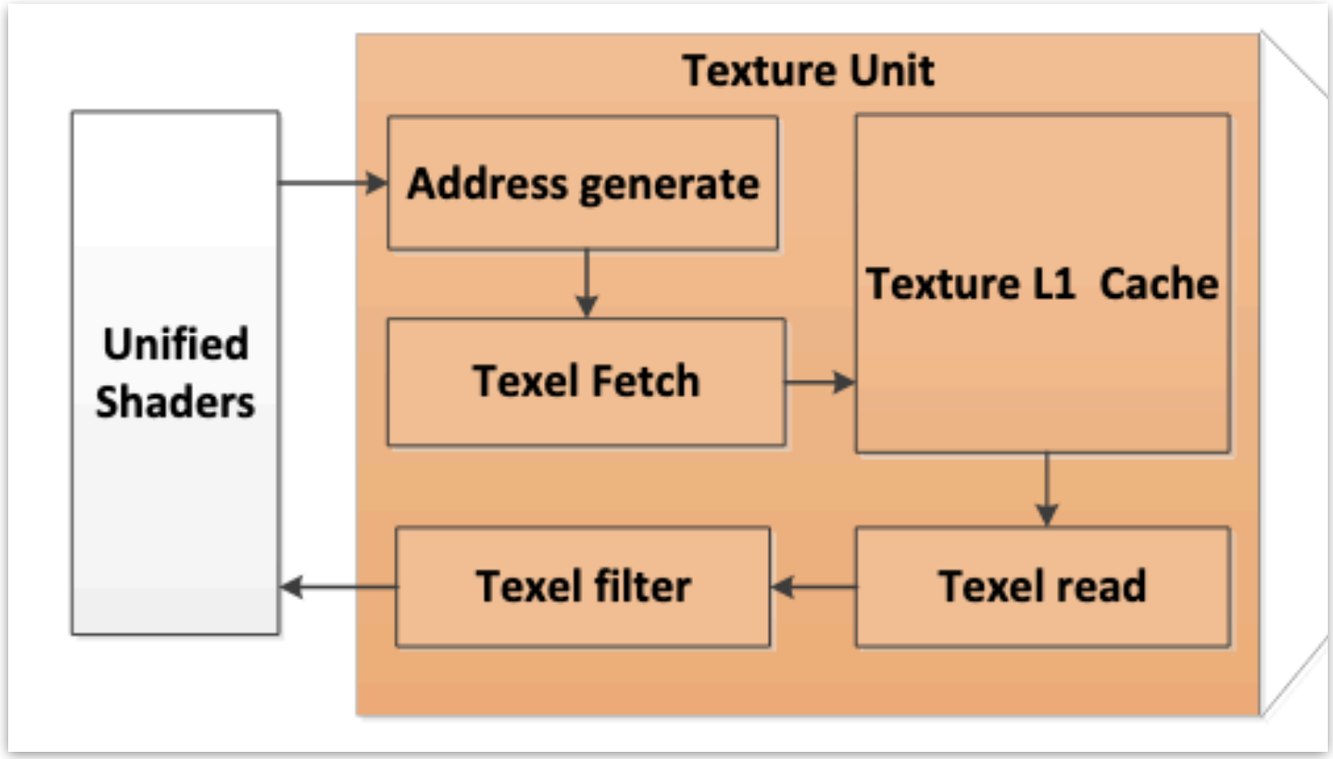


- **Problem**: Doesn't exploit internal bandwidth of HMC.

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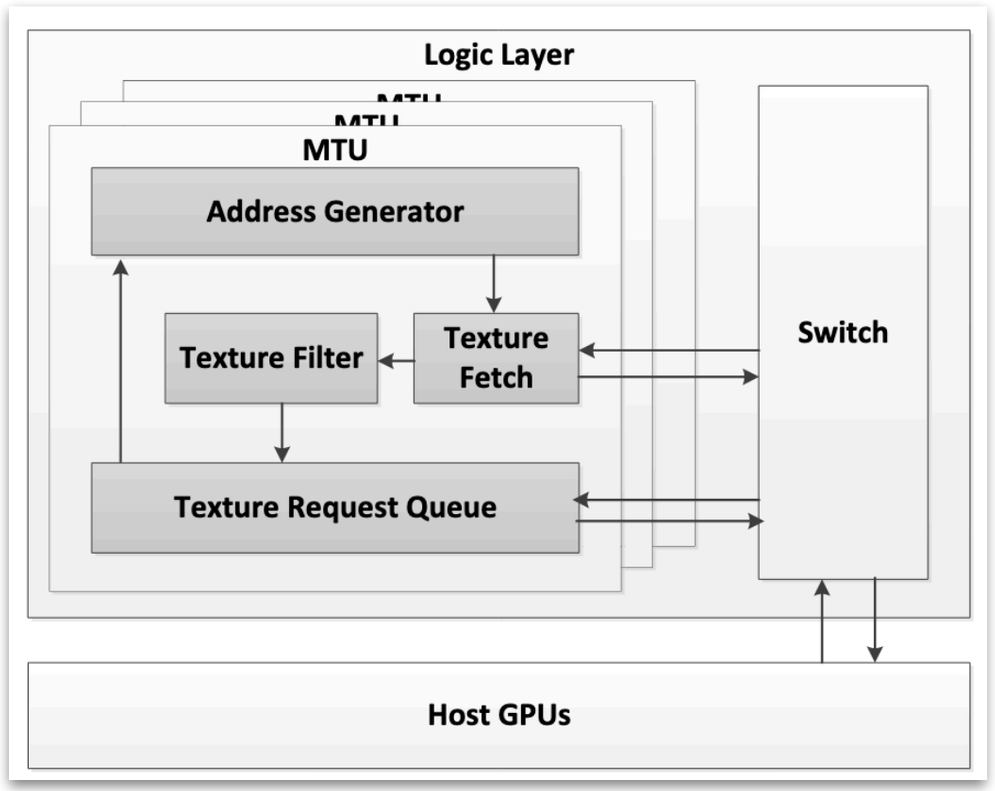
## Overview of S-TFIM architecture



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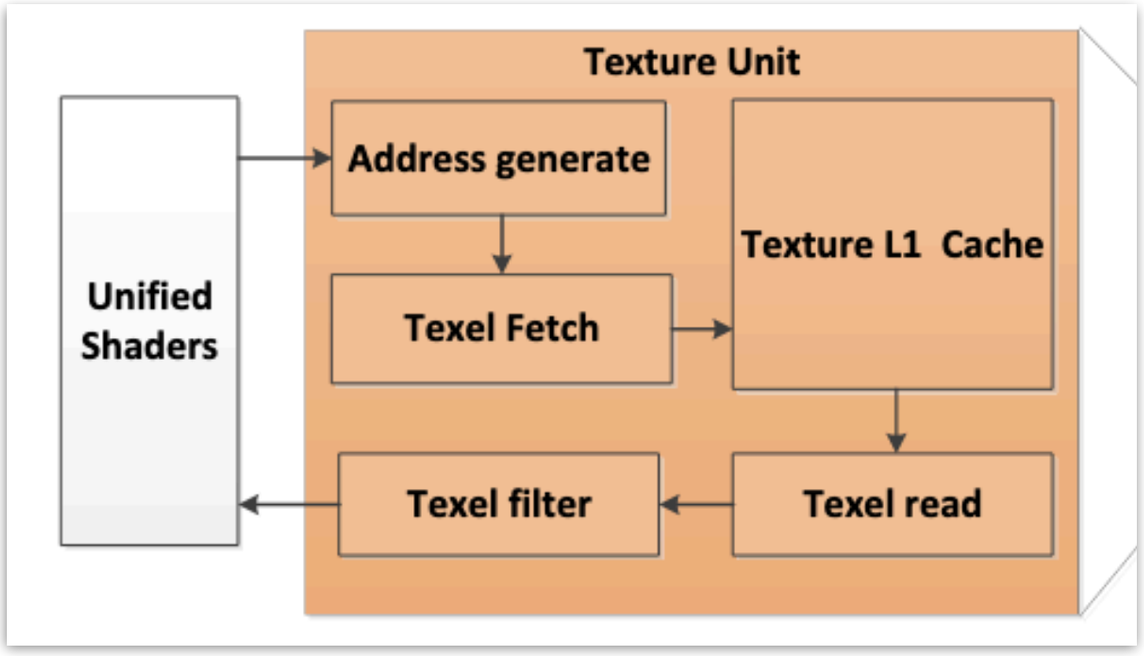
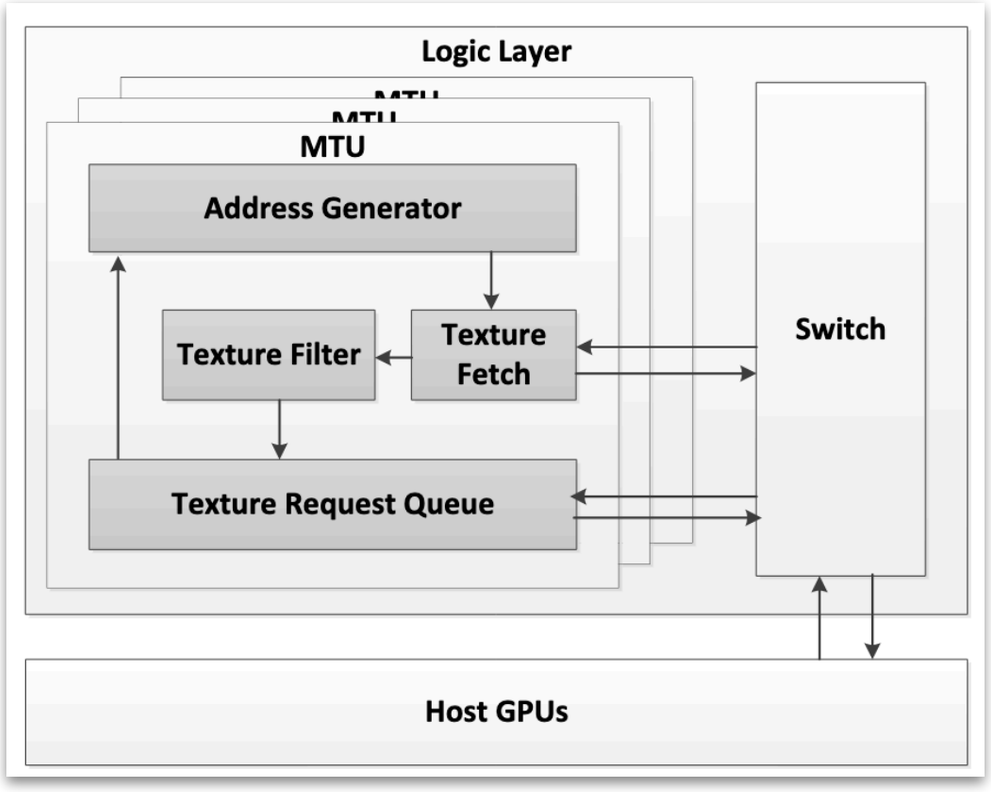


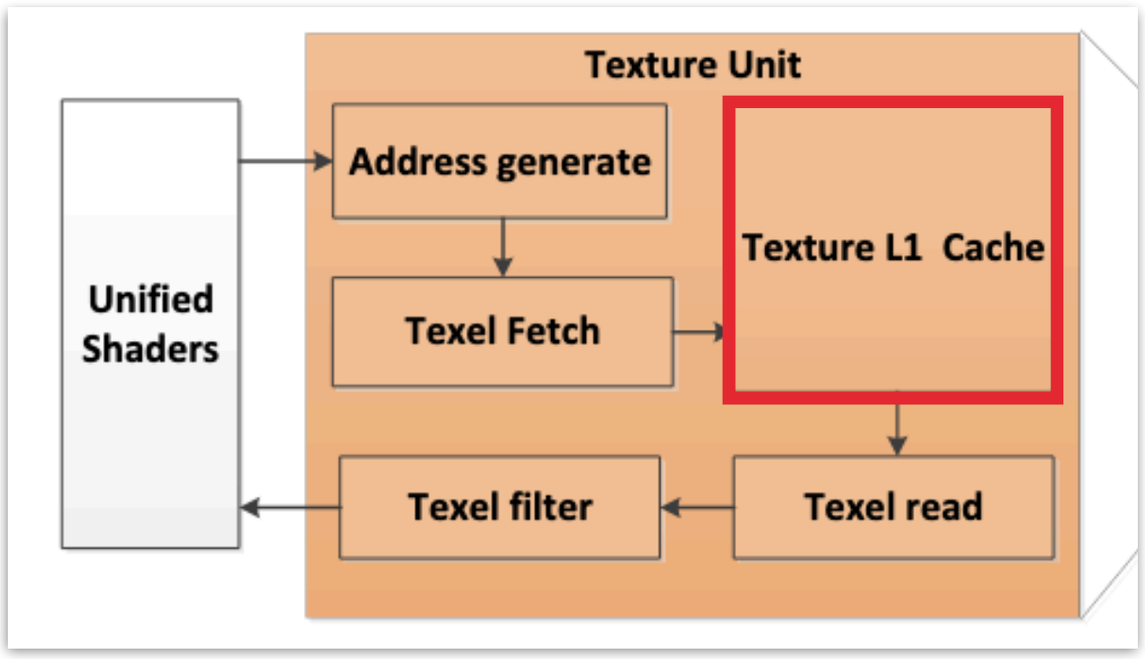

**Overview of S-TFIM architecture**



# S-TFIM: SIMPLE TEXTURE FILTERING IN MEMORY

- Idea: Move **all texture filtering** to logic layer of HMC.
- Unified Shader (US) requests texel => HMC provides filtered texel.
- Memory Texture Unit (MTU): Does filtering in Logic layer of HMC.

**Overview of the B-PIM baseline Texture Unit**

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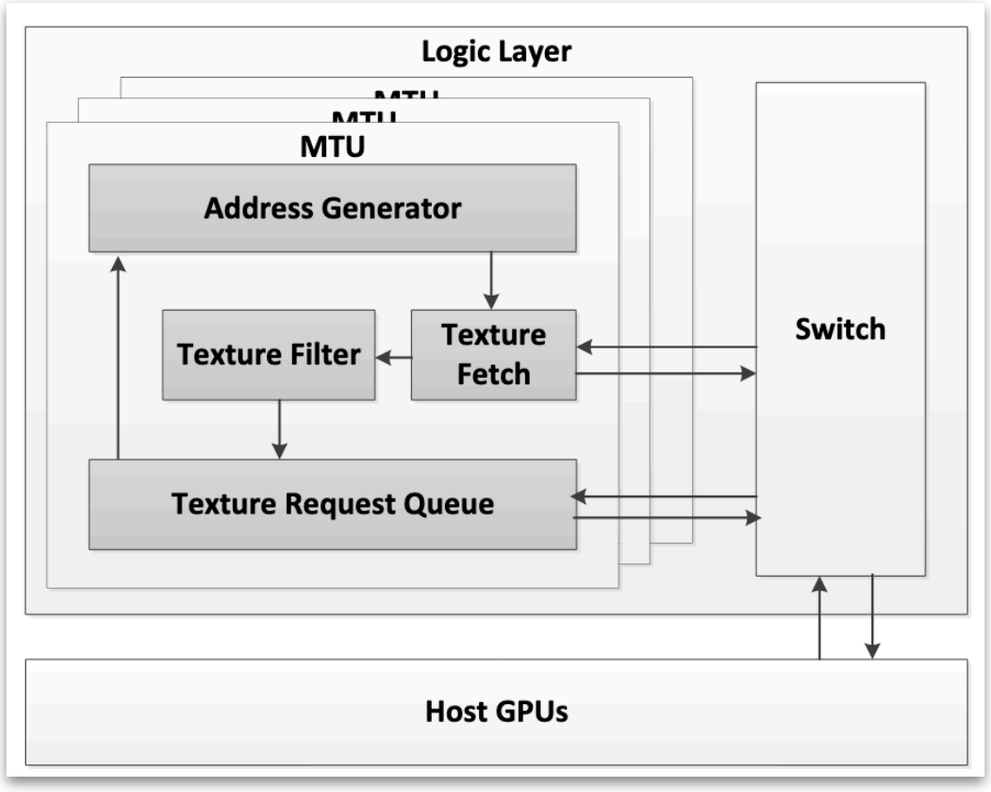


- **Problem**: Intermediate filtered-texel caching is no longer possible.

# OUTLINE

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- Two types of texels:
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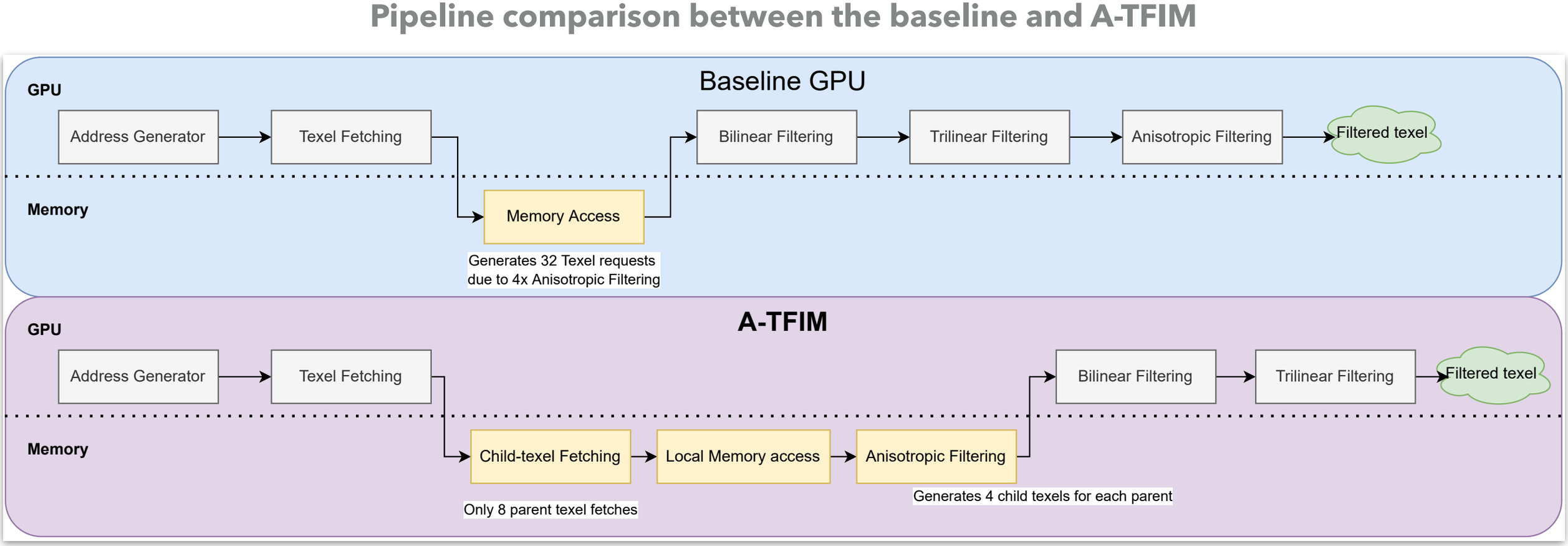

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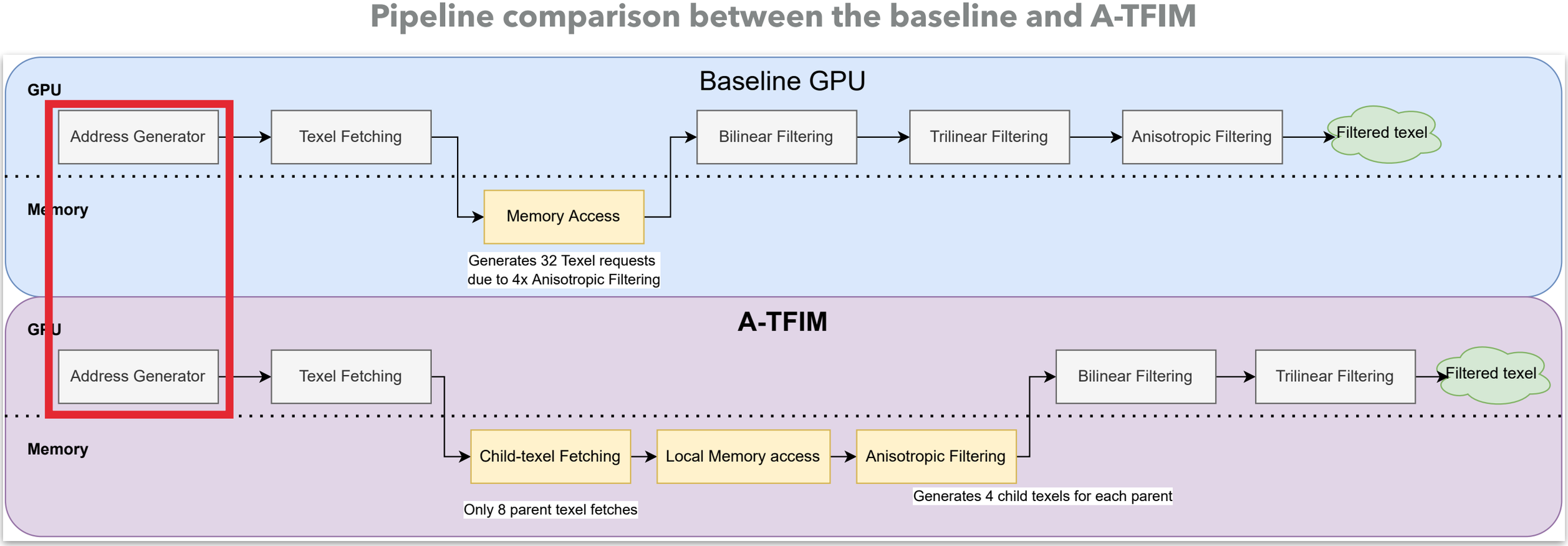

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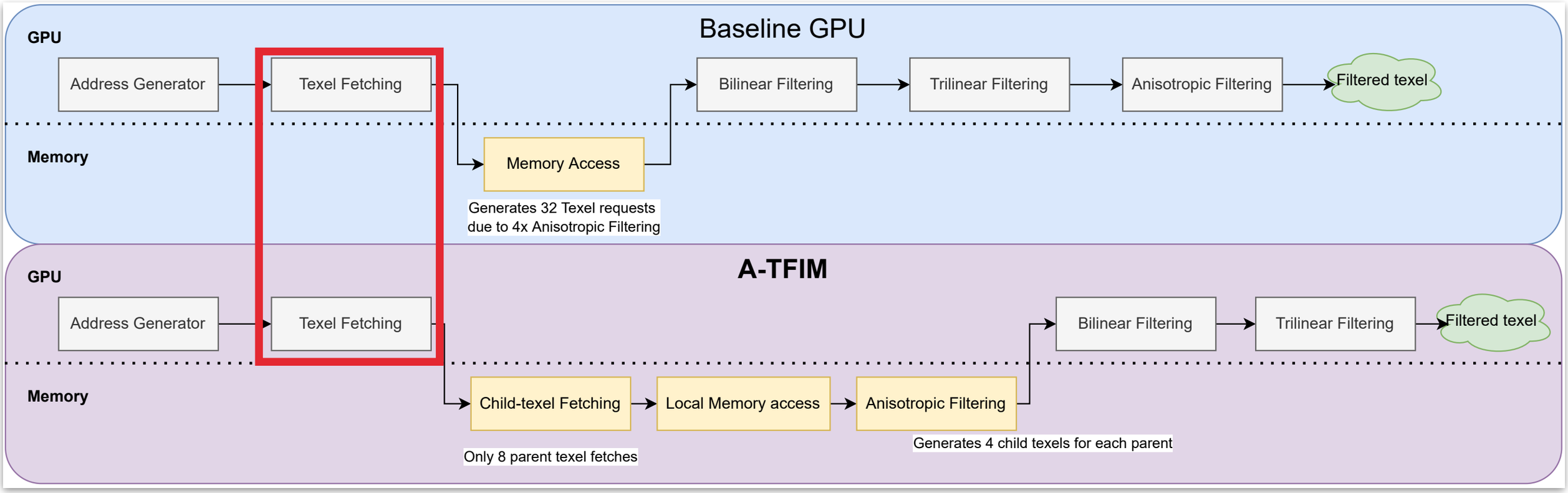

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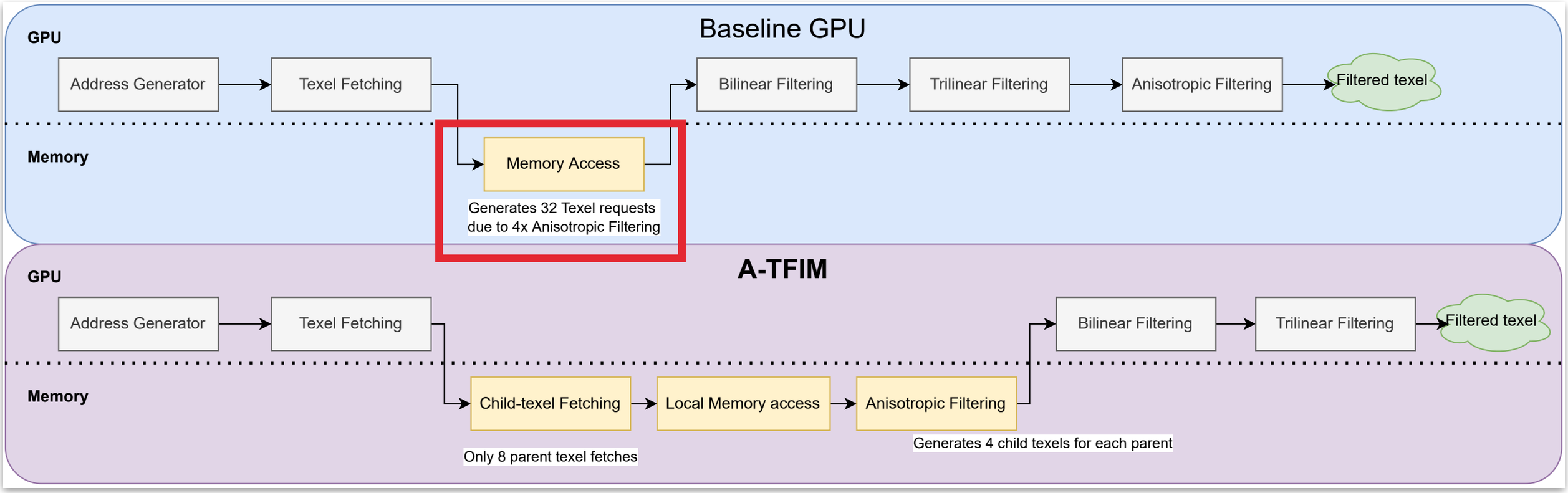

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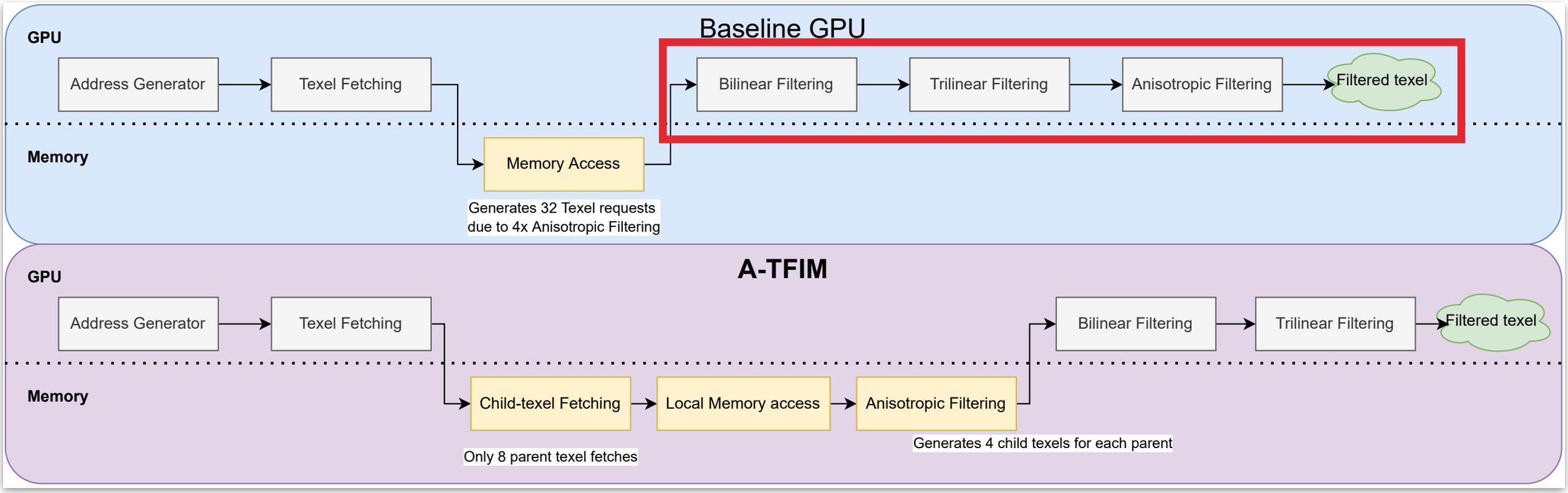

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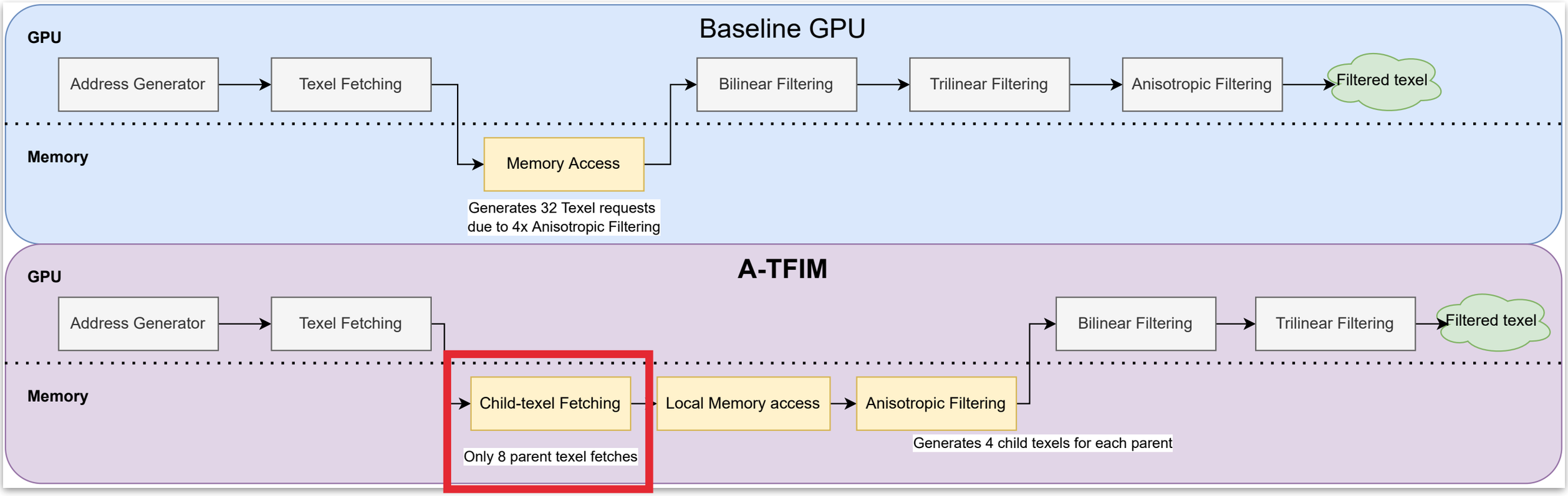

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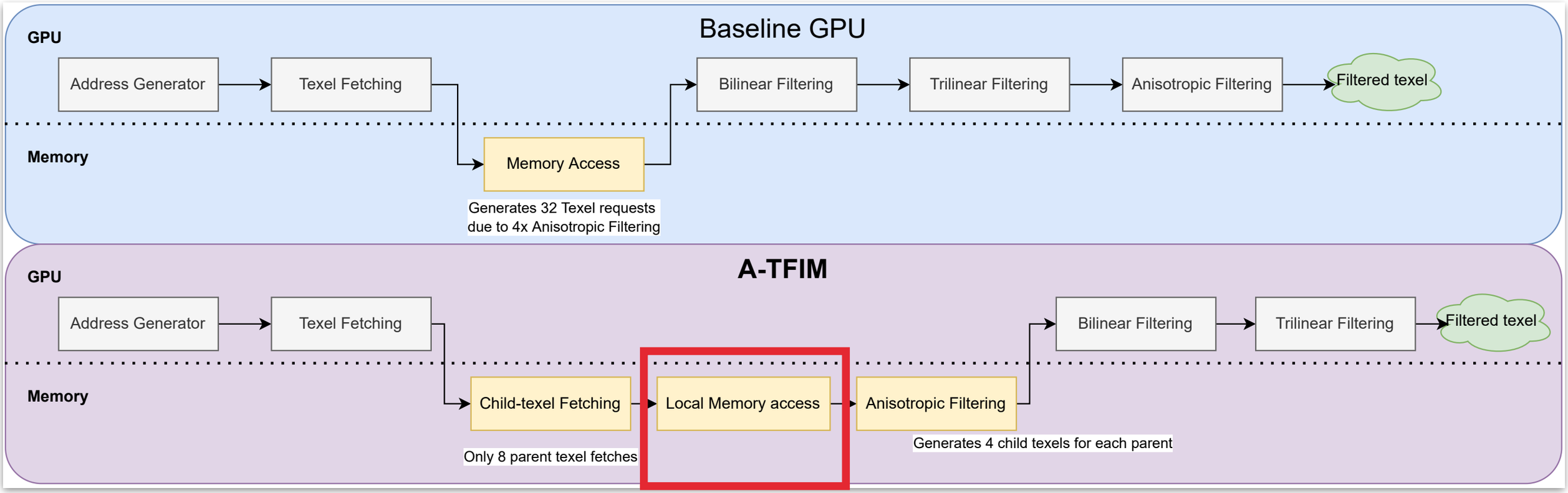

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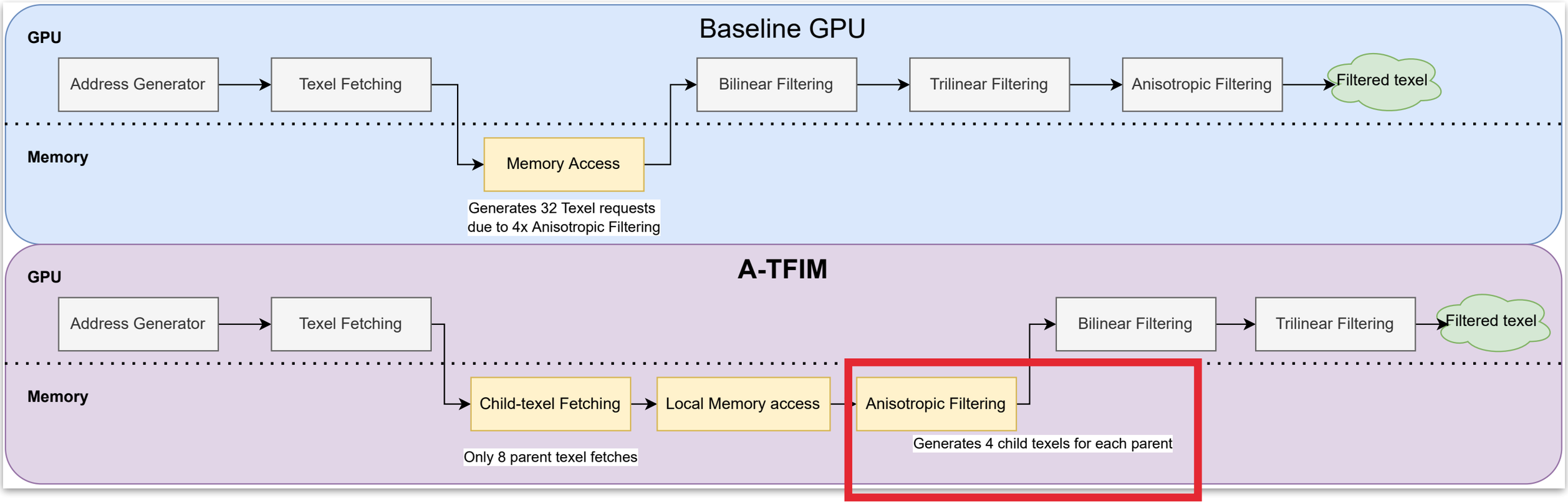

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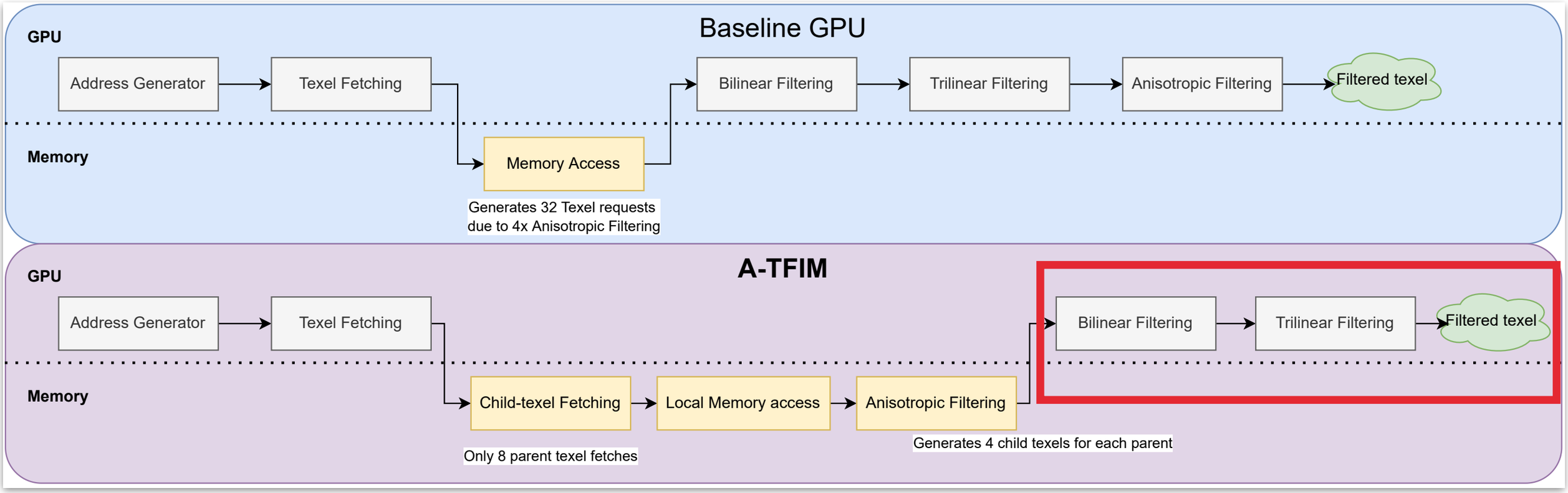


- **A-TFIM allows intermediate filtered texels to be cached like in baseline.**

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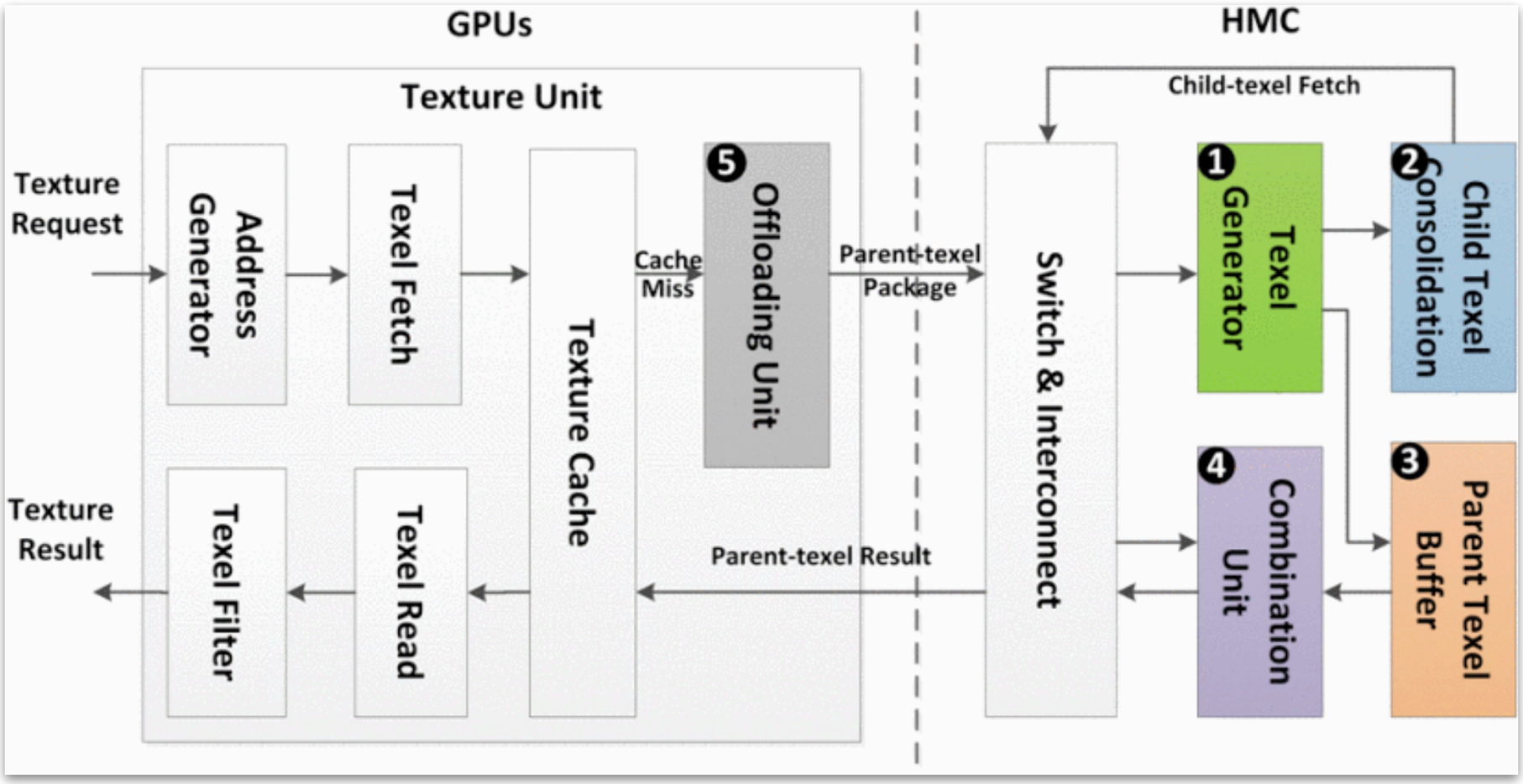

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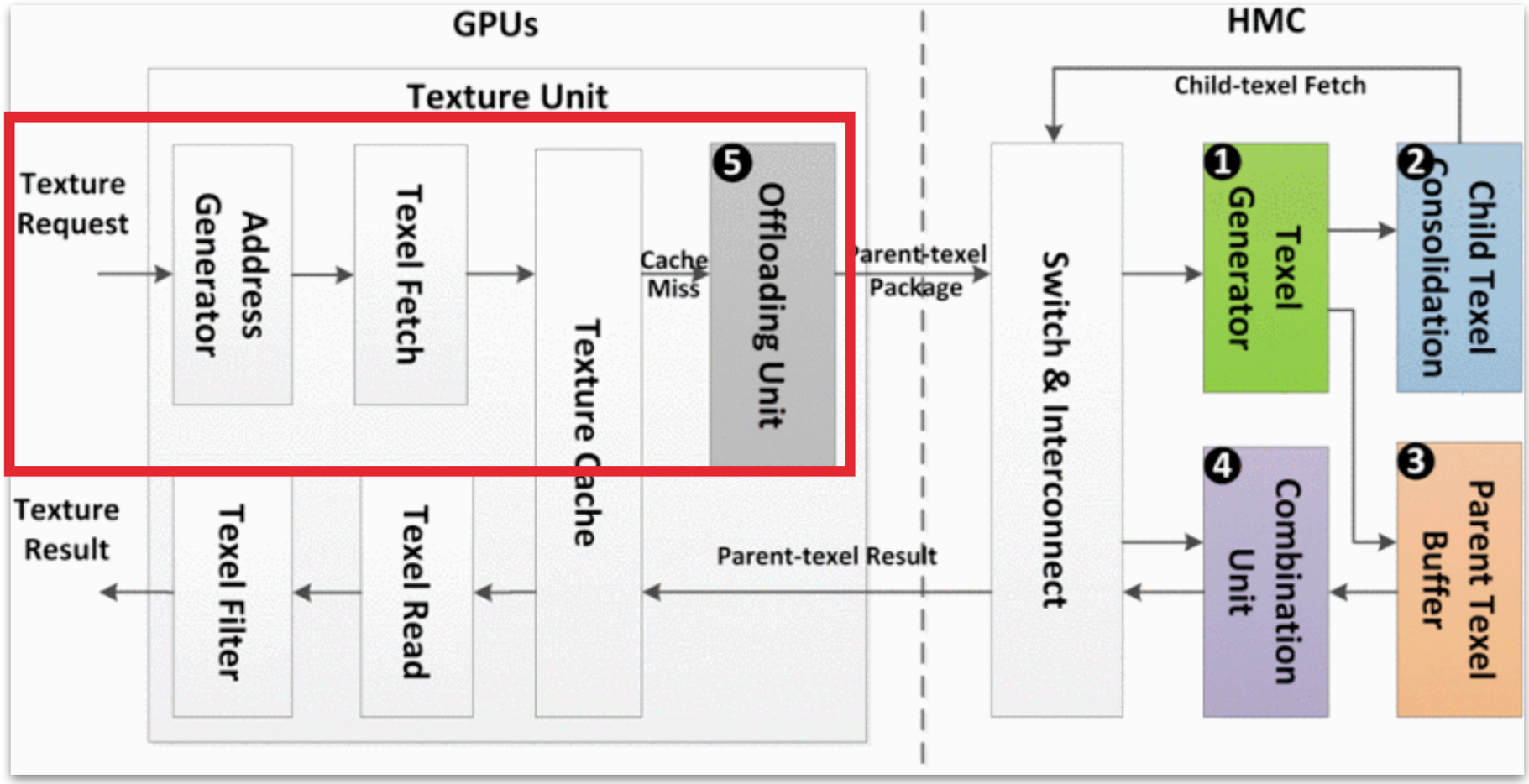

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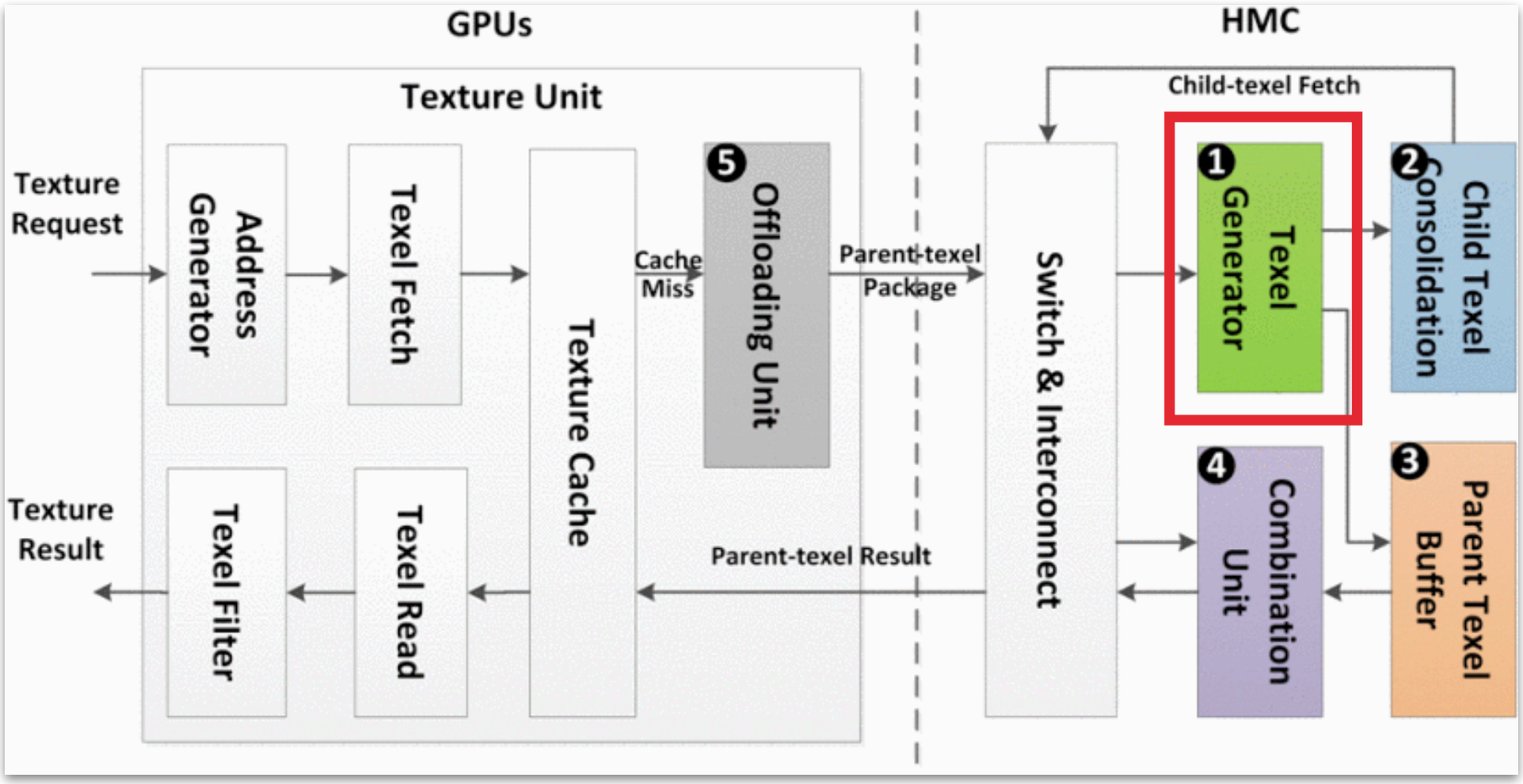

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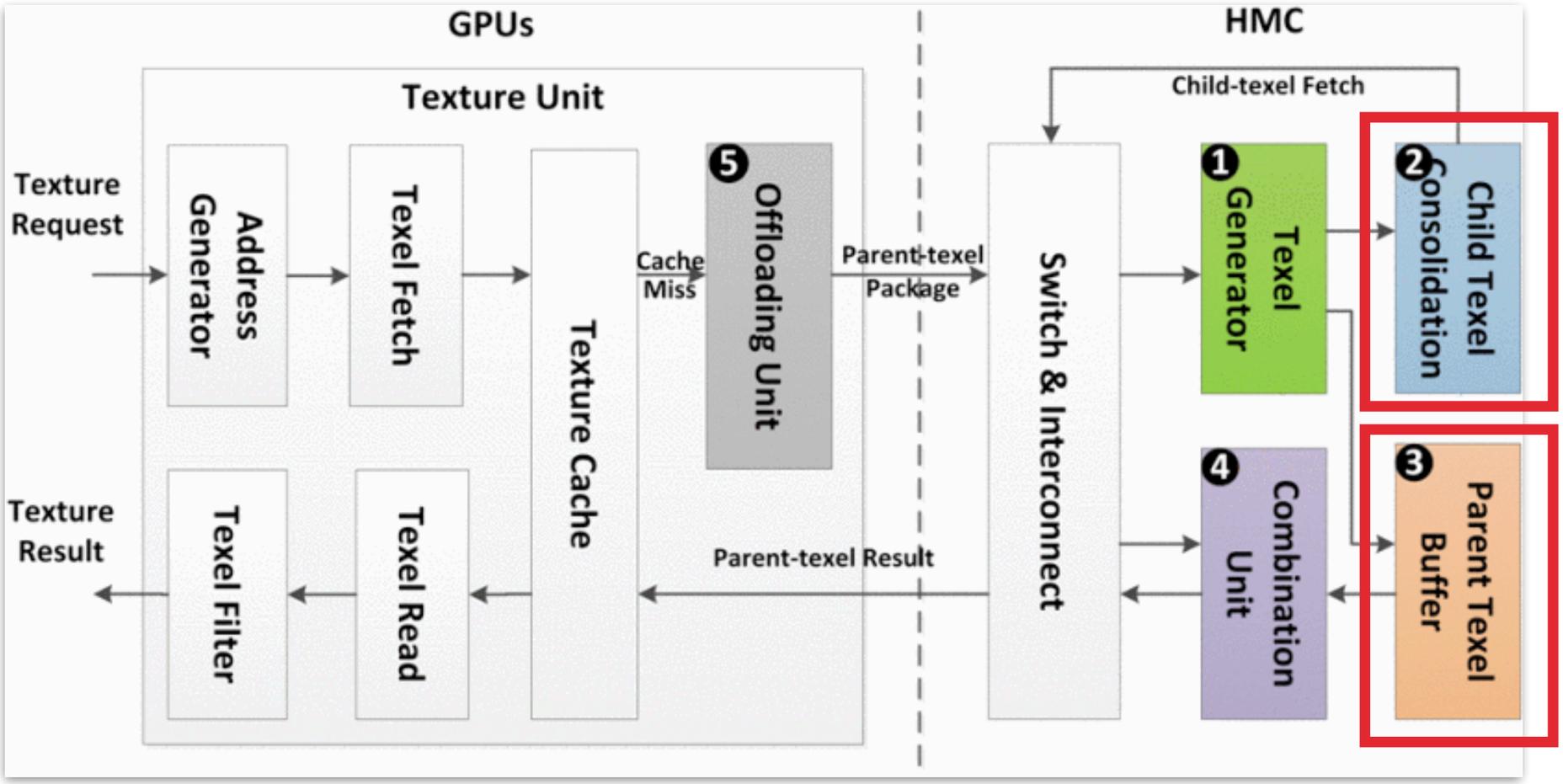

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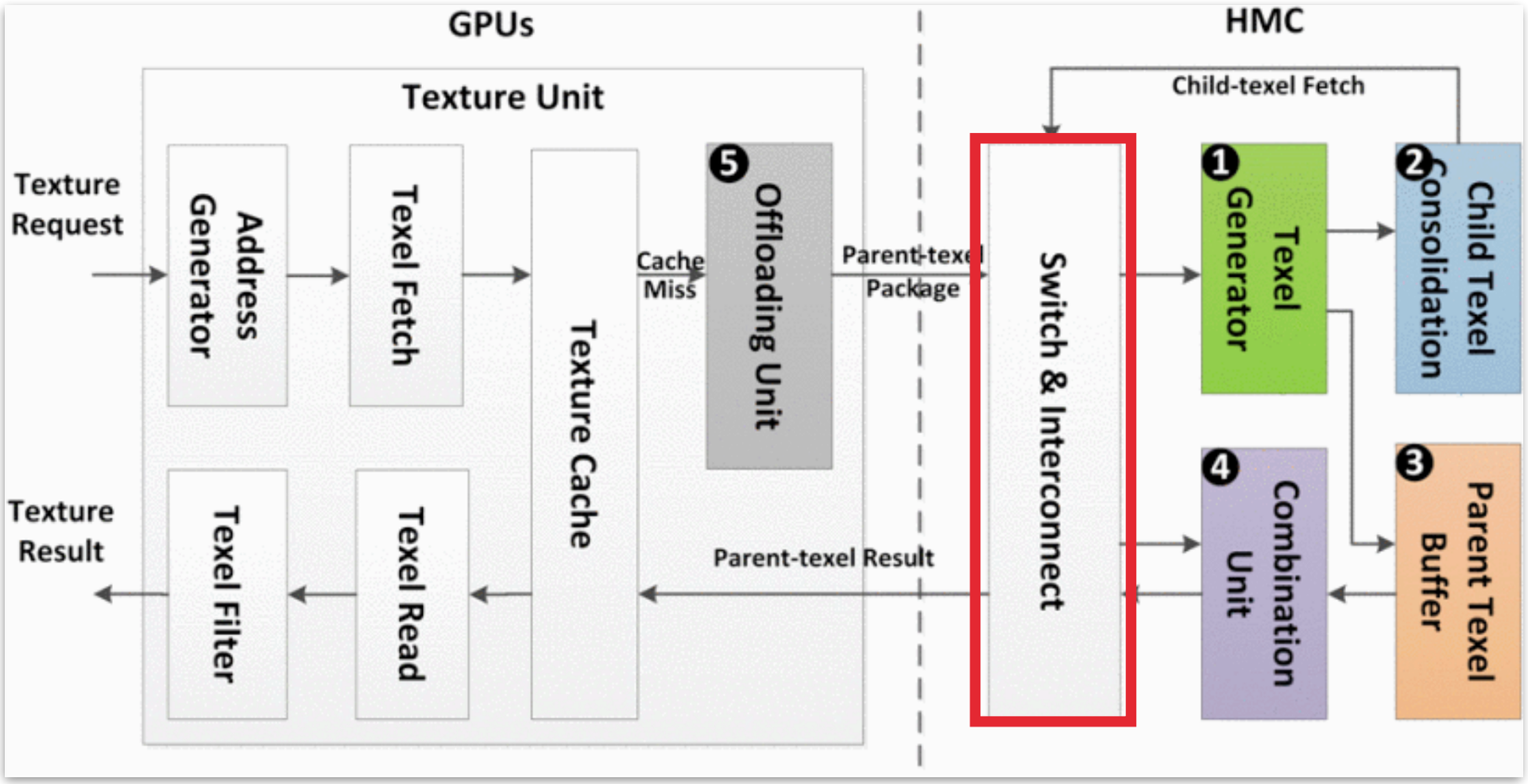

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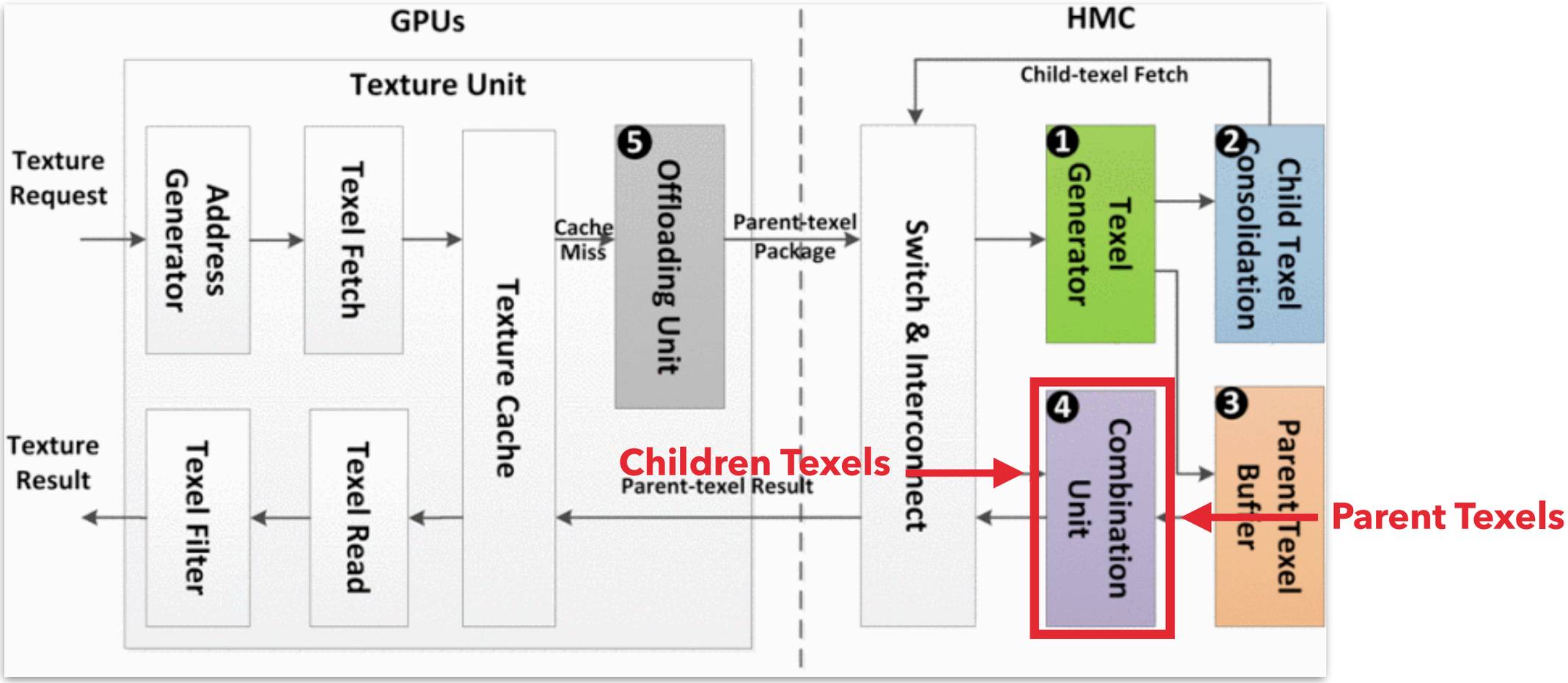


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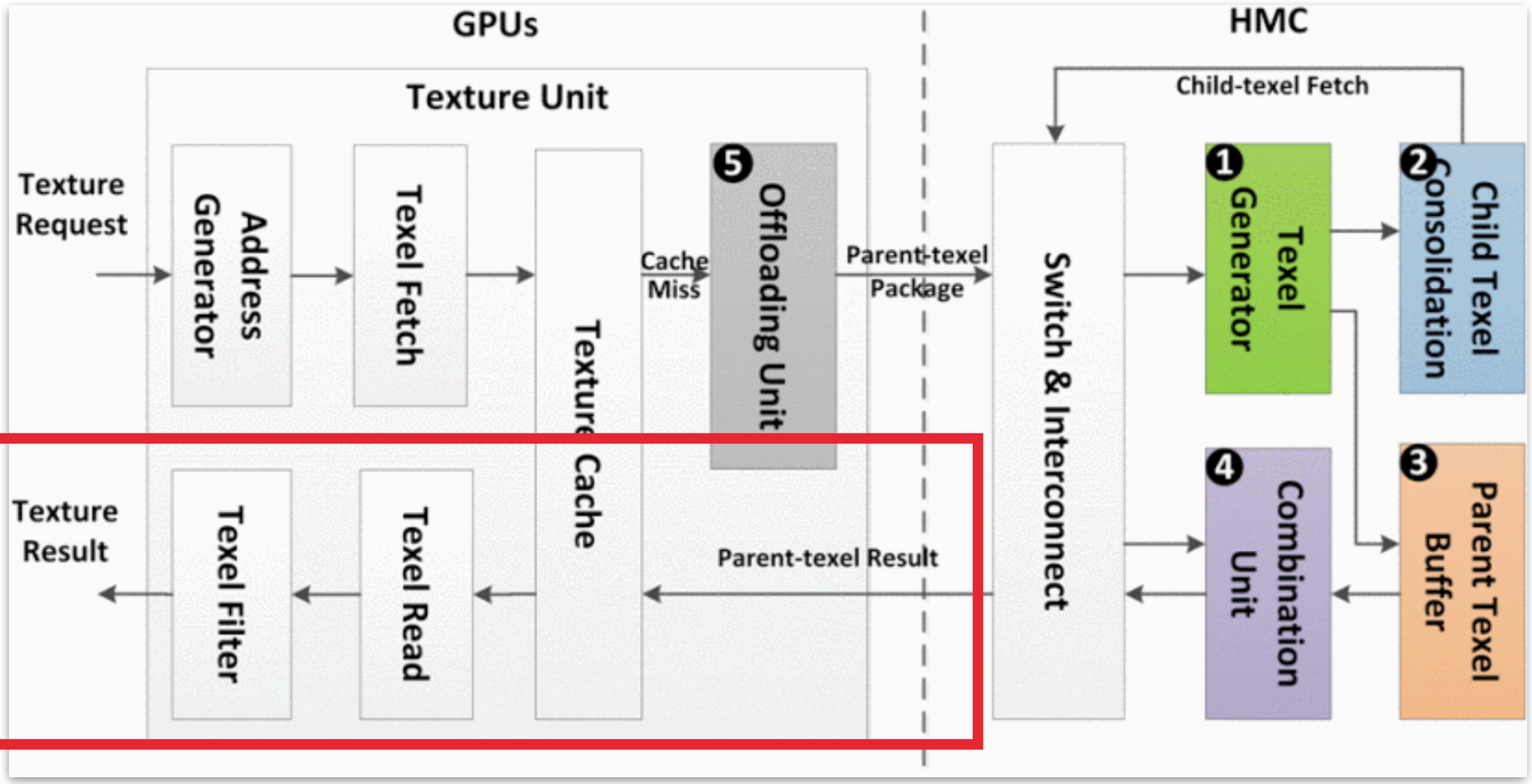

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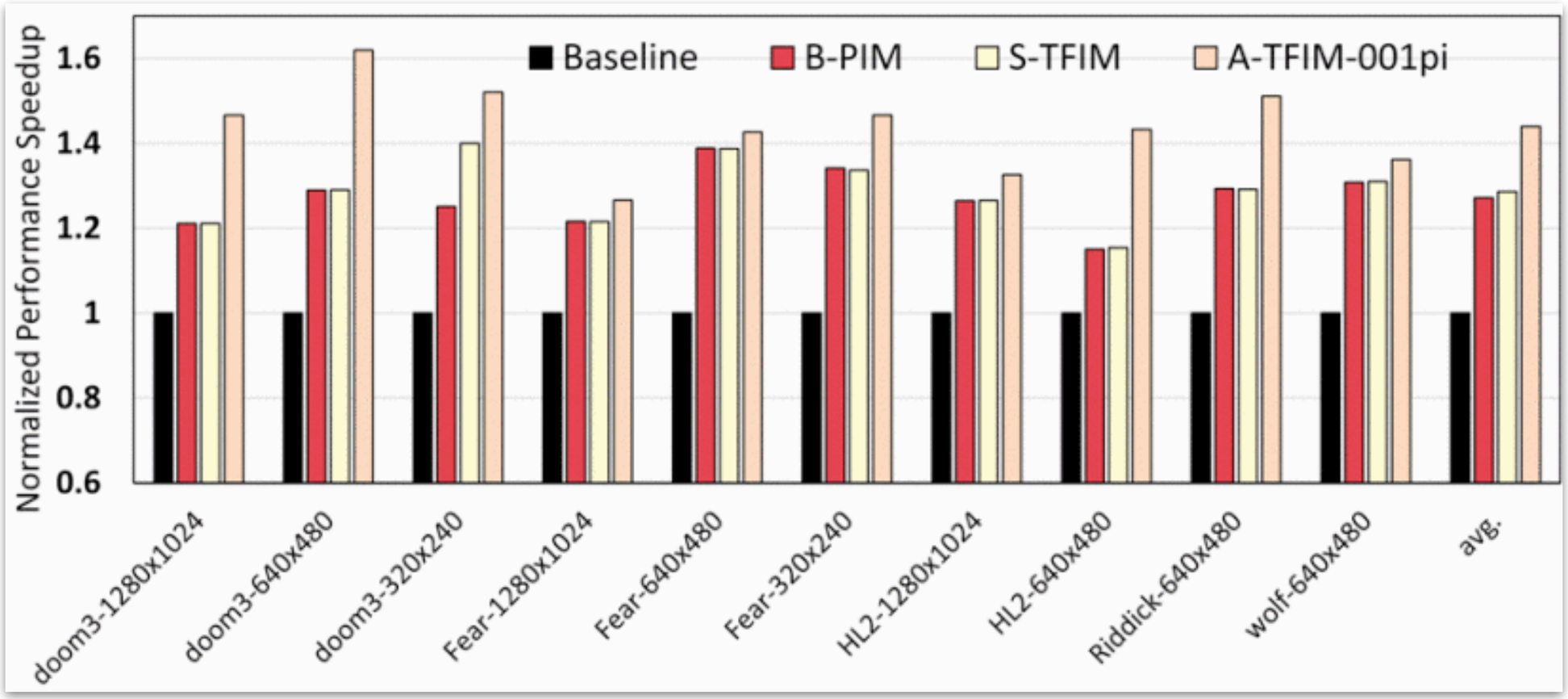

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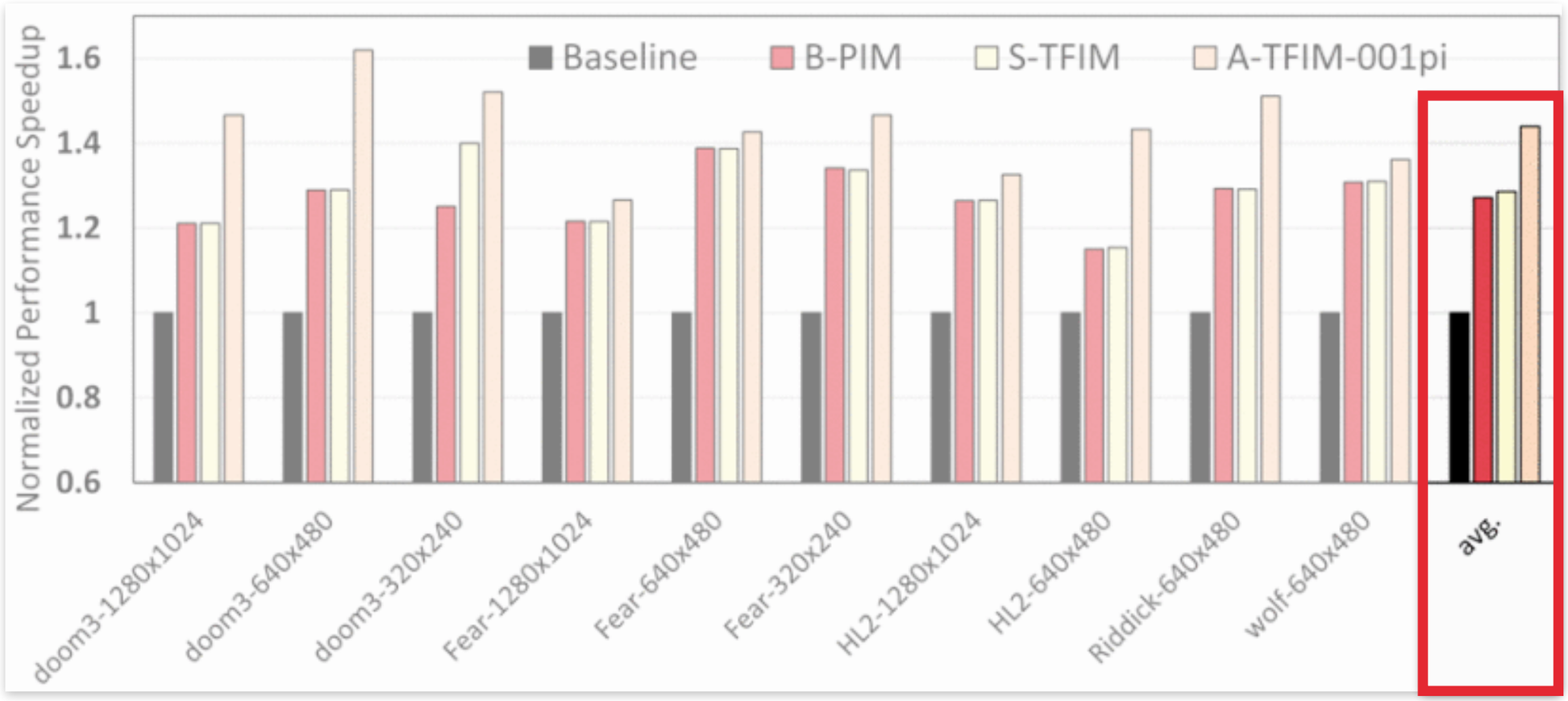

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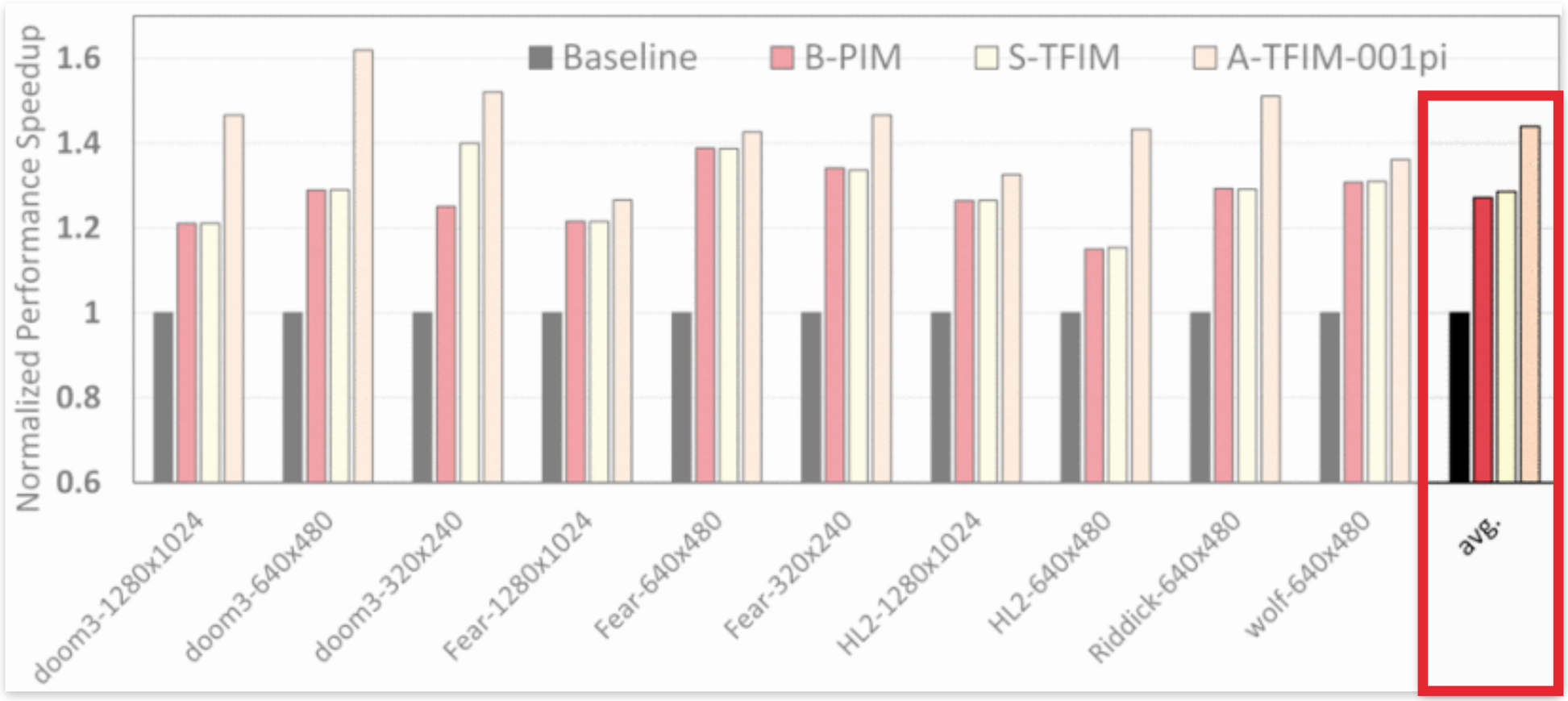


- S-TFIM: Same performance as B-PIM.
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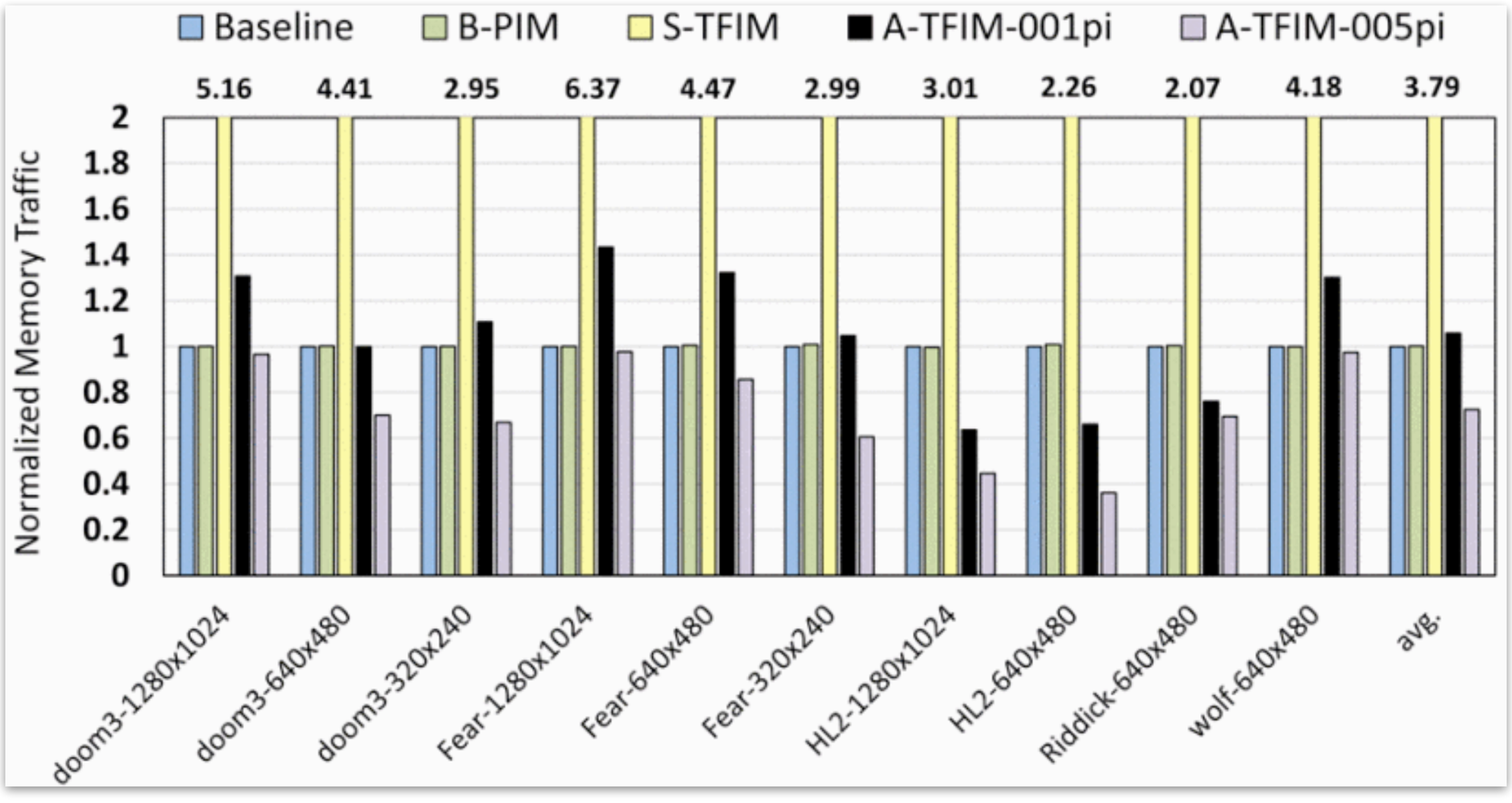

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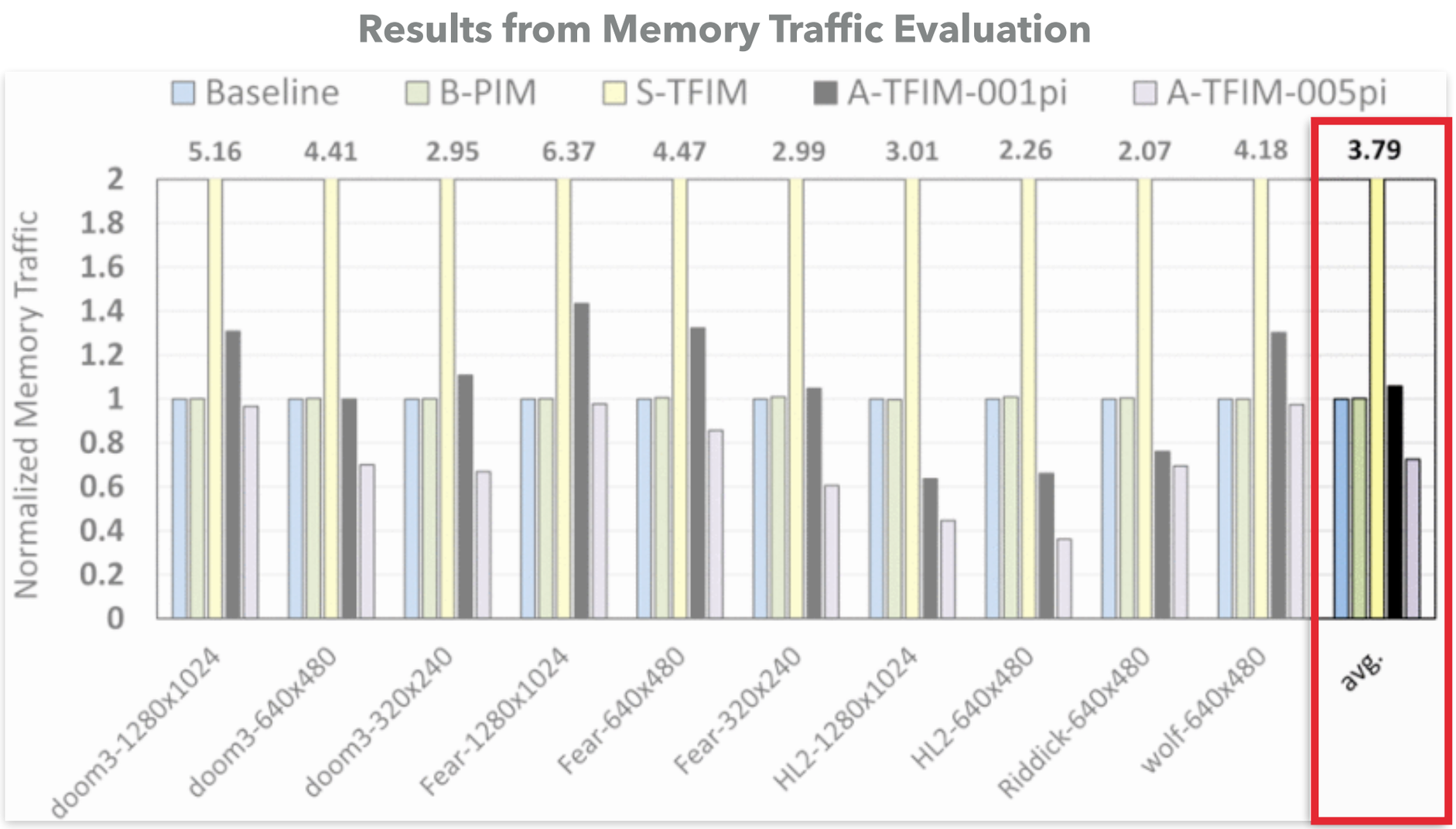

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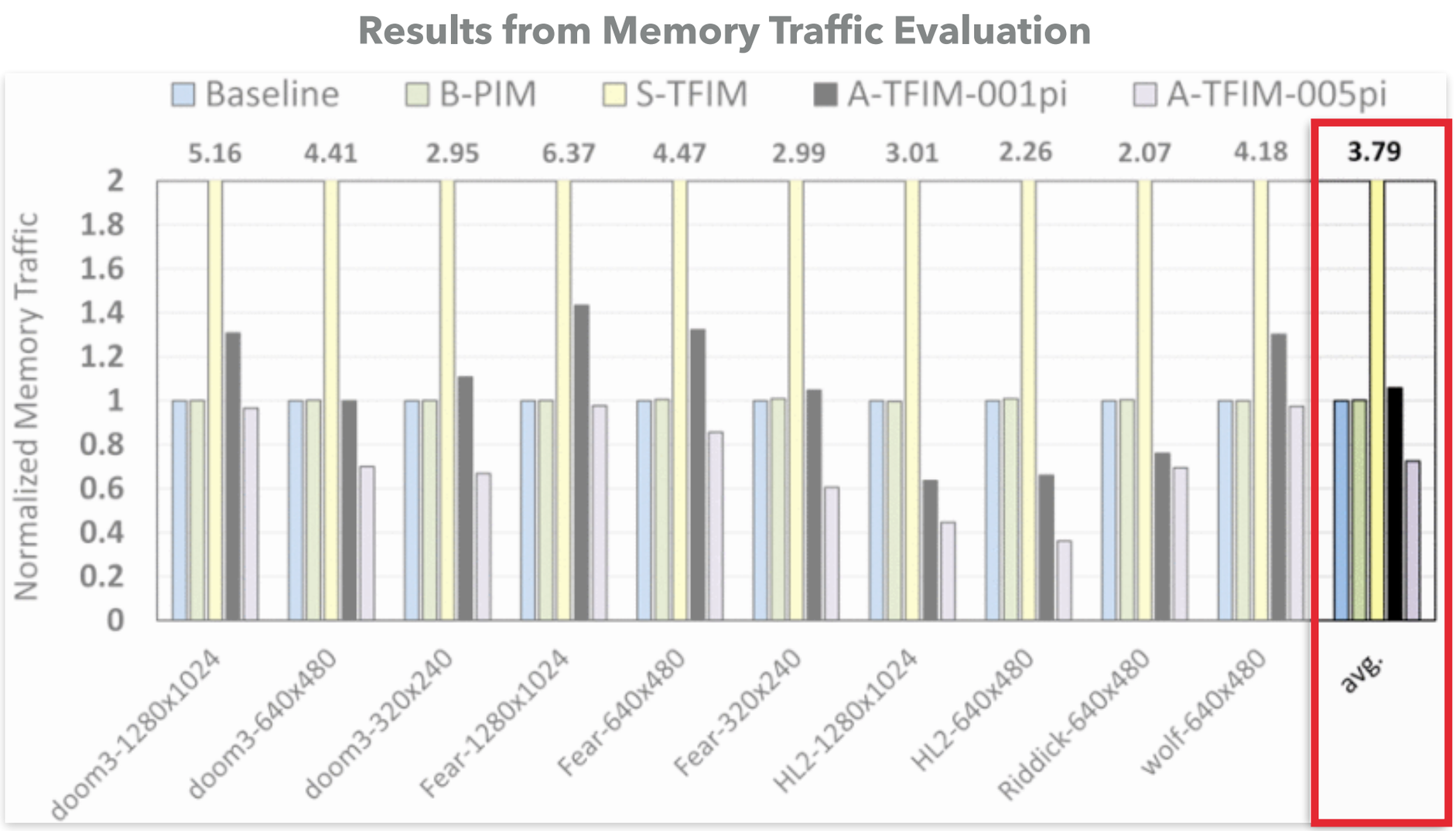


- S-TFIM: Forced re-computation of intermediate texels due to lack of texel-caching in GPU ==> **High memory traffic**.

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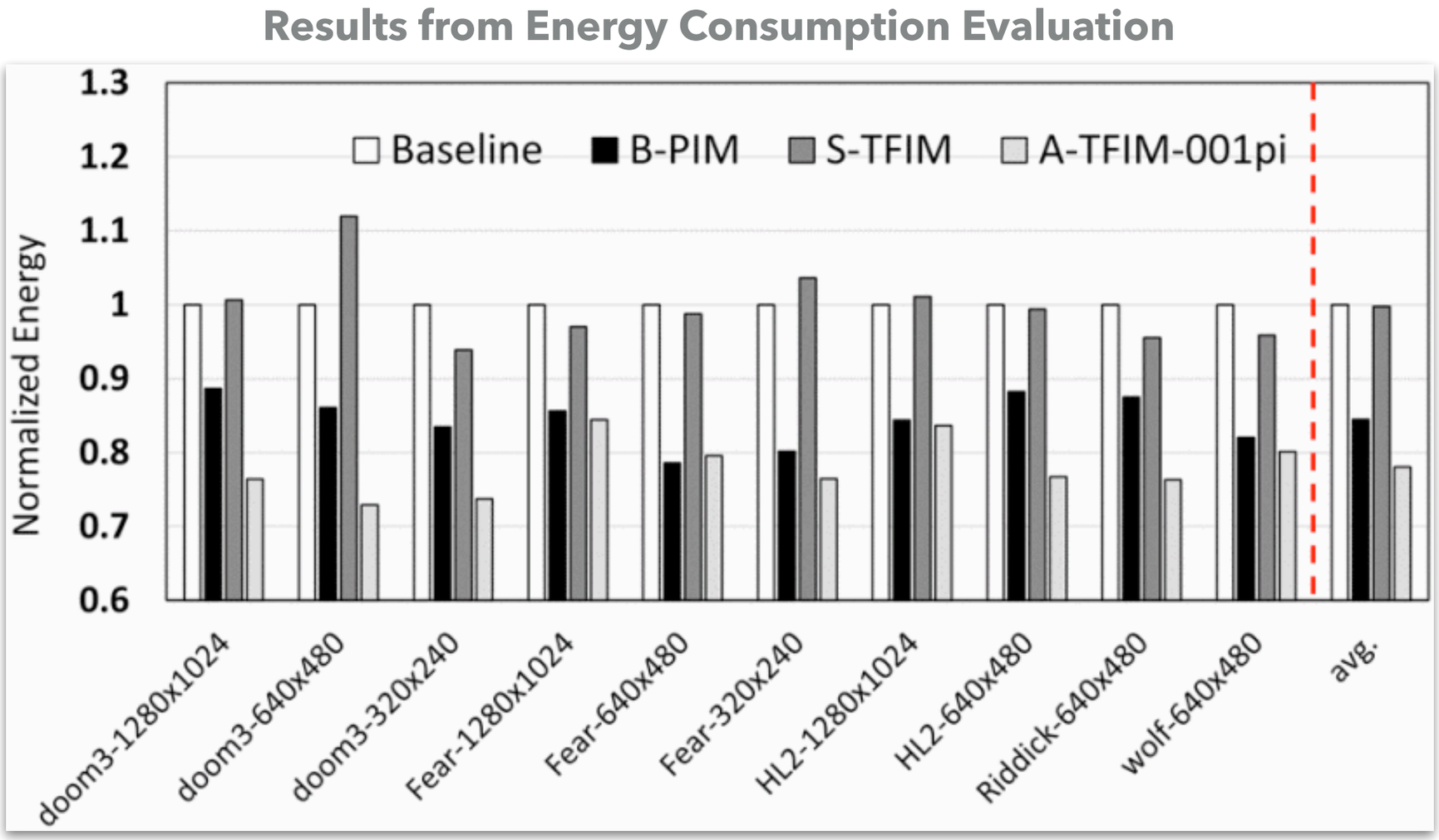

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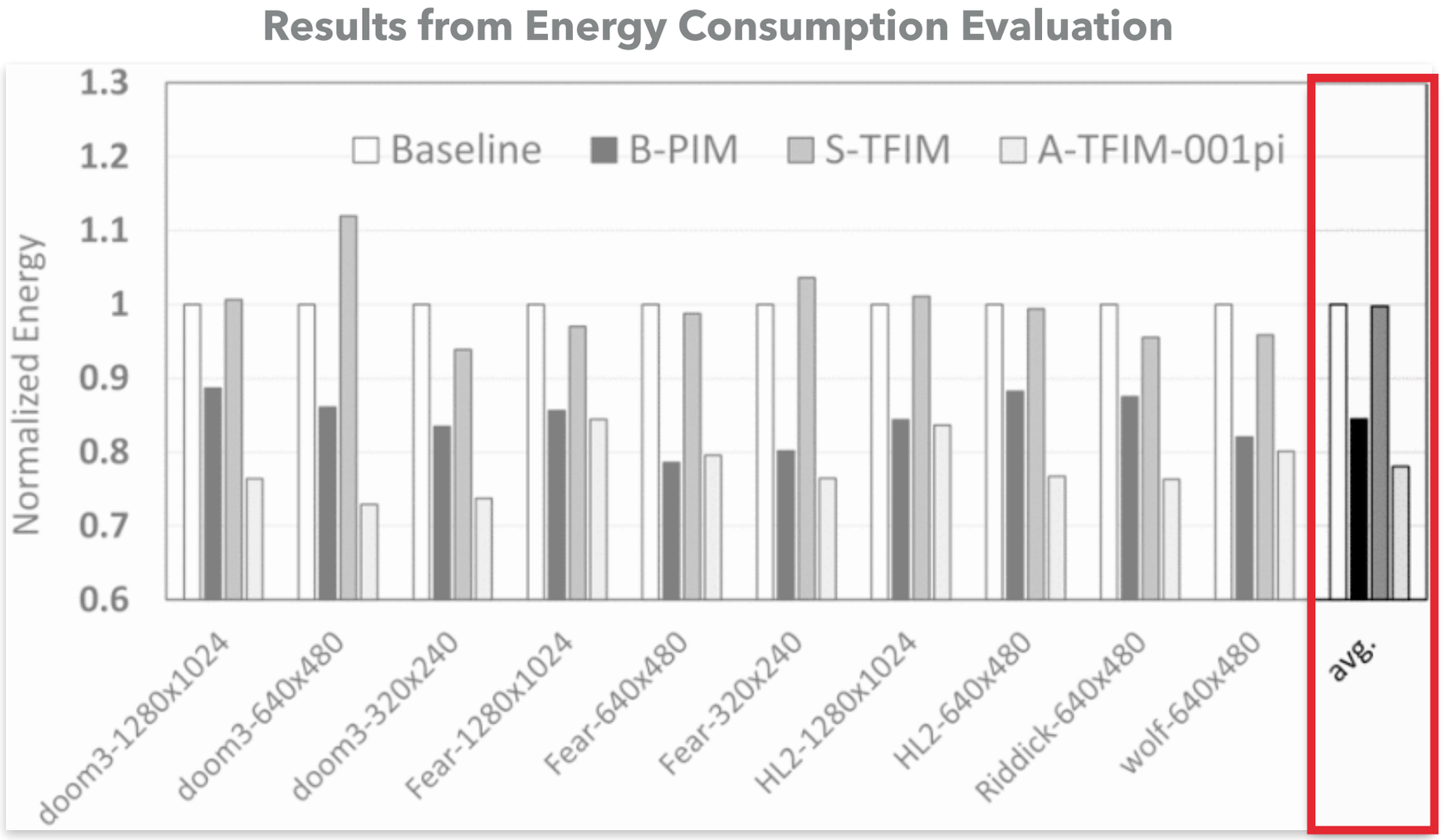

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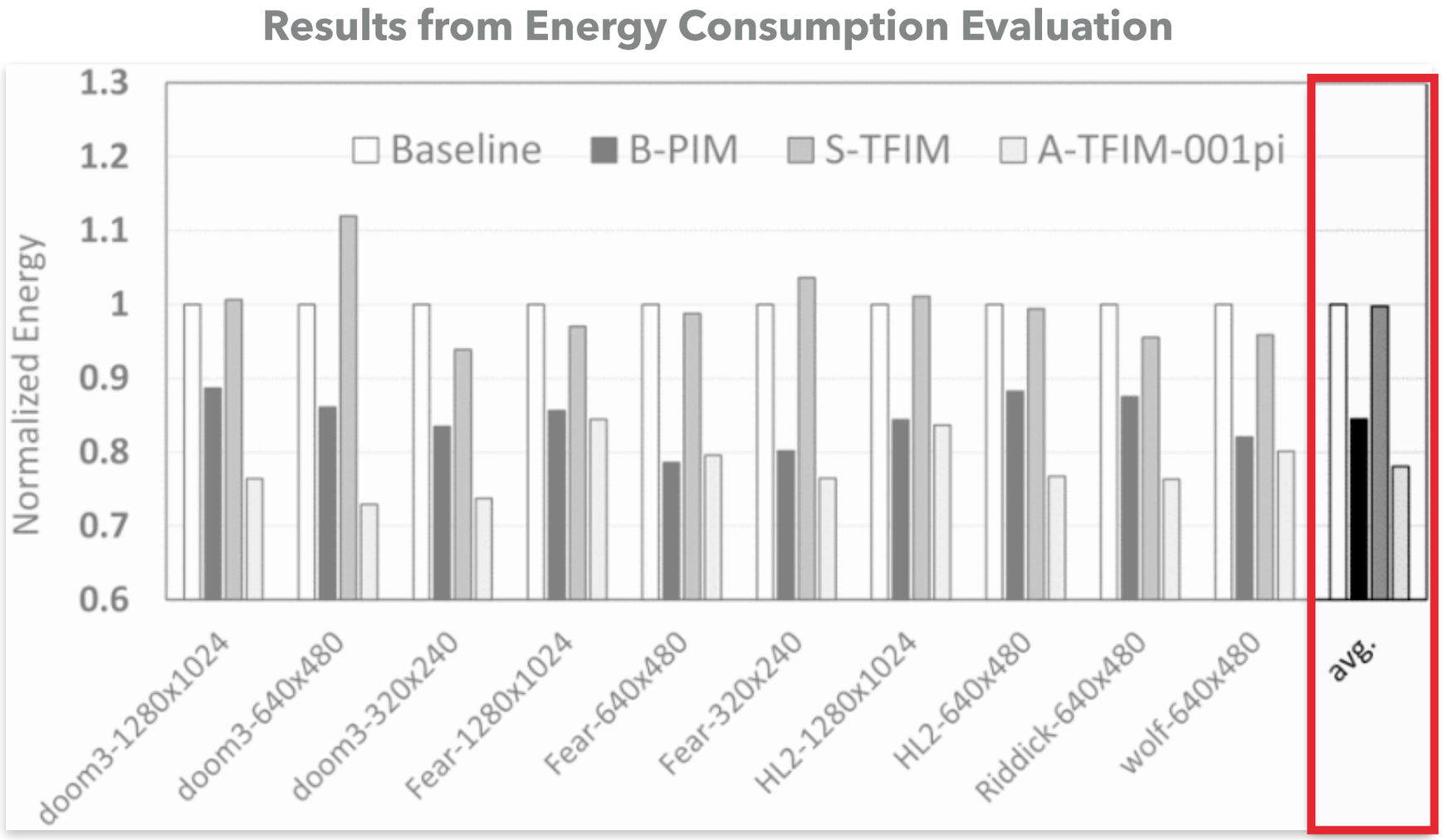


- A-TFIM: Reduces energy consumption by **25%** over baseline GPU.

# RESULTS: QUALITY VS. SPEEDUP FOR A-TFIM ANGLES

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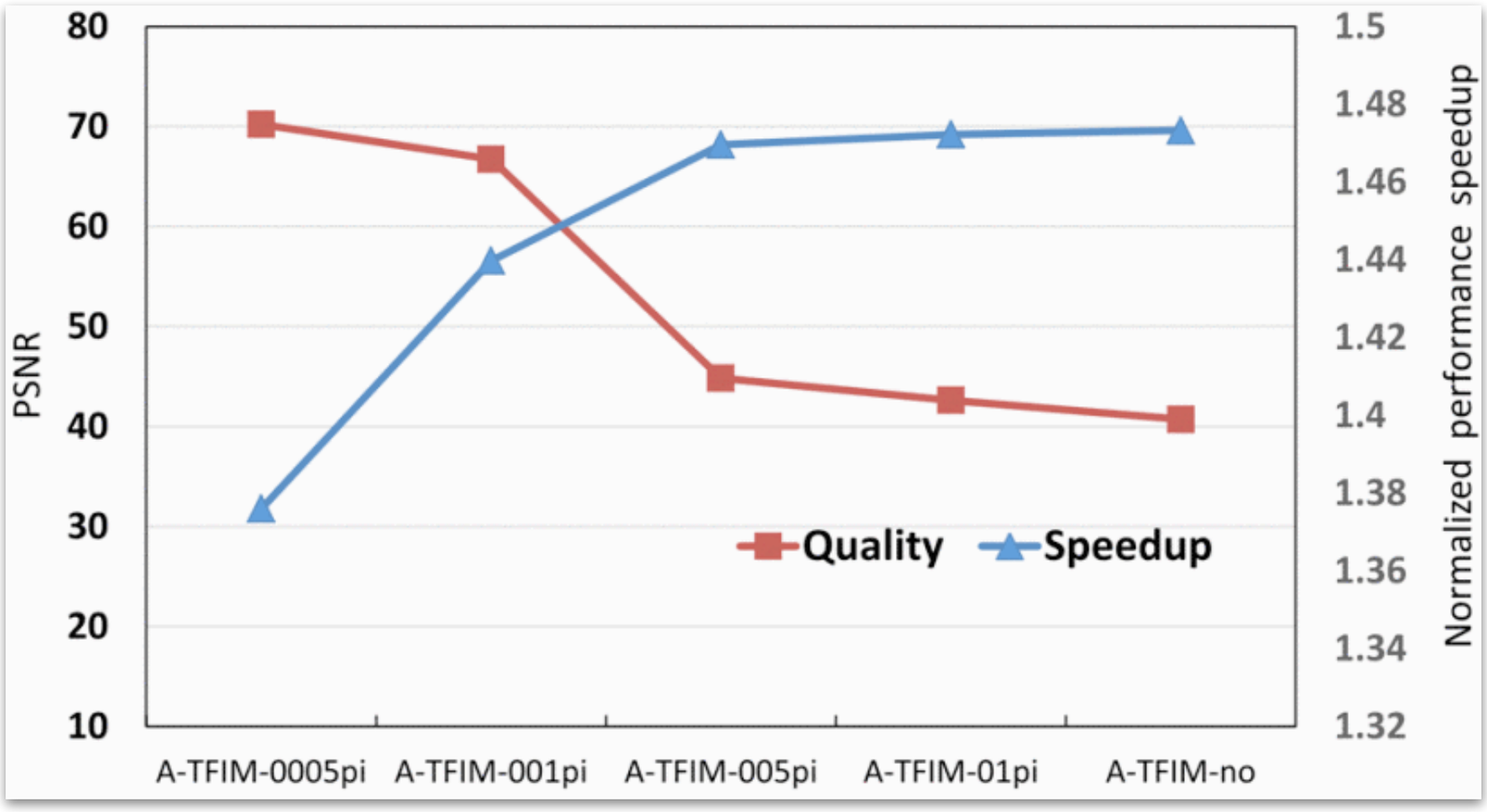

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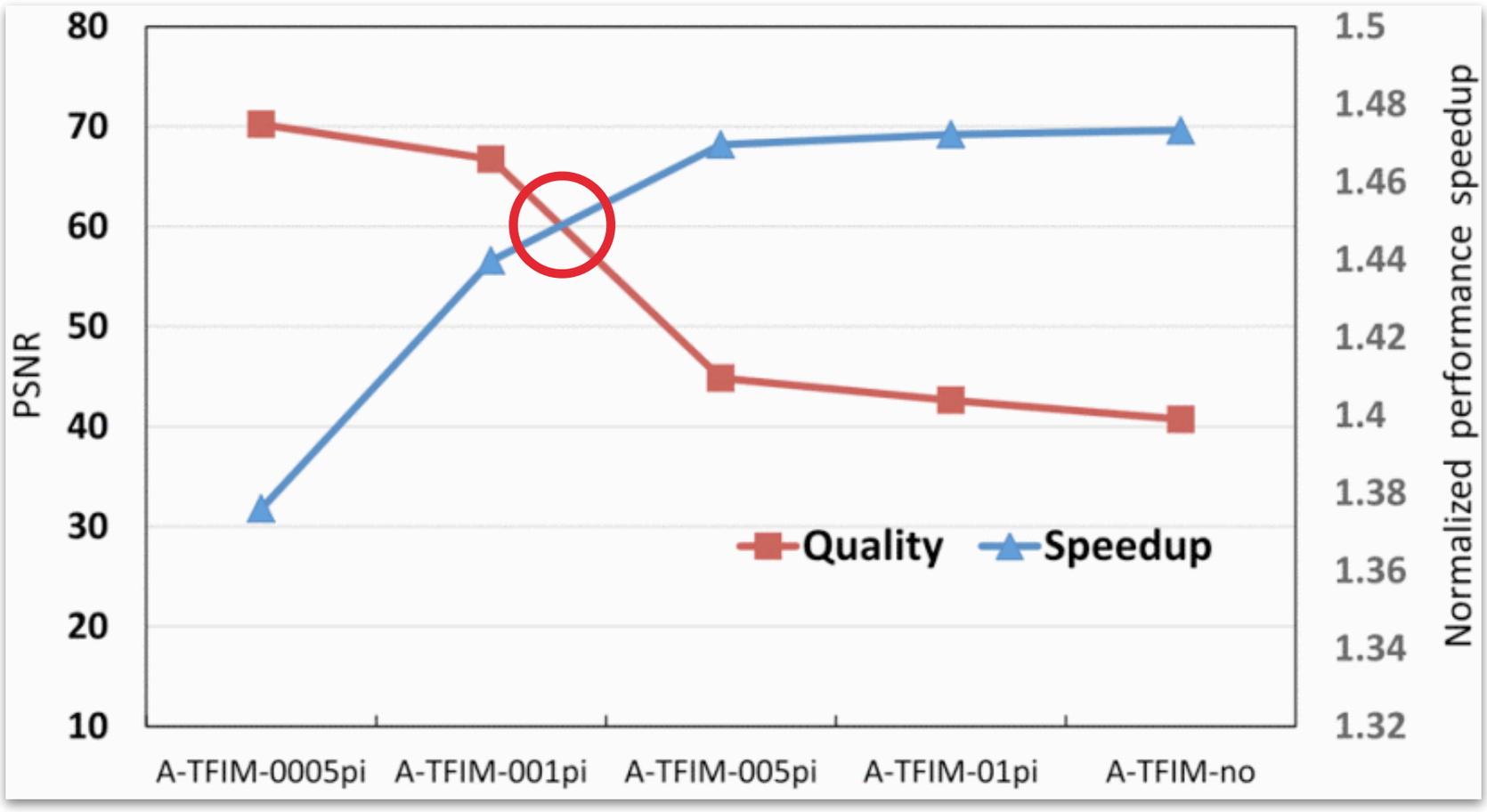

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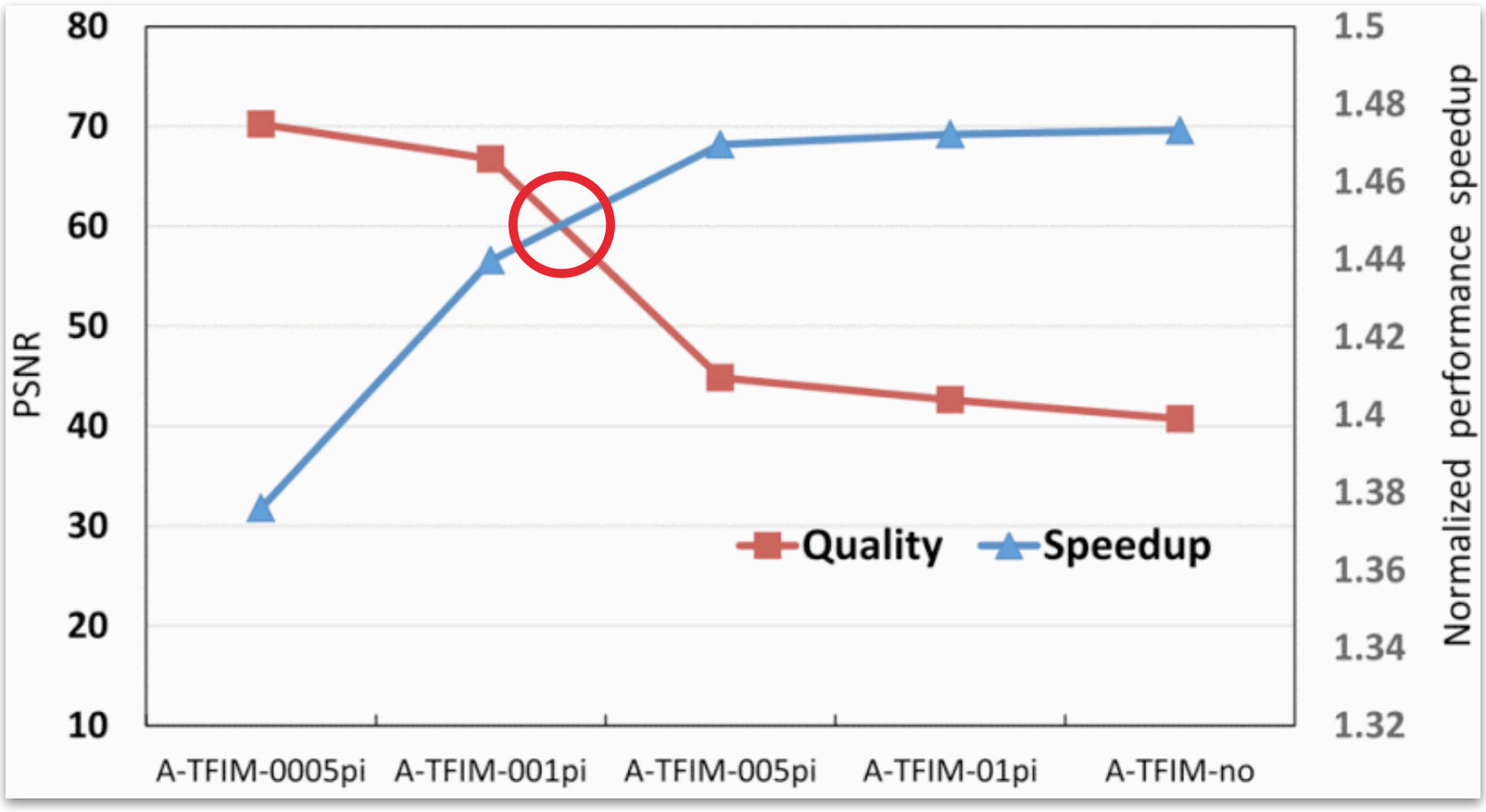


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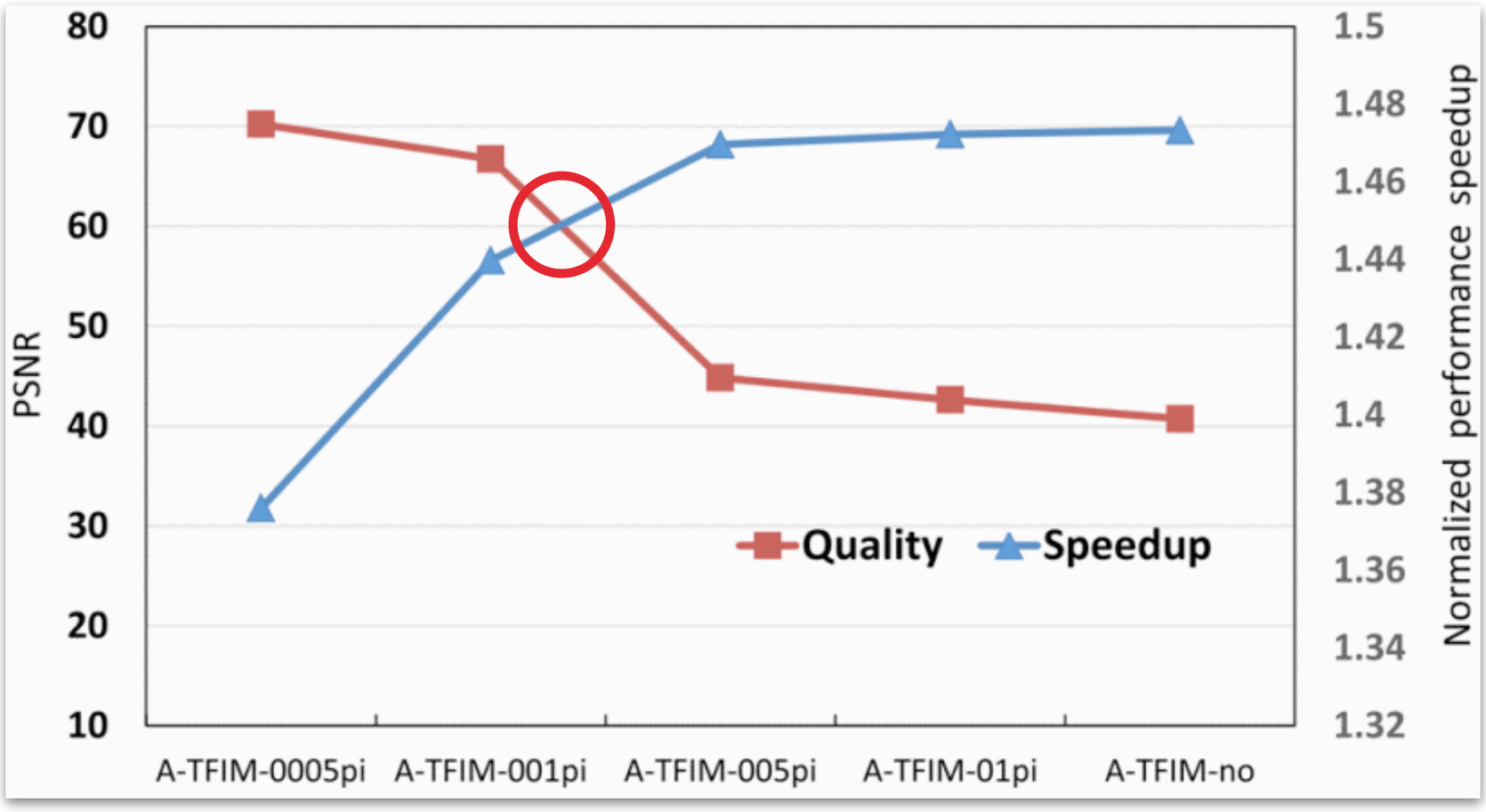


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- Ideal threshold: 0.01pi ≈ 1.8°

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# CONCLUSION

- **Motivation**: Texture filtering = **60%** of **memory requests** in real-time rendering applications.
- **Problem**: Real-time rendering is a highly memory bound task due to texture filtering.
- **Idea**: Bypass memory bottleneck caused by texture filtering by:
  - Using **more** *memory efficient* filtering pipeline.
  - **Reducing** data movement in system.
- **Solution**: Advanced-Texture Filtering In Memory (A-TFIM).
  - Implements a portion of the **texture filtering pipeline** in **HMC**.
  - Uses a **camera-angle threshold** for **performance/accuracy** ratio control.
- **Key results**: Evaluated on various 3D video-games.
  - Average **1.4x** rendering speedup over baseline.
  - Average **22% less** energy consumption compared to baseline.

# QUESTIONS?

# REVIEW

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- Results obtained are impressive in terms of energy efficiency, which would be **great for mobile rendering**.
- The proposed pipeline reordering with low precision loss requires **domain-expertise** from the authors to figure out, showing the authors' investment in the field.

# WEAKNESSES

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- Many different works have tackled this, could lead to **better results** with **simpler implementations** (look at texture compression for example).
- The system was **only tested on games from 20+years ago**, rendering demands have greatly changed since then, how does this perform on modern applications?

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- This work proves that PIM architecture can be used to construct better accelerators for 3D rendering.
- Currently feels like a “proof of concept” and needs to be adapted for modern workloads.

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- **Question: Can these new systems benefit from using PIM architectures?**

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- Most of the work in PIM architectures is in isolating these parts from the entire application.
- **Question: How to decide when/what to offload to PIM systems? Can this be automated? Is a cache miss always the best decision metric?**

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- Modern rendering applications struggle more with **unpredictable memory latencies** from geometry fetches rather than textures.
- **<u>Question</u>: Can we leverage PIM architectures for handling unpredictable memory latencies?**

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- Big thanks to my mentors:
  - Geraldo De Oliveira
  - Mohammad Sadrosadati
  - Haocong Luo
- For all of their feedback throughout the (many) iterations of this presentation.

# LET'S DISCUSS

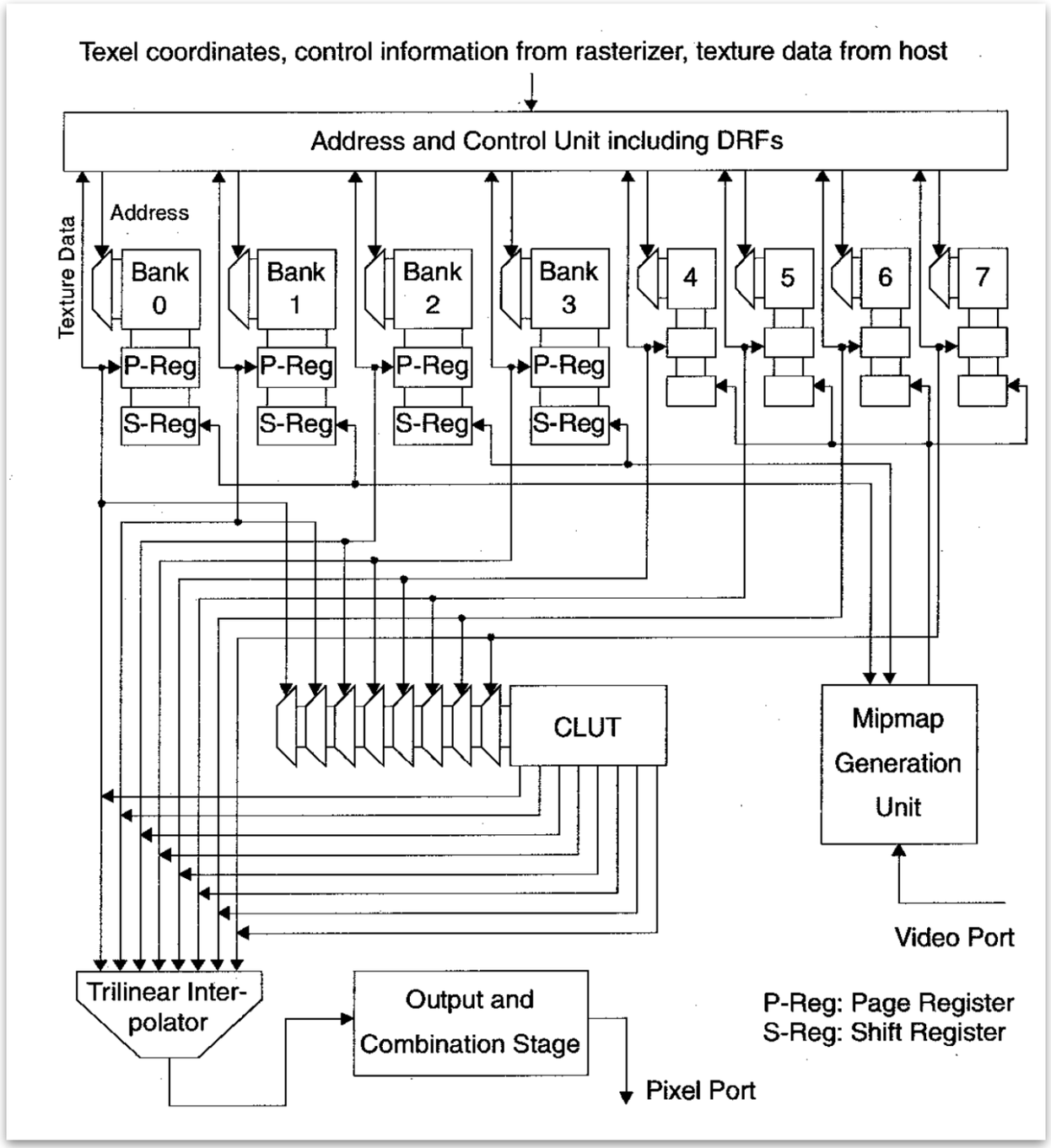
# PRIOR WORK: TEXRAM, A SMART MEMORY FOR TEXTURING

**Texram chip:**

Separate chip with its own memory capable of generating Mipmaps and performing Bilinear and Trilinear filtering.

**Reference:**

*Andreas Schilling, Gunter Knittel, and Wolfgang Strasser - IEEE Computer Graphics and Applications 1996*



# FOLLOW-UP WORK: PIM-VR

- **Idea**: Reduce head movement response delay in Virtual Reality systems by accelerating Asynchronous Time Warp (ATW) using a PIM architecture.
- **Reference**: (Same authors as this work) *"PIM-VR: Erasing Motion Anomalies In Highly-Interactive Virtual Reality World With Customized Memory Cube" - HPCA 2019*