Functionally-Complete Boolean Logic in Real DRAM Chips
Experimental Characterization and Analysis

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Yahya C. Tugrul  Ataberk Olgun  F. Nisa Bostancı
A. Giray Yağlıkçı  Geraldo F. Oliveira  Haocong Luo
Juan Gómez–Luna  Mohammad Sadr  Onur Mutlu

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Executive Summary

- **Motivation:** Processing using DRAM can alleviate the performance and energy bottlenecks caused by data movement
  - Prior works show that existing DRAM chips can perform three-input majority and two-input AND and OR operations
- **Problem:** Proof-of-concept demonstrations on commercial off-the-shelf (COTS) DRAM chips do not provide
  - functionally-complete operations (e.g., NAND or NOR)
  - NOT operation
  - AND and OR operations with more than two inputs
- **Experimental Study:** 256 DDR4 chips from two major manufacturers
- **Key Results:**
  - COTS DRAM chips can perform NOT and {2, 4, 8, 16}-input AND, NAND, OR, and NOR operations with very high reliability (>94% success rate)
  - Data pattern and temperature only slightly affect the reliability of these operations (<1.98% decrease in success rate)
Outline

Background

Goal & Overview

Experimental Methodology

Multiple-Row Activation in Neighboring Subarrays

NOT Operation

AND, NAND, OR, and NOR Operations

Conclusion
DRAM Organization

DRAM Module

DRAM Chip

Chip I/O

Bank

DRAM Chip

DRAM Bank

Sense Amplifiers

Subarray

DRAM Row

Wordline

Sense Amps.

Bitline

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DRAM Open Bitline Architecture

[Diagram showing the architecture of DRAM Open with subarrays and sense amplifiers, connected to bitlines.]
DRAM Open Bitline Architecture

- DRAM Bank
- Subarray
- SA

Activated

Not Activated

Serves as the reference for the SA

NOT Gate

bitline
DRAM Operation

**DRAM Subarray**

1. **ACTIVATE (ACT):** Fetch the row’s content into the sense amplifiers

2. **Column Access (RD/WR):** Read/Write the target column and drive to I/O

3. **PRECHARGE (PRE):** Prepare the subarray for a new ACTIVATE
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Our Goal

Understand the **capability** of COTS DRAM chips beyond just storing data

Rigorously **characterize** the **reliability** of this capability
We demonstrate that COTS DRAM chips:

1. Can simultaneously activate up to 48 rows in two neighboring subarrays.

2. Can perform NOT operation with up to 32 output operands.

3. Can perform up to 16-input AND, NAND, OR, and NOR operations.
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DRAM Testing Infrastructure

• Developed from DRAM Bender [Olgun+, TCAD’23]*

• Fine-grained control over DRAM commands, timings, and temperature

## DRAM Chips Tested

- 256 DDR4 chips from **two major DRAM manufacturers**
- Covers **different die revisions and chip densities**

### DRAM Chips Tested

<table>
<thead>
<tr>
<th>Chip Mfr.</th>
<th>#Modules (#Chips)</th>
<th>Die Rev.</th>
<th>Mfr. Date&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Chip Density</th>
<th>Chip Org.</th>
<th>Speed Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>SK Hynix</td>
<td>9 (72)</td>
<td>M</td>
<td>N/A</td>
<td>4Gb</td>
<td>x8</td>
<td>2666MT/s</td>
</tr>
<tr>
<td></td>
<td>5 (40)</td>
<td>A</td>
<td>N/A</td>
<td>4Gb</td>
<td>x8</td>
<td>2133MT/s</td>
</tr>
<tr>
<td></td>
<td>1 (16)</td>
<td>A</td>
<td>N/A</td>
<td>8Gb</td>
<td>x8</td>
<td>2666MT/s</td>
</tr>
<tr>
<td></td>
<td>1 (32)</td>
<td>A</td>
<td>18-14</td>
<td>4Gb</td>
<td>x4</td>
<td>2400MT/s</td>
</tr>
<tr>
<td></td>
<td>1 (32)</td>
<td>A</td>
<td>16-49</td>
<td>8Gb</td>
<td>x4</td>
<td>2400MT/s</td>
</tr>
<tr>
<td></td>
<td>1 (32)</td>
<td>M</td>
<td>16-22</td>
<td>8Gb</td>
<td>x4</td>
<td>2666MT/s</td>
</tr>
<tr>
<td>Samsung</td>
<td>1 (8)</td>
<td>F</td>
<td>21-02</td>
<td>4Gb</td>
<td>x8</td>
<td>2666MT/s</td>
</tr>
<tr>
<td></td>
<td>2 (16)</td>
<td>D</td>
<td>21-10</td>
<td>8Gb</td>
<td>x8</td>
<td>2133MT/s</td>
</tr>
<tr>
<td></td>
<td>1 (8)</td>
<td>A</td>
<td>22-12</td>
<td>8Gb</td>
<td>x8</td>
<td>3200MT/s</td>
</tr>
</tbody>
</table>
Testing Methodology

- Carefully sweep:
  - Row addresses: Row A and Row B
  - Timing parameters: Between ACT → PRE and PRE → ACT
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NOT Operation

AND, NAND, OR, and NOR Operations

Conclusion
The Capability of COTS DRAM Chips

We demonstrate that COTS DRAM chips:

1. Can simultaneously activate up to 48 rows in two neighboring subarrays

2. Can perform NOT operation with up to 32 output operands

3. Can perform up to 16-input AND, NAND, OR, and NOR operations
Key Observation

Activating two rows in quick succession can simultaneously activate multiple rows in neighboring subarrays.

- **ACT Row A**
  - 3ns
  - <3ns

- **PRE**
  - 14ns
  - <3ns

- **ACT Row B**
Characterization Methodology

- To understand which and how many rows are simultaneously activated
  - **Sweep** Row A and Row B addresses

All rows in Subarray X

All rows in Subarray Y

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COTS DRAM chips have **two distinct** sets of activation patterns in **neighboring subarrays** when two rows are activated with **violated timings**

- **Exactly the same number** of rows in each subarray are activated
- **Twice as many** rows in one subarray compared to its neighbor subarray are activated

<table>
<thead>
<tr>
<th>Subarray X</th>
<th>Up to 16 rows</th>
<th>Shared Sense Amplifiers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Subarray Y</td>
<td>Up to 16 rows</td>
<td></td>
</tr>
</tbody>
</table>

A total of **32 rows**

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<tr>
<th>Subarray X</th>
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<tbody>
<tr>
<td>Subarray Y</td>
<td>Up to 32 rows</td>
<td></td>
</tr>
</tbody>
</table>

A total of **48 rows**
COTS DRAM chips can simultaneously activate up to 48 rows in two neighboring subarrays.

(More results in the paper)

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We demonstrate that COTS DRAM chips:

1. Can simultaneously activate up to 48 rows in two neighboring subarrays

2. Can perform **NOT operation** with **up to 32** output operands

3. Can perform **up to 16-input AND, NAND, OR, and NOR** operations
Key Idea

Connect rows in neighboring subarrays through a NOT gate by simultaneously activating rows.
NOT Operation: A Walkthrough

ACT src

connects src to bitline
NOT Operation: A Walkthrough

ACT src
Nominal

GND
src
GND

drives bitline to GND

VDD
dst
GND

drives bitline to VDD
NOT Operation: A Walkthrough

- **ACT src** to **PRE**: Nominal transition in <3ns.
- **ACT dst**: The sense amplifier is still enabled.
- **src** connects **dst** to the bitline.
- **dst**'s bitline is still VDD.

**Diagram Notes**:
- GND
- VDD
- connect dst to bitline
- sense amplifier is still enabled
NOT Operation: A Walkthrough

ACT src → PRE → ACT dst

Nominal → <3ns

GND

src → VDD

negated value of src (VDD) is written to dst

dst

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Characterization Methodology

• Sweep **Row A and Row B addresses**

• Sweep **DRAM chip temperature**

- All rows in Subarray X
- All rows in Subarray Y

ACT Row A ➔ PRE ➔ ACT Row B

Nominal <3ns

Temperature

50°C ➔ 95°C
Reliability Metric

**Success Rate** (for a DRAM cell)

Percentage of trials where the **correct output** of a tested operation is stored in the cell

Total of 10000 trials

Success rate for this cell: 50%
# Key Takeaways from In-DRAM NOT Operation

<table>
<thead>
<tr>
<th>Key Takeaway 1</th>
</tr>
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<tbody>
<tr>
<td><strong>COTS DRAM chips can perform NOT operations with up to 32 destination rows</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Key Takeaway 2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature has a small effect on the reliability of NOT operations</strong></td>
</tr>
</tbody>
</table>
Performing NOT in COTS DRAM Chips

There is at least one DRAM cell that can perform the NOT operation with a 100% success rate.

COTS DRAM chips can perform NOT operations with up to 32 destination rows.
**Impact of Temperature**

- Used **destination cells** that can perform NOT operation with >90% success rate at 50°C

---

**Temperature has a small effect on the reliability of NOT operations**

- From 50°C to 95°C only 0.2% variation in average success rate
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We demonstrate that COTS DRAM chips:

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Key Idea

Manipulate the bitline voltage to express a wide variety of functions using multiple-row activation in neighboring subarrays.

![Diagram showing multiple-row activation](image)

- sense amp. compares $V_{(A,B)}$ and $V_{(X,Y)}$
- Multiple Row ACT
Two-Input AND and NAND Operations

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Two-Input AND and NAND Operations

\[ \text{V}_{\text{DD}} = 1 \, \& \, \text{GND} = 0 \]

- \( \text{ACT} \) and \( \text{PRE} \) operations are separated by less than 3ns.

- The sense amp. compares the voltages on the bitlines.

- \( \text{REF} \) is set to 1.

- \( \text{V}_{\text{DD}}/4 \) is used for the voltage levels.
Two-Input AND and NAND Operations

V_{DD} = 1 & GND = 0

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>COM</th>
<th>REF</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

sense amp. compares the voltages on the bitlines

V_{DD}/2

3V_{DD}/4
Two-Input AND and NAND Operations

V\text{DD}=1 \& \text{GND} = 0

\begin{array}{|c|c|c|c|c|}
\hline
X & Y & COM & REF \\
\hline
0 & 0 & 0 & 1 \\
0 & 1 & 0 & 1 \\
1 & 0 & 0 & 1 \\
\hline
\end{array}

\text{sense amp. compares the voltages on the bitlines}

V\text{DD}/2 \rightarrow 3V\text{DD}/4
Two-Input AND and NAND Operations

V_{DD} = 1 & GND = 0

<table>
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</tr>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
Two-Input AND and NAND Operations

\[
V_{DD} = 1 \quad \text{GND} = 0
\]

Reference Subarray (REF)

Compute Subarray (COM)

\[
\text{AVG}(V_{DD}, V_{DD}/2)
\]

\[
\text{AVG}(X, Y)
\]

\[
V_{DD} = 1 \quad \text{GND} = 0
\]

\[
\begin{array}{cccc}
X & Y & \text{COM} & \text{REF} \\
0 & 0 & 0 & 1 \\
0 & 1 & 0 & 1 \\
1 & 0 & 0 & 1 \\
1 & 1 & 1 & 0 \\
\end{array}
\]

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Many-Input AND, NAND, OR, and NOR Operations

We can express **AND, NAND, OR, and NOR operations** by carefully manipulating the **reference voltage**

Functionally-Complete Boolean Logic in Real DRAM Chips: Experimental Characterization and Analysis

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(Max details in the paper)

Characterization Methodology

- **Sweep** Row A and Row B addresses

![Diagram showing ACT, PRE, and ACT processes for Subarrays X and Y with Row A and Row B addresses.]
**Key Takeaways from In-DRAM Operations**

<table>
<thead>
<tr>
<th>Key Takeaway 1</th>
<th>COTS DRAM chips can perform {2, 4, 8, 16}-input AND, NAND, OR, and NOR operations</th>
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<tr>
<td>Key Takeaway 2</td>
<td>COTS DRAM chips can perform AND, NAND, OR, and NOR operations with very high reliability</td>
</tr>
<tr>
<td>Key Takeaway 3</td>
<td>Data pattern slightly affects the reliability of AND, NAND, OR, and NOR operations</td>
</tr>
</tbody>
</table>
Performing AND, NAND, OR, and NOR

COTS DRAM chips can perform \{2, 4, 8, 16\}-input AND, NAND, OR, and NOR operations
Performing AND, NAND, OR, and NOR

COTS DRAM chips can perform 16-input AND, NAND, OR, and NOR operations with very high success rate (>94%)
Impact of Data Pattern

1.98% variation in average success rate across all number of input operands
Impact of data pattern is consistent across all tested operations
Impact of Data Pattern

Data pattern slightly affects the reliability of AND, NAND, OR, and NOR operations.
More in the Paper

• Detailed hypotheses & key ideas to perform
  – NOT operation
  – Many-input AND, NAND, OR, and NOR operations

• How the reliability of bitwise operations are affected by
  – The location of activated rows
  – Temperature (for AND, NAND, OR, and NOR)
  – DRAM speed rate
  – Chip density and die revision

• Discussion on the limitations of COTS DRAM chips
Functionally-Complete Boolean Logic in Real DRAM Chips: Experimental Characterization and Analysis

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Processing-using-DRAM (PuD) is an emerging paradigm that leverages the analog operational properties of DRAM circuitry to enable massively parallel in-DRAM computation. PuD has the potential to significantly reduce or eliminate costly data movement between processing elements and main memory. A common approach for PuD architectures is to make use of bulk bitwise computation (e.g., AND, OR, NOT). Prior works experimentally demonstrate three-input MAJ (i.e., MAJ3) and two-input AND and OR operations in commercial off-the-shelf (COTS) DRAM chips. Yet, demonstrations on COTS DRAM chips do not provide a functionally complete set of operations (e.g., NAND or AND and NOT).

We experimentally demonstrate that COTS DRAM chips are capable of performing 1) functionally-complete Boolean operations: NOT, NAND, and NOR and 2) many-input (i.e., more than two-input) AND and OR operations. We present an extensive systems and applications [12, 13]. Processing-using-DRAM (PuD) [29–32] is a promising paradigm that can alleviate the data movement bottleneck. PuD uses the analog operational properties of the DRAM circuitry to enable massively parallel in-DRAM computation. Many prior works [29–53] demonstrate that PuD can greatly reduce or eliminate data movement.

A widely used approach for PuD is to perform bulk bitwise operations, i.e., bitwise operations on large bit vectors. To perform bulk bitwise operations using DRAM, prior works propose modifications to the DRAM circuitry [29–31, 33, 35, 36, 43, 44, 46, 48–58]. Recent works [38, 41, 42, 45] experimentally demonstrate the feasibility of executing data copy & initialization [42, 45], i.e., the RowClone operation [49], and a subset of bitwise operations, i.e., three-input bitwise majority (MAJ3) and two-input AND and OR operations in unmodified commercial off-the-shelf (COTS) DRAM chips by operating beyond

Source code is available on GitHub

https://github.com/CMU-SAFARI/FCDRAM
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- We experimentally demonstrate that commercial off-the-shelf (COTS) DRAM chips can perform:
  - **Functionally-complete** Boolean operations: NOT, NAND, and NOR
  - **Up to 16-input** AND, NAND, OR, and NOR operations
- We characterize **the success rate** of these operations on 256 COTS DDR4 chips from two major manufacturers
- We highlight **two key results**:
  - We can perform **NOT** and  
    \{2, 4, 8, 16\}-input AND, NAND, OR, and NOR operations  
    on COTS DRAM chips with **very high success rates** (>94%)
  - **Data pattern** and **temperature** only slightly affect  
    the reliability of these operations

We believe these empirical results demonstrate  
the promising potential of using DRAM as a computation substrate
Functionally-Complete Boolean Logic in Real DRAM Chips
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Functionally-Complete Boolean Logic in Real DRAM Chips
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DISCUSSION

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Strengths

• The first demonstration of NOT, NAND, NOR operations and more than two-input AND and OR operations in real DRAM chips
  – A total of 256 DDR4 DRAM chips from 18 DRAM modules

• A rigorous reliability characterization of these operations under various parameters
  – E.g., spatial variation, data pattern, and temperature

• Source code available online
  – Can be tested, extended and improved
Weaknesses - I

- Computation can be done on only half of the rows due to open-bitline architecture
Weaknesses - II

• Output of NOT-based operations (i.e., NOT, NAND, and NOR) are in the neighboring subarray
  – Further computation on input and the output requires data relocation

• Example: XOR(A, B) = A'B + AB'
  – Assume you have A and B
    • 1) Perform NOT operation for A and B
    • 2) \{A', B'\} and \{A, B\} are in the neighboring subarrays!
      – There is no inter-subarray row copy operation
Weaknesses – III (Potpourri)

• No evaluation on how applications would benefit from the new in-DRAM operations

• No discussion/evaluation on how to integrate these operations into a system

• How voltage would affect the in-DRAM operations’ reliability is not analyzed

• Only DDR4 chips are evaluated;
  – No HBM and DDR5 chips
How can we utilize all cells in row to perform in-DRAM operations?

- Leveraging the connection between three neighboring subarrays
- Assume three consecutive subarrays:
  - Half of the rows in the middle subarray are connected to the top subarray
  - Other half of the rows in the middle subarray are connected to the bottom subarray
- We can divide the data into two parts and store them into the top and bottom subarrays
Discussion - II

• Is there a way to solve the data relocation problem?
  – Can we perform computations on output of NOT-based operations and input data without data relocation (or with lower overhead)?

• One simple solution:
  – Store A and B in the neighboring subarray
  – Increases the latency
    • i.e., 2x more write operation
  – Eliminates the reading back the output and write it to the other subarray where A and B are stored
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Experimental Methodology

We test all banks in each DRAM chip

We test three neighboring subarray pairs in each bank

We test all possible combinations of activated rows
Performing NOT in COTS DRAM Chips

As the number of destination rows increases, more DRAM cells produce incorrect results.

The average success of the NOT operation with
- four destination row: 98.37%
- thirty-two destination rows: 7.95%
The Coverage of Multiple-Row Activation

Figure 5: Coverage of each $N_{RF}:N_{RL}$ activation type across tested $R_F$ and $R_L$ row pairs.
NOT vs. Activation Trend

Figure 8: Success rate of the NOT operation vs. $N_{RF}:N_{RL}$ activation type.
Impact of Location in NOT Op.

- Categorize the distance between activated rows (source and destination rows) and the sense amplifiers into three regions: Far, Middle, and Close.

The distance between activated rows and the sense amplifiers significantly affects the reliability.
The effect of DRAM Speed Rate on NOT

Figure 11: Success rate of the NOT operation for different DRAM speed rates.
Figure 12: Success rate of the NOT operation for different chip density and die revision combinations for two major manufacturers.
Performing AND, NAND, OR, and NOR

The reliability distributions are very similar between
1) AND-NAND and 2) OR – NOR operations.
Impact of Temperature

Temperature has a small effect on the reliability of AND, NAND, OR, and NOR operations.
Boolean Operations vs. Number of 1s

Figure 16: Success rates of AND and OR operations based on the number of logic-1s in the input operands.
The Effect of the Location

(a) AND

(b) NAND

(c) OR

(d) NOR
Figure 20: Success rates of AND, NAND, OR, and NOR operations for three DRAM speed rates.
Chip Density & Die Revision vs. Bitwise Ops.

The diagram illustrates the success rate (%) of different operations (AND, NAND, OR, NOR) with varying numbers of input operands (2, 4, 8, 16). The success rate is depicted across different die revisions (4Gb A-die, 4Gb M-die, 8Gb A-die, 8Gb M-die). The data points and error bars indicate the variability in success rates for each combination of operation and number of operands.
DRAM Cell Operation

1. ACTIVATE (ACT)
2. PRECHARGE (PRE)

- Wordline
- Bitline
- Capacitor
- Access Transistor
- Enable
- NOT Gate
DRAM Cell Operation - ACTIVATE

1. **raise wordline**
2. **capacitor**
3. **access transistor**
4. **bitline**
5. **cell loses charge to bitline**

- **1/2 V_{DD} + \delta**
- deviation in bitline voltage
- connects cell to bitline

6. **enable sense amp**

- **1/2 V_{DD}**
- **enable**

7. **cell regains charge to bitline**

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DRAM Cell Operation - PRECHARGE

precharge bitline for next access

lower wordline

wordline

capacitor

access transistor

enable

Disable Sense Amp

1/2 \( V_{DD} \)

1/2 \( V_{DD} \)