LAB 1 – Drawing a Basic Circuit

Goals

- Design a simple combinatorial circuit using schematic entry.

To Do

- You design a 4-bit comparator circuit that accepts two 4-bit binary inputs (A and B) and outputs a logic-1 if both inputs are equal.
- Follow the instructions. Paragraphs that have a gray background like the current paragraph denote descriptions that require you to do something.
- To complete the lab you need to show your results to an assistant. The last pages of this document is formatted as a report that contains some (optional) exercises. You only need to show your work to assistants when instructed in the report. The assistants will note down your work in their internal grading sheet. Other questions are optional.

Introduction

Throughout this course, you will learn to design digital circuits. For later exercises, we will program digital circuits in the Verilog programming language using the Vivado programming suite provided by Xilinx. Vivado allows us to design our circuit, convert our design idea from a description into an actual circuit that can be implemented on the FPGA board (synthesis), allocate resources on the actual FPGA, connect these to implement our circuit (placement and routing) and downloads the final configuration to the FPGA itself (programming).

Most modern designs are described using high-level hardware description languages like Verilog or VHDL (we will use Verilog in the next few weeks). However, in this exercise we will first learn to design simple circuits by drawing them on paper.

The Comparator Circuit

As we have not yet covered how complex circuits can be designed, we start with a fairly simple circuit that we should be able to come up with using a few simple gates. As the name implies, a comparator accepts two values and tells us when the two values are the same. To keep the complexity under control we will use two 4-bit numbers and we will design the circuit so that the output is logic-1 if both 4-bit numbers have the same value, and logic-0 if they differ.

Sketch the circuit schematic of the comparator using basic 2–input logic gates on your report sheet using a pen. Call the 4-bit inputs A and B, and the output EQ. To make things easier consider a two-step approach: First compare A and B bit by bit. And then in the second step, combine the results of the previous step so that EQ is logic-1 only if A and B have the same value.

Show your schematic to an assistant, and if necessary make corrections.

It is always good practice to have a circuit sketch before beginning to work on the computer. In this case, the circuit is very simple, and the advantage of doing so may not be immediately obvious, but trust us, having a diagram of the circuit makes life easier.

Please finish the report by answering some related questions on the report form.

Last Words

Drawing schematics (either by hand or automatically) was the only way to describe circuits before the advent of hardware description languages. For smaller circuits like the one we have designed in this lab, it is not very difficult to draw schematics. For larger circuits however, the amount of work increases significantly.

Digital Circuits Laboratory Exercises

Lab 1: Drawing a Basic Circuit

Date		
Group Number		
Names		

Part 1

Draw the schematic of the comparator.

Part 2

Show your schematic from Part 1 to an assistant to obtain the lab grade.

Part 3

In the lecture it was said that it is possible to realize all boolean functions with only 2-input NAND or 2-input NOR gates. Try re-drawing the schematic with only 2-input NAND gates. Try to use as few gates as possible (no extra points, it will just take you much less time to draw). Hint – use DeMorgan's Theorem to express the combinatorial logic in terms of NAND operations only. It is also acceptable to draw the gates used in Part 1 using NAND gates only.

Part 4a

Assume that we were only using 2-input AND gates and 2-input XNOR gates to create our comparator. How many of each gate would you use for a comparator of size 8, 16, 32 and 64 bits? This will give the area of the circuit. How many gates will the signal propagate through in each case? This will determine the speed of the circuit. Note: the logic depth of a combinational circuit is defined as the number of logic gates in the longest signal path (path from input to output).

Comparator Size	2-input XNOR gates	2-input AND gates	Logic depth
8 bits			
16 bits			
32 bits			
64 bits			

Part 4b

Derive a general expression for the number of 2-input XNOR gates, the number of 2-input AND gates and the logic depth for a comparator of size N.

Part 5

Sketch how you would enhance the circuit from Part 1 to include a second output (OP) which would be logic-1 if all the bits are completely opposite of each other. OP should be logic-1 when, for example, A is 1100 and B is 0011 or A is 1001 and B is 0110.

Part 6

If you have any comments about the exercise please add them here: mistakes in the text, difficulty level of the exercise, anything that will help us improve it for the next time.