| Design of Digital Circuits: Lab Report | | |
|---|---|---|
| **Lab 9: The Performance of MIPS** | | |
| Date | | Grade |
| Names | | |
| | | Lab session / lab room |
| | | |

**You have to submit this report and the required codes via Moodle.**

**Use a zip file or tarball that contains the report and the codes. Only one of the members of each group should submit. All member of the group will get the same grade.**

**The name of the submitted file should be *Lab8_part1_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the family names of the members of the group.**

**Part 1**

For the following values of A and B, how many clock cycles are needed to execute your program from Lab 7? Assuming that we run the MIPS processor at 20 MHz, how much time (in seconds) would that take?

| Value of A | Value of B | Number of cycles | Time in seconds |
|---|---|---|---|
| 0 | 8 | | |
| 6 | 8 | | |
| 0 | 250’000’000 | | |
| 249’999’996 | 250’000’002 | | |

**Part 2**

Fill in the new values for the Table in Part 1 when using the modified MIPS architecture running the optimized code.

| Value of A | Value of B | Number of cycles | Time in seconds |
|---|---|---|---|
| 0 | 8 | | |
| 6 | 8 | | |
| 0 | 250’000’000 | | |
| 249’999’996 | 250’000’002 | | |

**Part 3**

Compare the size/device utilization of the two implementations (before and after the modifications). What differences do you see? Briefly comment on them. *Hint: Look into the synthesis report.*

**Part 4**

If you have any comments about the exercise, please explain or e-mail them to a TA: mistakes in the text, difficulty level of the exercise, anything that will help us improve it for the next time.