Design of Digital Circuits: Lab Report		
Lab 6: Testing the ALU		
Date		Grade
Names		
		Lab session / lab room

You have to submit this report via Moodle.

Use a zip file or tarball that contains the report and any other required material. Only one member from each group should submit the report. All members of the group will get the same grade.

The name of the submitted file should be *Lab1_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.

Note 1: Please include all the required material. No links/shortcuts are accepted.

Note 2: The deadline for the report is a hard deadline and it will not be extended.

Exercise 1. Designing a Testbench for the FSM of Lab 4

In the manual, you learned how to design a testbench for a combinational circuit (the ALU.) In this exercise you will design a simple testbench for the FSM from Lab4.

In this exercise, you just need to use the testbench to pass the inputs to the unit under test, which is your FSM, and observe and verify the state transitions (current state and next state) in the waveforms. You do not need to provide the golden result and compare it with your FSM output through the testbench.

Note: Enable and disable the reset signal during the initialization phase. You also need to pass the clock signal to the FSM module.

In your submission, include your testbench Verilog code, your FSM codes from lab 4, your input file, and the print-screen of your state transitions in the waveforms for the case you set right signal equal to logic-1.

Feedback

If you have any comments about the exercise please add them here: mistakes in the text, difficulty level of the exercise, or anything that will help us improve it for the next time.