

Design of Digital Circuits

Lab 6 Supplement:

Testing the ALU

Prof. Onur Mutlu

ETH Zurich

Spring 2019

9 April 2019

What Will We Learn?

- In lab 6, you learn how to
 - write testbenches in Verilog to verify the functionality of the design.
 - Find and resolve bugs in your design
- Write a testbench that verifies the correctness of your ALU form Lab 5.
- Use the same testbench to find and solve bugs in a buggy ALU that we provide.

Preparation

- You are expected to finish Lab 5 before continuing with this lab, because we will be testing the ALU from lab 5.
- Download the material for lab 6, which includes:
 - A template/example for a **testbench file**
 - The template for the **test-vectors**
 - A Verilog description of an ALU, which **contains some bugs**

Part 1: Expected Results

- Before writing our testbench, we need to prepare a set of inputs that we know the **expected results** for.
- you will be given **a set of inputs** for the ALU designed in Lab 5.
- **Determine the correct 'result'** for each set and enter them to the file 'testvectors_hex.txt' that we provide.
- **For output 'zero':** directly set its expected value within the testbench

Part 2: Preparing the Testbench

- Create a project with your ALU from lab 5 and the testbench template we provided you with.
- Make the necessary modifications to the testbench.
- After this, we will have a testbench that will
 - Apply the vectors in the "testvectors_hex.txt" file
 - Check the actual outputs of our ALU against what we expect.

Part 3: Simulating the ALU

- Run behavioral simulation using Vivado's built-in simulator.

The screenshot displays the Vivado 2016.4 Behavioral Simulation environment. The main window shows a simulation error in the Tcl Console:

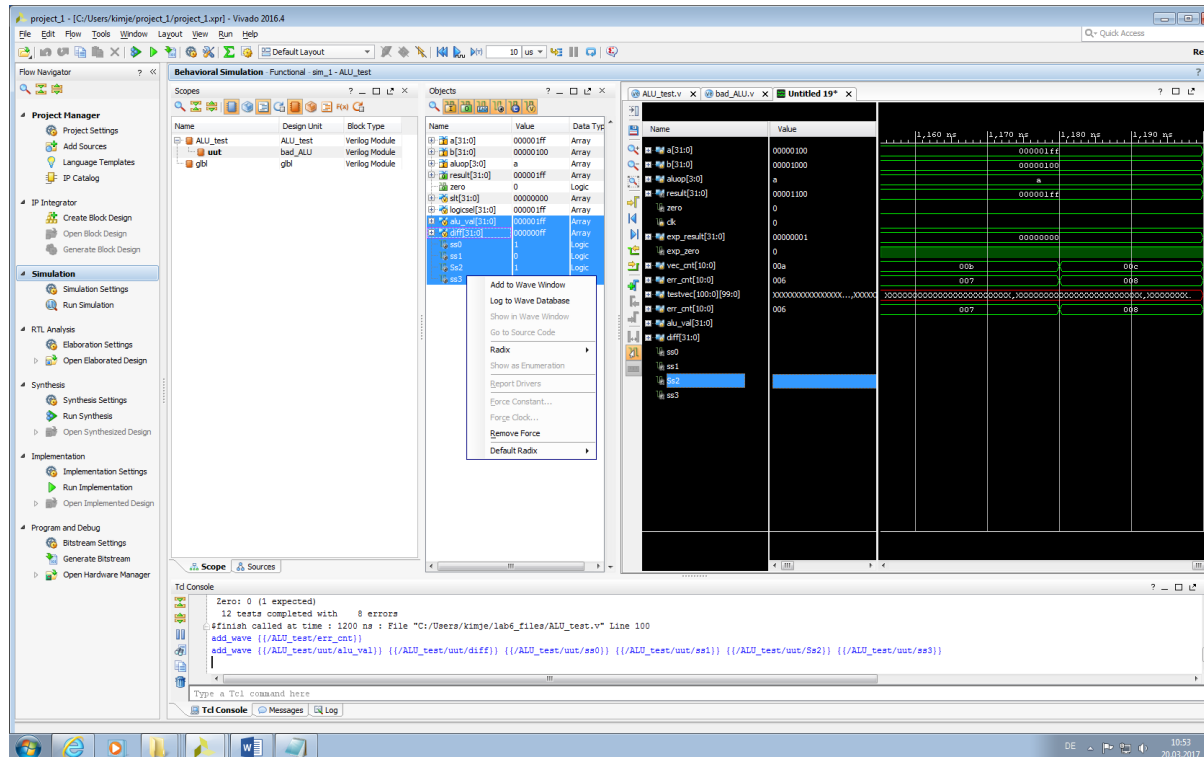
```
Error at 80 ns: Aluop 0000 a=00000000 b=00000000  
00000000 (00000001 expected)  
Zero: 1 (0 expected)  
INFO: [USF-XSim-96] XSim completed. Design snapshot 'ALU_test_behav' loaded.  
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

The timing diagram on the right shows the simulation results for various signals over time. The signals include a, b, aluop, result, zero, ck, exp_result, exp_zero, vec_cnt, and testvec. The error message indicates that the ALU operation result is 00000000, which does not match the expected result of 00000001.

- Errors
- Display messages

Part 4: Debugging the Problem

- Using a simulator can help you locate the problems in your circuits.
- You can not only observe the outputs but the state of all internal variables as well.



Last Words

- In lab 6, you learn how to
 - write testbenches in Verilog to verify the functionality of the design.
 - Find and resolve bugs in your design
- Write a testbench that verifies the correctness of your ALU form Lab 5.
- Use the same testbench to find and solve bugs in a buggy ALU that we provide.
- In the report, you will design a testbench for your FSM form lab 4.

Design of Digital Circuits

Lab 6 Supplement:

Testing the ALU

Prof. Onur Mutlu

ETH Zurich

Spring 2019

9 April 2019