

Design of Digital Circuits: Lab Report		
LAB 9 – The Performance of MIPS		
Date		Grade
Names		
		Lab session / lab room

You have to submit this report via Moodle.

Use a zip file or tarball that contains the report and any other required material. Only one member from each group should submit the report. All members of the group will get the same grade.

The name of the submitted file should be *LabN_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.

Note 1: Please include all the required material. No links/shortcuts are accepted.

Note 2: The deadline for the report is a hard deadline and it will not be extended.

Exercise 1

For the following values of A and B, how many clock cycles are needed to execute your first program from Lab 7 on your baseline MIPS processor, before adding optimizations of Lab 9? Assuming that we run the MIPS processor at 20 MHz, how much time (in seconds) would that take?

Value of A	Value of B	Number of cycles	Time in seconds
0	8		
6	8		
0	250'000'000		
249'999'996	250'000'002		

Exercise 2

Fill in the new values for the Table in Exercise 1 when using the modified MIPS architecture running the optimized code, as discussed in the manual for Lab 9.

Value of A	Value of B	Number of cycles	Time in seconds
0	8		
6	8		
0	250'000'000		
249'999'996	250'000'002		

Exercise 3

Compare the size/device utilization of the two implementations (before and after the modifications in Lab manual 9). What differences do you see? Briefly comment on them.
Hint: Look into the synthesis report.

Feedback

If you have any comments about the exercise please add them here: mistakes in the text, difficulty level of the exercise, or anything that will help us improve it for the next time.

