# Design of Digital Circuits
## Discussion Session 1

Prof. Onur Mutlu
ETH Zurich
Spring 2019
31 May 2019

# Discussion Session

- Boolean logic and truth table (HW2, Q4)
- Pipelining I (HW4, Q2)
- Out-of-order execution – Reverse engineering II (HW4, Q8)
- Branch prediction (HW5, Q9)
- Vector processing (HW6, Q1)
- GPU and SIMD III (HW6, Q6)
- Reverse engineering caches (HW7, Q2)

# Extra Discussion Session

- We will solve the Spring 2018 final exam

- We will set a poll in Moodle. Two possible dates:
  - Wednesday, June 12, 9am
  - Wednesday, July 10, 9am

- The poll will be open until Tuesday, June 4, 11:59pm

# Final Exam
# August 23, 2019, 2pm

# Preparing for the Final Exam

- 1. Study to understand the material and concepts. Understanding is the most important thing we will test for
- 2. Do the optional homeworks and understand them
- 3. Some questions on the exam will have similarity to optional homeworks and past exams. However, some questions on the exam will be different from those in the past exams and homeworks. Regardless, the questions will be designed to test your understanding of the material and the ability to think using that understanding
- 4. You can go over the lectures again to reinforce your understanding of the material. We would recommend this. As you know, all lecture videos are available on Youtube at https://www.youtube.com/playlist?list=PL5Q2soXY2Zi8J58xLKBNFQFHRO3GrXxA9
- 5. All material we covered in lectures and the labs can be part of the exam
- 6. We have made past exams and their solutions available online on the course webpage

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