1 Verilog (I)

Please answer the following three questions about Verilog.

(a) Does the following code result in a D Flip-Flop with a synchronous active-low reset? Please explain your answer.

```
module mem (input clk, input reset, input [1:0] d, output reg [1:0] q);
always @ (posedge clk or negedge reset)
begin
  if (!reset) q <= 0;
  else q <= d;
end
endmodule
```

No. The code implements two D Flip-Flops, not one. Each D Flip-Flop works with an asynchronous active-low reset signal.

Explanation:

- D and Q signals are two-bit-wide. Therefore, this code implements two D flip-flops.
- The reset input is included in the sensitivity list, therefore it is not synchronous.
- The code resets the output if the reset signal is low. Thus, the reset signal is active-low.
(b) Does the following code result in a sequential circuit or a combinational circuit? Please explain your answer.

```verilog
module Mask (input [1:0] data_in, input mask, output reg [1:0] data_out);
    always @ (*)
        begin
            data_out[1] = data_in[1];
            if (mask)
                data_out[0] = 0;
        end
endmodule
```

Sequential circuit.

**Explanation:**
This code results in a sequential circuit, as all the left-hand side signals are not assigned in every possible condition. For example, `data_out[0]` is not assigned when mask signal equals to zero.

(c) Is the following code syntactically correct? If not, please explain the mistake(s) and how to fix it/them.

```verilog
module fulladd (input a, b, c, output reg s, c_out);
    assign s = a^b;
    assign c_out = (a & b) | (b & c) & (c & a);
endmodule

module top (input wire [5:0] instr, input wire op, output z);
    reg [1:0] r1, r2;
    wire [3:0] w1, w2;
    fulladd FA1 (.a(instr[0]), .b(instr[1]), .c(instr[2]),
        .c_out(r1[1]), .z(r1[0]));
    fulladd FA2 (.a(instr[3]), .b(instr[4]), .c(instr[5]),
        .z(r2[0]), .c_out(r2[1]));
    assign z = r1 | op;
    assign w1 = r1 + 1;
    assign w2 = r2 << 1;
    assign op = r1 ^ r2;
endmodule
```

The code is not syntactically correct.

**Explanation:**
- `r1` and `r2` have to be declared as wires.
- `op` signal is connected to multiple drivers. It gets assigned from the input port and in line 19.
- The module `fulladd` does not have ports named `z`. Those need to be changed to `s`.
- The output signals `s` and `c_out` have to be declared as wires but not as regs, since they are driven by assign statements.
2 Verilog (II)

Please answer the following four questions about Verilog.

(a) Does the following code result in a D Flip-Flop with asynchronous reset? Please explain why.

```verilog
module dff (input clk, input reset, input [3:0] d, output reg [3:0] q);
always @ (posedge clk)
begin
  if (reset == 0) q <= 0;
  else q <= d;
end
endmodule
```

No.

Explanation:
Since the reset input is not included in the sensitivity list, this code will implement a synchronous D Flip-Flop.

(b) Does the following code result in a sequential circuit or a combinational circuit? Explain why.

```verilog
module concat (input clk, input data_in1, input data_in2, output reg [1:0] data_out);
always @ (posedge clk, data_in1, data_in2)
if (data_in1 > data_in2)
data_out = {data_in1, data_in2};
else
data_out = {data_in2, data_in1};
endmodule
```

Combinational circuit.

Explanation:
This code results in a combinational circuit because sensitivity list does include all inputs of the circuit: data_in1 and data_in2.
(c) Is the following code syntactically correct? If not, please explain the mistake(s) and how to fix it/them.

```verilog
module Inn3r ( input [3:0] d, input op , output s);
  assign s = op ? (d[1:0] - d[3:2]) :
               (d[3:2] + d[1:0]);
endmodule

module top ( input wire [6:0] instr , input wire op , output reg z);
  reg[1:0] r1 , r2 , r3;
  wire [3:0] w1 , w2;
  Inn3r i0 (.instr(instr[1:0]), .op(instr[7]), .z(r1));
  Inn3r i1 (.instr(instr[3:2]), .op(instr[0]), .z(r2));
  assign z = r1 | r2;
  assign w1 = r1 + 1;
  assign w2 = r2 << 1;
  top t (.instr({w1, w2, w1==w2}), .op(z), .z(r3));
  assign op = r1 ^ r2 ^ r3;
endmodule
```

The code is not syntactically correct.

**Explanation:**

- Modules cannot be instantiated recursively.
- 'r1' and 'r2' have to be declared as 'wire's.
- The module 'Inn3r' does not have ports named 'instr' and 'z'. Those need to be changed to 'd' and 's', respectively.
- Output 'z' is driven by two circuits: lines 14 and 18.
- The output signal 'z' has to be declared as a 'wire' but not 'reg'.
(d) Does the following code correctly implement a counter that counts down from 10 to 1 (e.g., 10, 9, 8, ..., 2, 1, 10, 9, ...) if so, say "Correct". If not, correct the code with minimal modification.

```verilog
module the_final_count_down (clk, count);
  wire clk;
  reg[3:0] count = 10;
  reg[3:0] count_next;

  always @ * begin
    count_next <= count;
    if(count != 1)
      count_next <= count_next - 1;
    else
      count_next <= 1;
  end

  always@(posedge clk)
    count = count_next;
endmodule
```

Answer and concise explanation:

No, the implementation is not correct.

Explanation:
The correct implementation:

```verilog
module the_final_count_down (clk, count);
  wire clk;
  reg[3:0] count = 10;
  reg[3:0] count_next;

  always @ * begin
    //count_next <= count;
    if(count != 1)
      count_next <= count - 1;
    else
      count_next <= 10;
  end

  always@(posedge clk)
    count = count_next;
endmodule
```
(e) Which of the combinational logic blocks does the following verilog code implement?

```verilog
module mystery(input select, input enable, output result);
    wire [3:0] result;
    wire [1:0] select;
    wire enable;

    assign result = enable << (select);
endmodule
```

A 2:4 decoder.

**Explanation:**
The code basically shifts `enable` by select positions. For example, if `enable` is 1 and `select` is 10, `result` will be `0100`. 
3 Finite State Machines (FSM) (I)

This question has three parts.

(a) An engineer has designed a deterministic finite state machine with a one-bit input \((A)\) and a two-bit output \((Z)\). He started the design by drawing the following state transition diagram:

Although the exact functionality of the FSM is not known to you, there are at least three mistakes in this diagram. Please list all the mistakes.

There are four problems with this diagram:

(a) Most states have a Moore labelling (output state in the bubble), one has a Mealy type labelling (output given with input transitions) red(5 points)

(b) There are two different transitions both with \(A = 1\) from state \(S1\). What will happen with \(A = 0\) is missing red(5 points)

(c) There are two different transitions from state \(S2\), without labeling which input triggers them red(5 points)

(d) There is no reset state red(5 points)
After learning from his mistakes, your colleague has proceeded to write the following Verilog code for a much better (and **different**) FSM. The code has been verified for syntax errors and found to be OK.

```verilog
module fsm (input CLK, RST, A, output [1:0] Z);

    reg [2:0] nextState, presentState;

    parameter start = 3'b000;
    parameter flash1 = 3'b010;
    parameter flash2 = 3'b011;
    parameter prepare = 3'b100;
    parameter recovery = 3'b110;
    parameter error = 3'b111;

    always @ (posedge CLK, posedge RST)
        if (RST) presentState <= start;
        else presentState <= nextState;

    assign Z = (presentState == recovery) ? 2'b11 :
            (presentState == error)  ? 2'b11 :
            (presentState == flash1) ? 2'b01 :
            (presentState == flash2) ? 2'b10 : 2'b00;

    always @ (presentState, A)
        case (presentState)
            start : nextState <= prepare;
            prepare : if (A) nextState <= flash1;
            flash1 : if (A) nextState <= flash2;
            else nextState <= recovery;
            flash2 : if (A) nextState <= flash1;
            else nextState <= recovery;
            recovery : if (A) nextState <= prepare;
            else nextState <= recovery;
            error  : if (~A) nextState <= start;
            default : nextState <= presentState;
        endcase

endmodule
```
Draw a proper state transition diagram that corresponds to the FSM described in this Verilog code.

(c) Is the FSM described by the previous Verilog code a Moore or a Mealy FSM? Why?

Moore, the output Z only depends on the state (presentState) and not on the input (A).
4 Finite State Machines (FSM) (II)

You are given the following FSM with two one-bit input signals ($T_A$ and $T_B$) and one two-bit output signal ($O$). You need to implement this FSM, but you are unsure about how you should encode the states. Answer the following questions to get a better sense of the FSM and how the three different types of state encoding we discussed in the lecture (i.e., one-hot, binary, output) will affect the implementation.

(a) There is one critical component of an FSM that is missing in this diagram. Please write what is missing in the answer box below.

The reset line or indication for initial state.

(b) What kind of an FSM is this?

Moore
(c) List one major advantage of each type of state encoding below.

<table>
<thead>
<tr>
<th>Encoding</th>
<th>Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>One-hot</td>
<td>reduces next-state logic</td>
</tr>
<tr>
<td>Binary</td>
<td>reduces FFs to hold state</td>
</tr>
<tr>
<td>Output</td>
<td>reduces output logic</td>
</tr>
</tbody>
</table>

(d) Fully describe the FSM with equations given that the states are encoded with one-hot encoding. Assign state encodings such that numerical values of states increase monotonically for states A through D while using the minimum possible number of bits to represent the states with one-hot encoding. Indicate the values you assign to each state and simplify all equations:

State assignments: A: 0001, B: 0010, C: 0100, D: 1000

\[
\begin{align*}
NS[1] &= T\overline{B} \times (TS[0] + TS[3]) \\
NS[0] &= TS[1] \times TA \\
\end{align*}
\]
(e) Fully describe the FSM with equations given that the states are encoded with binary encoding. Assign state encodings such that numerical values of states increase monotonically for states A through D while using the minimum possible number of bits to represent the states with binary encoding. Indicate the values you assign to each state and simplify all equations:

<table>
<thead>
<tr>
<th>State assignments: A: 00, B: 01, C: 10, D: 11</th>
</tr>
</thead>
<tbody>
<tr>
<td>$NS[1] = TS[1] \cdot (TS[0] \cdot TB + TS[0] \cdot TA) + TS[1] \cdot (TS[0] + TS[0] \cdot TB)$</td>
</tr>
<tr>
<td>$NS[0] = TS[1] \cdot TS[0] \cdot TB + TS[1]$</td>
</tr>
<tr>
<td>$O[1] = TS[1]$</td>
</tr>
<tr>
<td>$O[0] = TS[1] \text{ XOR } TS[0]$</td>
</tr>
</tbody>
</table>
(f) Fully describe the FSM with equations given that the states are encoded with output encoding. Use the minimum possible number of bits to represent the states with output encoding. Indicate the values you assign to each state and simplify all equations:

State assignments: A: 10, B: 11, C: 01, D: 00

\[
\begin{align*}
NS[1] &= TS[1] \cdot \overline{TS[0]} \cdot \overline{TB} + TS[1] \cdot TS[0] \cdot TA + \overline{TS[1]} \cdot \overline{TS[0]} \cdot TB \\
&= \overline{TS[0]} \cdot TB + TS[1] \cdot TS[0] \cdot TA \\
NS[0] &= TS[1] \cdot TS[0] + TS[1] \cdot TS[0] \cdot TA + \overline{TS[1]} \cdot \overline{TS[0]} \cdot TB \\
&= TS[1] \cdot (\overline{TS[0]} + TS[0] \cdot TA) + \overline{TS[1]} \cdot \overline{TS[0]} \cdot TB \\
O[0] &= TS[0]
\end{align*}
\]
(g) Assume the following conditions:

- We can only implement our FSM with 2-input AND gates, 2-input OR gates, and D flip-flops.
- 2-input AND gates and 2-input OR gates occupy the same area.
- D flip-flops occupy 3x the area of 2-input AND gates.

Which state-encoding do you choose to implement in order to minimize the total area of this FSM?

<table>
<thead>
<tr>
<th>Encoding</th>
<th>Logic Gates</th>
<th>FFs</th>
</tr>
</thead>
<tbody>
<tr>
<td>one-hot</td>
<td>10</td>
<td>4</td>
</tr>
<tr>
<td>binary</td>
<td>16</td>
<td>2</td>
</tr>
<tr>
<td>output</td>
<td>10</td>
<td>2</td>
</tr>
</tbody>
</table>

Output encoding has the least amount of circuitry elements.
5 Finite State Machines (FSM) (III)

You are given two one-bit input signals \( T_A \) and \( T_B \) and one one-bit output signal \( O \) for the following modular equation: \( 2N(T_A) + N(T_B) \equiv 2 \pmod{4} \). In this modular equation, \( N(T_A) \) and \( N(T_B) \) represent the total number of times the inputs \( T_A \) and \( T_B \) are high (i.e., logic 1) at each positive clock edge, respectively. The one-bit output signal, \( O \), is set to 1 when the modular equation is satisfied (i.e., \( 2N(T_A) + N(T_B) \equiv 2 \pmod{4} \)), and 0 otherwise. An example that sets \( O = 1 \) at the end of the fourth cycle would be:

- (1st cycle) \( T_A = 0 \) (\( N(T_A) = 0 \)), \( T_B = 0 \) (\( N(T_B) = 0 \)), \( 2N(T_A) + N(T_B) \equiv 0 \pmod{4} \) \( \Rightarrow O = 0 \)
- (2nd cycle) \( T_A = 1 \) (\( N(T_A) = 1 \)), \( T_B = 1 \) (\( N(T_B) = 1 \)), \( 2N(T_A) + N(T_B) \equiv 3 \pmod{4} \) \( \Rightarrow O = 0 \)
- (3rd cycle) \( T_A = 1 \) (\( N(T_A) = 2 \)), \( T_B = 0 \) (\( N(T_B) = 1 \)), \( 2N(T_A) + N(T_B) \equiv 1 \pmod{4} \) \( \Rightarrow O = 0 \)
- (4th cycle) \( T_A = 0 \) (\( N(T_A) = 2 \)), \( T_B = 1 \) (\( N(T_B) = 2 \)), \( 2N(T_A) + N(T_B) \equiv 2 \pmod{4} \) \( \Rightarrow O = 1 \)

(a) You are given a partial Moore machine state transition diagram that corresponds to the modular equation described above. However, the input labels of most of the transitions are still missing in this diagram. Please label the transitions with the correct inputs so that the FSM correctly implements the above specification.
the FSM with Boolean equations assuming that the states are encoded with **one-hot encoding**. Assign state encodings while using the **minimum** possible number of bits to represent the states. Please indicate the values you assign to each state.

| State assignments: 0 (mod 4): 0001, 1 (mod 4): 0010, 2 (mod 4): 0100, 3 (mod 4): 1000 |
| CS denotes current states, and NS denotes next states. |
| $NS[0] = CS[0] \overline{T_A} \overline{T_B} + CS[1] T_A T_B + CS[2] T_A \overline{T_B} + CS[3] \overline{T_A} T_B$ |
| $NS[1] = CS[1] \overline{T_A} \overline{T_B} + CS[2] T_A T_B + CS[3] T_A \overline{T_B} + CS[0] \overline{T_A} T_B$ |
| $NS[2] = CS[2] \overline{T_A} \overline{T_B} + CS[3] T_A T_B + CS[0] T_A \overline{T_B} + CS[1] \overline{T_A} T_B$ |
| $NS[3] = CS[3] \overline{T_A} \overline{T_B} + CS[0] T_A T_B + CS[1] T_A \overline{T_B} + CS[2] \overline{T_A} T_B$ |
| $O[0] = CS[2]$ |
(b) Describe the FSM with Boolean equations assuming that the states are encoded with **binary encoding** (i.e., fully encoding). Assign state encodings while using the **minimum** possible number of bits to represent the states. Please indicate the values you assign to each state.

State assignments: 0 (mod 4): 00, 1 (mod 4): 01, 2 (mod 4): 10, 3 (mod 4): 11

CS denotes current states, and NS denotes next states.

\[
\begin{align*}
NS[0] &= CS[0] \cdot T_B + CS[0] \cdot T_B \\
NS[1] &= CS[0] \cdot (CS[1] \text{ XOR } TA \text{ XOR } TB) + CS[0] \cdot (TA \text{ XOR } CS[1]) \\
O[0] &= CS[1] \cdot CS[0]
\end{align*}
\]
(c) Consider an implementation of the FSM assuming that the states are encoded with output encoding. What is the minimum number of bits required to encode the states with output encoding?

A minimum of three bits are required to represent the state $2 \pmod{4}$ uniquely so that the output logic layer is minimized. If we consider that the state assignments are as follows:

- $0 \pmod{4}$: 000
- $1 \pmod{4}$: 001
- $2 \pmod{4}$: 100
- $3 \pmod{4}$: 011

Then the output logic would be:

$$O[0] = CS[2]$$

There is no way of achieving this minimization using two bits, as we did with fully encoding, because $CS[1] = 1$ for both states $2 \pmod{4}$ and $3 \pmod{4}$. Since only $2 \pmod{4}$ should set $O = 1$, we would need to make sure that $CS[0] = 0$ while $CS[1] = 1$. Thus, it is impossible to have the same minimization as we did for output encoding with three-bit representation of the states.