Lab 8 Overview

- You will build a whole single-cycle processor and write assembly code that runs on the FPGA board.

- You will learn how a processor is built.

- Learn how the processor communicates with the outside world.

- Implement the MIPS processor and demonstrate a simple “snake” program on the FPGA starter kit.
Lab 8 Sessions

- **Session I:** The Crawling Snake
- **Session II:** Speed Up the Snake
Lab 8 Session II: Speed Up the Snake

- Extend the top-level hierarchy:
  - Modify the I/O controller to accept the inputs.

- Understand the provided assembly program and modify your assembly code to accept inputs.
  - The snake should crawl at different speeds for different inputs.
  - The inputs will be controlled by switches on the FPGA board.

- Optionally, you have two challenge tasks to complete.
  - Change the direction of the snake.
  - Change the pattern of the snake.
Lab 8 Session II: Summary of the Flow

HW

Edit Verilog files in Vivado

Check Syntax

Modify the XDC file if needed

SW

Edit .asm files in MARS

Assemble and simulate The code in MARS

Dump the data & instruction memory as hex text files.

Generate the FPGA bit file in Vivado
Lab 8 Session II: Extending I/O

**HW**
- Edit Verilog files in Vivado
- Check Syntax
- Modify the XDC file if needed

**SW**
- Edit .asm files in MARS
- Assemble and simulate The code in MARS
- Dump the data & instruction memory as hex text files.

Generate the FPGA bit file in Vivado
Lab 8 Session II: Modifying the Assembly

**HW**
- Edit Verilog files in Vivado
- Check Syntax
- Modify the XDC file if needed

**SW**
- Edit .asm files in MARS
- Assemble and simulate the code in MARS
- Dump the data & instruction memory as hex text files.

Generate the FPGA bit file in Vivado
Last Words

- You will build a whole single-cycle processor and write assembly code that runs on the FPGA board.
- You will learn how a processor is built.
- Learn how the processor communicates with the outside world.
- Implement the MIPS processor and demonstrate a simple “snake” program on the FPGA starter kit.
- You will have some questions to answer in the report.
23:59, 4 June 2021
Digital Design & Computer Arch.

Lab 8 Supplement:
Full System Integration

Prof. Onur Mutlu

ETH Zürich
Spring 2021
18 May 2021