

Technical Note

Calculating Memory System Power for DDR2

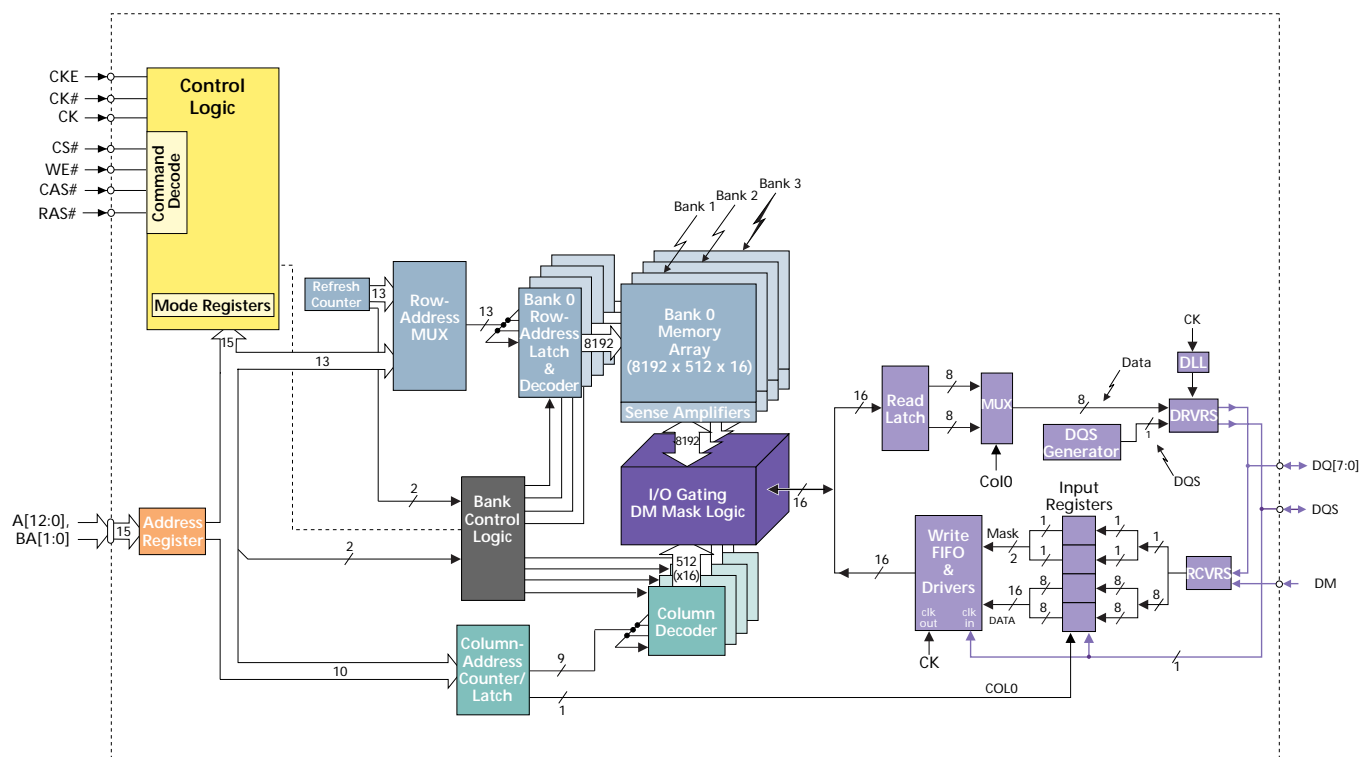
Introduction

This technical note details how DDR2 SDRAM consumes power, and it provides the tools system designers need to estimate power consumption in a given system. In addition to offering tools and techniques for calculating system power, examples are provided. The core equations and examples through Figure 9 on page 17 use the sample I_{DD} values for x8 components shown in Table 4 on page 18. AC timing values are available in the DDR2 -533, 512Mb data sheet at www.micron.com.

DRAM Operation

To estimate the power consumption of a DDR2 SDRAM, it is necessary to understand the basic functionality of the device (see Figure 1). The basic operation of a DDR2 device is similar to that of a DDR device. For both, the master operation of the DRAM is controlled by clock enable (CKE).

Figure 1: 256Mb DDR2 SDRAM Functional Block Diagram



If CKE is LOW, the DDR2 clock and input buffers are turned off. However, to communicate with the device, CKE must be HIGH, which enables the inputs and propagates the clock through the DRAM.

With CKE HIGH, commands can be sent to the DDR2 device. Typically, the first command (after the initialization) is ACTIVATE (ACT). This command selects a bank and row address and transfers the row's cell data, which is stored in the array, to the sense amplifiers, putting the device in the active state. The data stays in the sense amplifiers until a PRECHARGE (PRE) command to the same bank restores the data to the cells in the array, putting the device in the precharge state.

In the active state, the DDR2 device can perform READs and WRITEs. A READ command decodes a specific column along the row that is stored in the sense amplifiers. The data from this column is driven through the I/O gating to the internal read latch. From there, it is multiplexed onto the output drivers. The process for a WRITE is just the opposite. Data from the DQ pins is latched into the data receivers/registers and transferred to the internal data drivers. The drivers then transfer the data to the sense amplifiers through the I/O gating, to the decoded column address.

While DDR2 and DDR share similarities in basic operation, DDR2 adds on-die termination (ODT) to the data I/O pins. This feature is controlled by the ODT pin and consumes additional power when activated. Typically, on-die termination is only enabled to terminate write data to the DRAM or to terminate read data from a different DRAM. (For more information, see Micron Technical Note TN-47-02, "DDR2 SDRAM Offers New Features and Functionality.")

DRAM Power Calculations

The I_{DD} values referenced in this article are taken from Micron's 512Mb DDR2-533 SDRAM data sheet and are listed in "Sample I_{DD} Specifications" on page 18. While values provided in data sheets may differ from vendor to vendor and over time, the concepts behind calculating power are the same. It is important to verify all data sheet parameters before using the information in this article.

Three steps are required to calculate system power. First, the power subcomponents are calculated based on data sheet specifications. (This calculation is denoted as $P_{ds}(XXX)$, where XXX is the subcomponent power.) Then, the power is derated based on the command scheduling in the system [$P_{sch}(XXX)$]. Lastly, the power is derated to the system's actual operating V_{DD} and clock frequency [$P_{sys}(XXX)$]. The sum of the subcomponents is the total power consumed by the DRAM.

Background Power

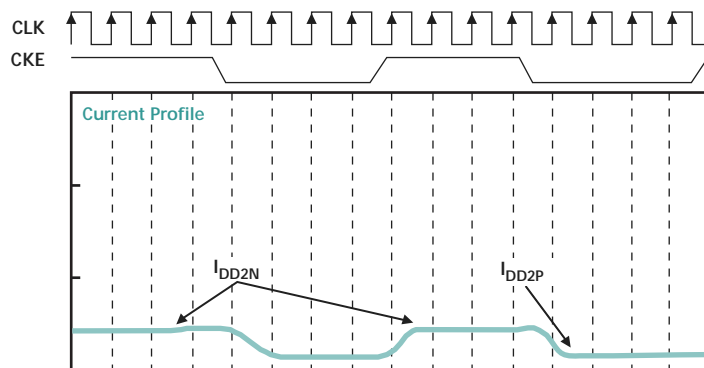
As stated previously, CKE is the master on-off switch for the DRAM. When CKE is LOW, all inputs, including clocks, are disabled. This is the lowest power state in which the device can operate and is specified in the data sheet as I_{DD2P} if all the banks are precharged. If any bank is open, the current consumed is I_{DD3P} . I_{DD3P} has two possible values, depending on whether mode register bit 12 is set for a slow or fast exit time from power-down, so the correct value must be entered. Slow exit is the lowest-power exit.

CKE must be taken HIGH to read or write data to the DDR2 SDRAM. When CKE goes HIGH, the clock signals start propagating through the device, and it prepares to receive commands. This activity within the DRAM, which increases the power consumption, is specified in the data sheet as I_{DD2N} .

Figure 2 shows the typical current use of a DDR2 device when CKE transitions, assuming all banks are precharged. When CKE is HIGH, the device draws approximately 45mA of current; when CKE goes LOW, that figure drops to 5mA.

Figure 2 assumes the device is in the precharge state. Thus, when CKE is HIGH, the DDR2 device uses I_{DD2N} current; and when CKE is LOW, it uses I_{DD2P} current. Similarly, if the device is in the active state, it consumes I_{DD3P} current in the power-down state (CKE = LOW) and I_{DD3N} current in standby (CKE = HIGH).

Figure 2: Effects of CKE



The power consumed by a DDR2 device is easily calculated by multiplying the I_{DD} values by the voltage applied to the device V_{DD} . Note that the data sheet specifications for all I_{DD} values are taken at worst-case V_{DD} , which is 1.9V for DDR2. The equations are solved as follows:

$$P_{ds}(\text{PRE_PDN}) = I_{DD2P} \times V_{DD}$$

$$P_{ds}(\text{PRE_PDN}) = 5mA \times 1.9V$$

$$P_{ds}(\text{PRE_PDN}) = 10mW$$

(Eq. 1)

$$P_{ds}(\text{PRE_STBY}) = I_{DD2N} \times V_{DD}$$

$$P_{ds}(\text{PRE_STBY}) = 45mA \times 1.9V$$

$$P_{ds}(\text{PRE_STBY}) = 86mW$$

(Eq. 2)

$$P_{ds}(\text{PRE_PDN}) = I_{DD3P} \times V_{DD}$$

$$P_{ds}(\text{PRE_PDN}) = 25mA \times 1.9V$$

$$P_{ds}(\text{PRE_PDN}) = 48mW$$

(Eq. 3)

$$P_{ds}(\text{PRE_STBY}) = I_{DD3N} \times V_{DD}$$

$$P_{ds}(\text{PRE_STBY}) = 45mA \times 1.9V$$

$$P_{ds}(\text{PRE_STBY}) = 86mW$$

(Eq. 4)

Note: I_{DD3P} in the above equations assumes MR12 = 0 (fast exit mode).

During normal operation, the DRAM always consumes one of four background powers. The amount of power consumed depends on whether all of the banks are precharged or one or more banks are activated. Additionally, the percent of time that CKE is LOW or HIGH during each of the conditions determines standby versus power-down currents. The three parameters in Table 1 are used to define the percent of time that the DRAM is in each power state.

Table 1: DDR2 Background Power Components

Component	Description
BNK_PRE%	Percent of time all banks are precharged
CKE_LO_PRE%	Percent of bank PRE time that CKE is LOW
CKE_LO_ACT%	Percent of bank ACT time that CKE is LOW

Equation 5 is used to derive the ratios of the background powers to the various data sheet powers, based on CKE HIGH/LOW times. Note that these numbers cover 100% of the total device operating time.

$$P_{sch}(\text{PRE_PDN}) = P_{ds}(\text{PRE_PDN}) \times \text{BNK_PRE\%} \times \text{CKE_LO_PRE\%}$$

$$P_{sch}(\text{PRE_PDN}) = P_{ds}(\text{PRE_PDN}) \times \text{BNK_PRE\%} \times \text{CKE_LO_PRE\%}$$

$$P_{sch}(\text{PRE_STBY}) = P_{ds}(\text{PRE_STBY}) \times \text{BNK_PRE\%} \times 1 - \text{CKE_LO_PRE\%}$$

$$P_{sch}(\text{ACT_PDN}) = P_{ds}(\text{ACT_PDN}) \times [1 - \text{BNK_PRE\%}] \times \text{CKE_LO_PRE\%}$$

$$P_{sch}(\text{ACT_STBY}) = P_{ds}(\text{ACT_STBY}) \times [1 - \text{BNK_PRE\%}] \times [1 - \text{CKE_LO_PRE\%}]$$

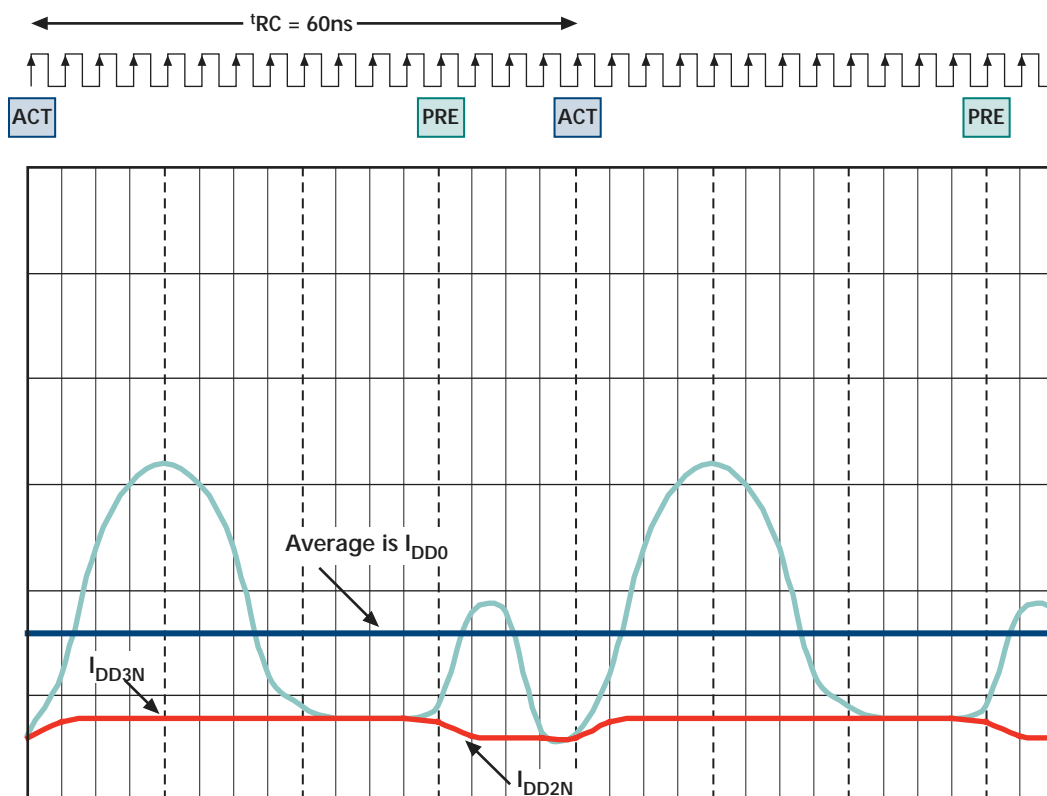
(Eq. 5)

Activate Power

To be useful, a DDR2 SDRAM must read and write data. To complete this task, a row must first be selected using an ACT command, along with a bank and row address. For every ACT command, there is a corresponding PRE command. The ACT command opens a row, and the PRE closes the row. The ACT and PRE commands are always paired together even though other commands may exist between them.

Figure 3 on page 5 shows a typical current profile for I_{DD0} . Following an ACT command, the device uses a significant amount of current to decode the command/address and then transfer the data from the DRAM array to the sense amplifiers. When this is complete, the DRAM is maintained in an active state until a PRE command is issued. The PRE command restores the data from the sense amplifiers into the memory array and resets the bank for the next ACT command. Then, the device is returned to the precharge state. For I_{DD0} , this cycle is repeated at t_{RC} intervals between ACT commands.

Figure 3: I_{DD0} Current Profile



The data sheet specifies I_{DD0} averaged over time, as represented by the dark blue line. During this operation, a base amount of background current is always consumed (I_{DD3N} when the row is active and I_{DD2N} when the row is precharged). This background current must be subtracted from I_{DD0} to identify the power consumed by the ACT and PRE commands. This is shown in Equation 6, where I_{DD3N} is subtracted from I_{DD0} during the t_{RAS} (row active) time and I_{DD2N} is subtracted during the remaining time.

$$Pds(CT) = \left[I_{dd0} - \frac{I_{DD3N} \times t_{RAS} + I_{DD2N} \times (t_{RC} - t_{RAS})}{t_{RC}} \right] \times V_{DD}$$

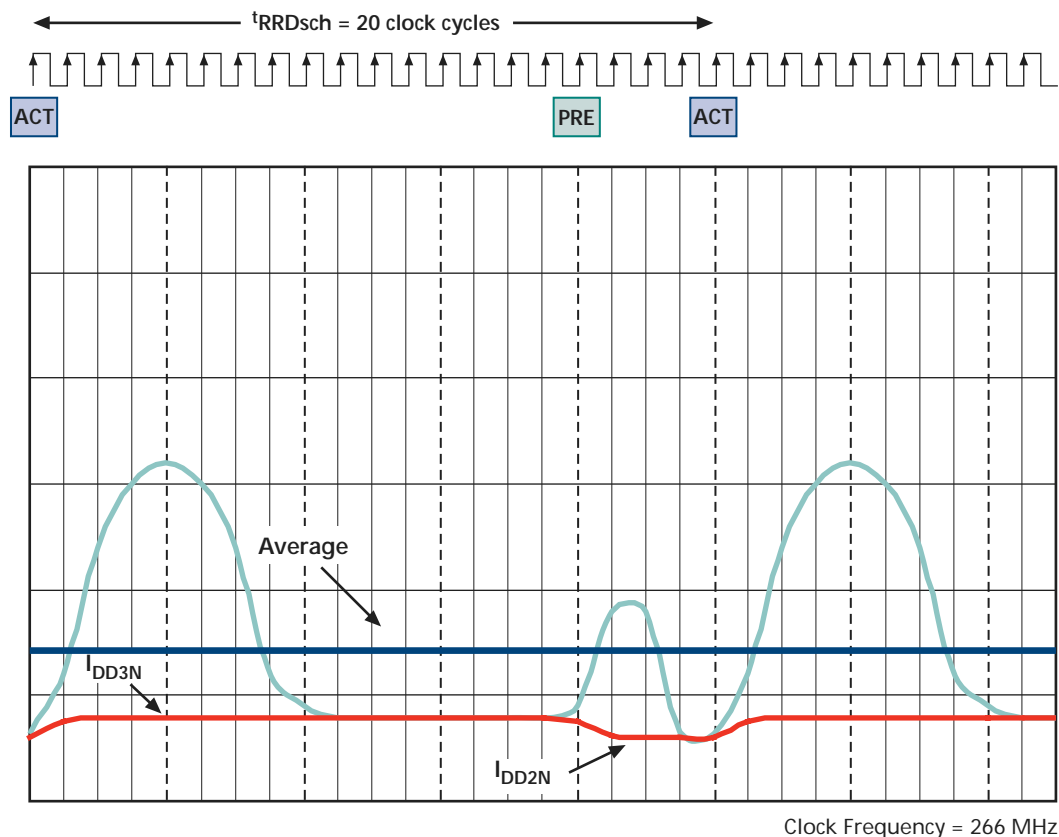
$$Pds(CT) = \left[80mA - \frac{[45mA \times 45ns] + [45mA \times (60ns - 45ns)]}{60ns} \right] \times 1.9V$$

$$Pds(CT) = 67mW$$

(Eq. 6)

Equation 6 is correct only if the DRAM is used at the minimum t_{RC} cycle time specified in the data sheet. This is noted as $P_{ds}(ACT)$, meaning “power under data sheet conditions.” However, not many systems operate in this manner. Fortunately, it is easy to scale the ACT current for other modes of operation. The scaling factor is represented as t_{RRDsch} , which is the average scheduled row-to-row activate timing. Two examples of scaling activate power with different spacings are shown in Figure 4 on page 6: one when t_{RRDsch} is greater than t_{RC} , and a second when the device is in bank interleave mode.

Figure 4: ACT-to-ACT Current with $t_{RRDsch} = 75ns$



In Figure 4, the average ACT-to-ACT cycle time is greater than the specified $t_{RC} = 60ns$, and t_{RRDsch} is stretched to 20 clock cycles, which is 75ns for a 266 MHz clock.

The I_{DD0} value can be easily scaled as a ratio of the actual t_{RRDsch} value to the data sheet t_{RC} conditions. The calculations are as follows:

$$P_{sch}(ACT) = P_{ds}(ACT) \times \frac{t_{RC}}{t_{RRDsch}}$$

$$P_{sch}(ACT) = 67mW \times \frac{60ns}{75ns}$$

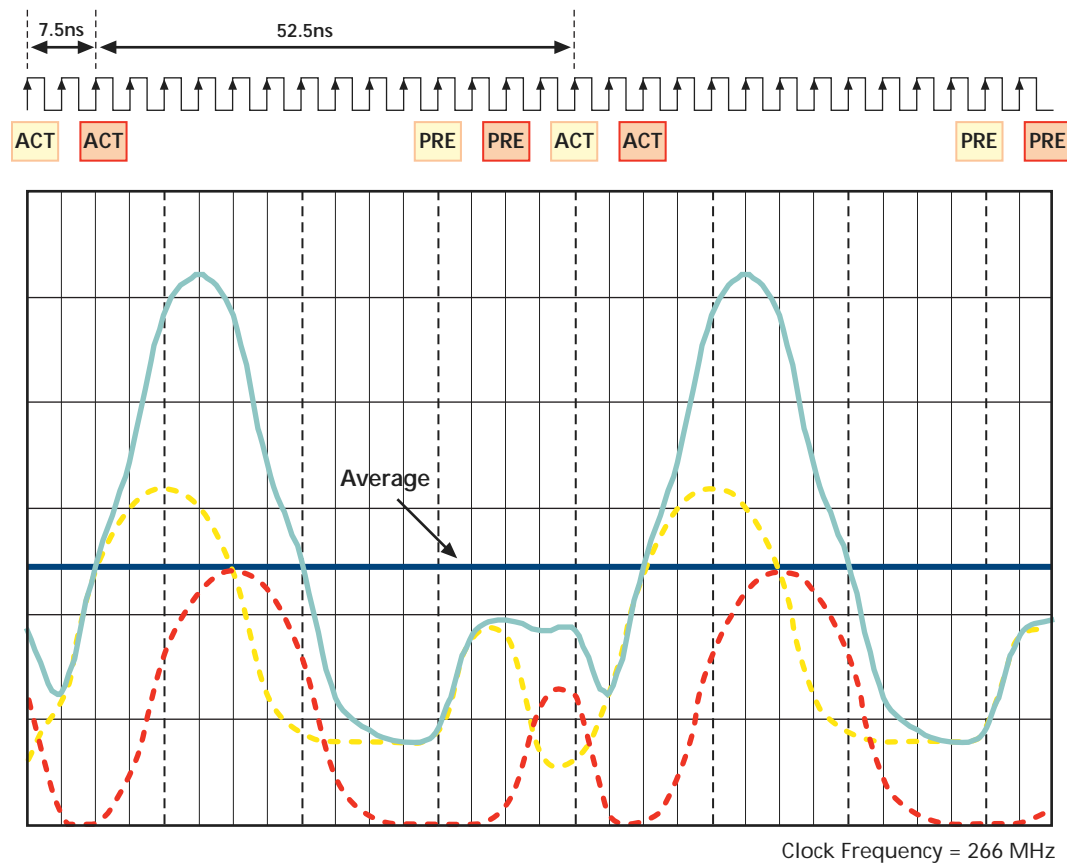
$$P_{sch}(ACT) = 54mW$$

(Eq. 7)

Therefore, by changing the ACT-to-ACT time from 60ns to 75ns, the activation power, $P_{sch}(ACT)$, drops from 67mW to 54mW. Note that this power is only the activation power and does not include the background power contributed by I_{DD2N} and I_{DD3N} .

Because a DDR2 device has multiple banks, it is possible to have several open rows at one time. Therefore, it is also possible to have ACT commands closer together than t_{RC} . Figure 5 on page 7 shows an example in which two banks are interleaved within 60ns, making the average t_{RRDsch} 30ns. Because t_{RRDsch} is an average, it does not matter that some commands are spaced 7.5ns apart while others are 52.5ns apart (see Figure 5). The yellow current profile represents the first bank activated and includes the I_{DD3N} component. This I_{DD3N} is only included one instance on the device, even if other banks are open. The red current profile, which represents the second bank activated, is offset by the lack of I_{DD3N} . The green curve represents the sum of the two banks.

Figure 5: ACT-to-ACT Current for Average $t_{RRDsch} = 30ns$



The calculation to determine the power consumption for the activation power is the same as before:

$$P_{sch}(ACT) = 67mW \times \frac{60ns}{30ns}$$

$$P_{sch}(ACT) = 134mW$$

(Eq. 8)

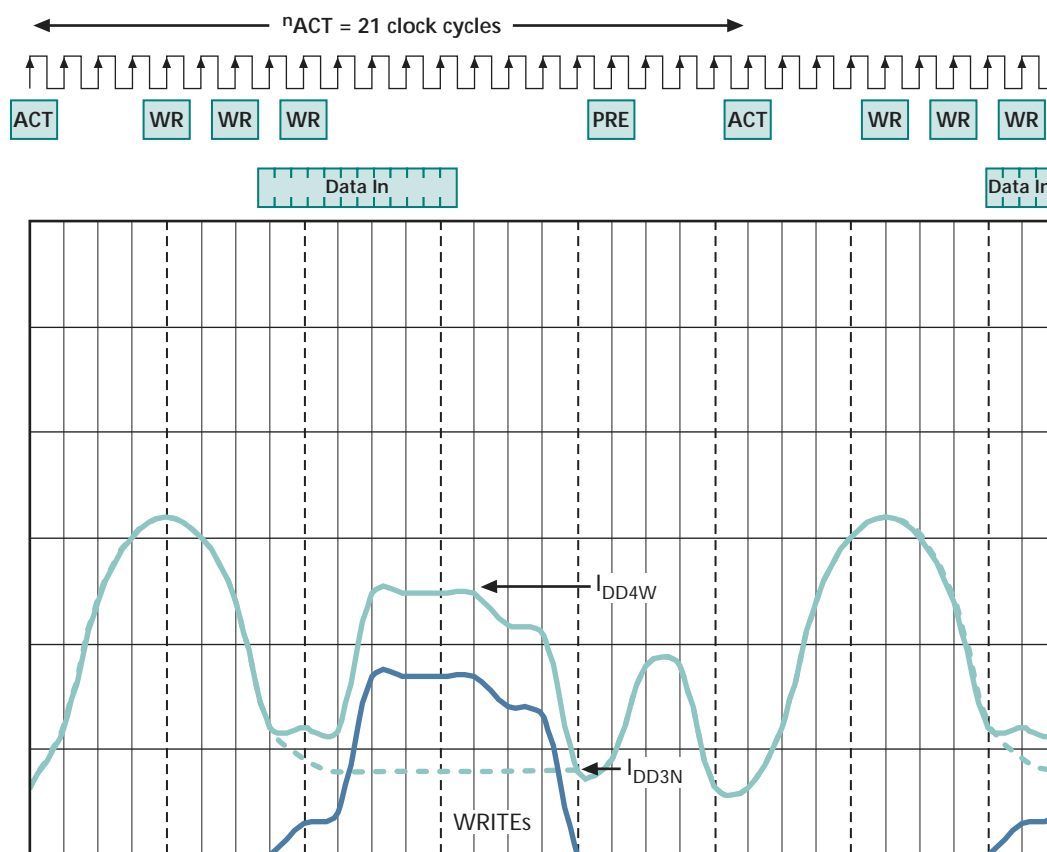
The $P_{sch}(ACT)$ for two interleaved banks increases from 67mW to 134mW, because twice the amount of ACT and PRE power is consumed when operating two banks compared to one.

With this basic equation, the ACT-to-PRE power can be calculated for any use condition, from eight interleaved banks to one bank that is seldom opened.

Write Power

When a bank is open, data can be either read from or written to the DDR2 SDRAM. The two cases are similar; see Figure for an example of a WRITE cycle.

WRITE Cycle



When several WRITES are added between ACT commands, the consumption of current associated with the WRITE is I_{DD4W} . To identify the power associated with only the WRITES and not the standby current, I_{DD3N} must be subtracted. The calculation for the data sheet write component of power, $P_{ds}(WR)$, is shown in Equation 9.

$$P_{ds}(WR) = (I_{DD4W} - I_{DD3N}) \times V_{DD}$$

$$P_{ds}(WR) = (130mA - 45mA) \times 1.9V$$

$$P_{ds}(WR) = 162mW$$

(Eq. 9)

To scale the data sheet power to actual power based on command scheduling, it must be calculated as a ratio of the write bandwidth. This is noted as $WRsch\%$, which is the total number of clock cycles that write data is on the bus (not WRITE commands) versus the total number of clock cycles. The $WRsch\%$ calculation is shown in Equation 10.

$$WRsch\% = \frac{\text{number of clock cycles with WRITE data on the bus}}{^nACT}$$

$$WRsch\% = \frac{6\text{clock cycles}}{21\text{clock cycles}}$$

$$WRsch\% = 29\%$$

(Eq. 10)

Where nACT = number of clock cycles from ACT to ACT

When the ratio of WRITES is known, the power associated with the scheduled WRITES, $Psch(WR)$, can be easily calculated from the data sheet write power, as shown in Equation 11.

$$Psch(WR) = Pds(WR) \times WRsch\%$$

$$Psch(WR) = Pds(WR) \times 29\%$$

$$Psch(WR) = 47mW$$

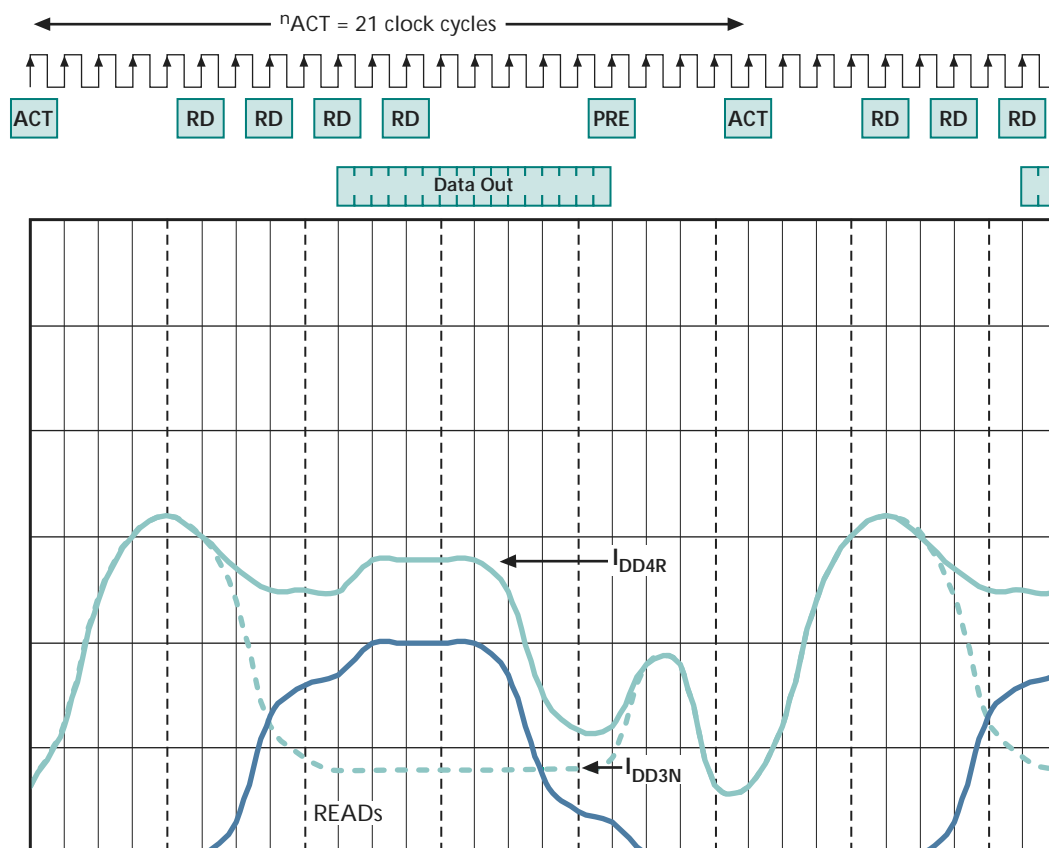
(Eq. 11)

The data sheet conditions specify I_{DD4W} with $BL = 4$. DDR2 devices often operate with burst lengths other than four. This causes the DDR2 device to generate additional addresses for the column locations associated with subsequent bits in the data burst. The power consumed is still approximated by counting how many clocks of data-in are used for the WRITE. Therefore, if a WRITE using $BL = 8$ is completed, it would require approximately the same amount of power as two WRITES with $BL = 4$ (four clock cycles).

Read Power

The power required to read data is similar to that needed to write data, as shown in Figure 6. A row is opened with an ACT command, and then a burst of four READs is started to columns in that row. After the READs are complete, the row is closed with a PRE command and the sequence is restarted.

Figure 6: Read Current Profile



The read current profile looks very similar to the write current profile. The average current is calculated exactly the same as in the write case, except I_{DD4R} is substituted for I_{DD4W} .

$$Pds(RD) = (I_{DD4R} - I_{DD3N}) \times V_{DD}$$

$$Pds(RD) = (145mW - 45mA) \times 1.9V$$

$$Pds(RD) = 190mW$$

(Eq. 12)

To scale the data sheet power to actual power based on command scheduling, it must be calculated as a ratio of the read bandwidth. This is denoted as $RDsch\%$, which is the total number of read data cycles (not READ commands) that are on the data bus versus the total number of clock cycles. The $RDsch\%$ calculation is shown in Equation 13.

$$RD_{sch}\% = \frac{\text{number of RD cycles with data on the bus}}{^nACT}$$

$$RD_{sch}\% = \frac{8 \text{ clock cycles}}{21 \text{ clock cycles}}$$

$$RD_{sch}\% = 38\%$$

(Eq. 13)

Where nACT = number of clock cycles from ACT to ACT

After the ratio of READs is known, the power associated with the scheduled READs, $Psch(RD)$, can be easily calculated from the data sheet read power in Equation 14.

$$Psch(RD) = Pds(RD) \times RD_{sch}\%$$

$$Psch(RD) = 190mW \times 38\%$$

$$Psch(RD) = 72mW$$

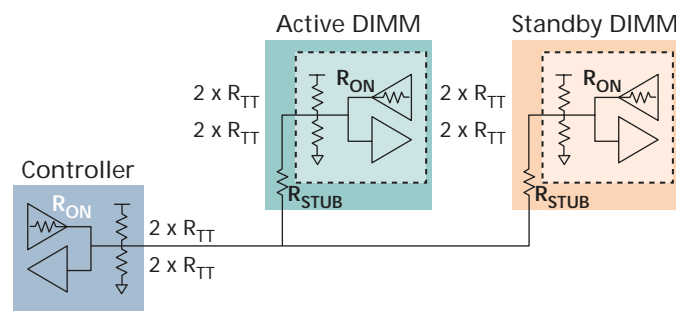
(Eq. 14)

I/O and Termination Power

$Psch(RD)$ and $Psch(WR)$ are only part of the total power for read and write sequences. This is because the actual I/O power and termination power vary depending on system configuration and must be calculated for each system; therefore, they have not been included.

A typical system data bus with two DIMMs is shown in Figure 7. Each DIMM has a DRAM that can transmit or terminate the data bus.

Figure 7: Typical System DQ Termination



A typical termination scheme is shown in Table 2. Further information is available on the Micron Web site.

Table 2: Termination Configuration

	Controller		DRAM	
	R_{ON}	R_{TT}	R_{ON}	R_{TT}
1 DIMM	35 Ω	75 Ω during READs	18 Ω	150 Ω during WRITEs
2 DIMMs	30 Ω	150 Ω during READs	18 Ω	150 Ω during READs and WRITEs (on standby module only)

Two methods can be used to calculate the power consumed by the output driver or on-die termination. One is to simulate the data bus in the system using SPICE models of all components and then average a sufficiently long pattern of pseudo random data. A simpler method, however, is to calculate the DC power of the output driver against the termination. This is usually not worst-case, but it provides a first-order approximation of the output power.

The I/O powers that must be calculated are:

- Pd_{qRD}: The output driver power when driving the bus
- Pd_{qWR}: The termination power when terminating a WRITE to the DRAM
- Pd_{qRDoth}: The termination power when terminating a READ from another DRAM
- Pd_{qWRoth}: The termination power when terminating write data to another DRAM

Typical DC powers for the system in Figure 7 on page 11 are shown in Table 3 on page 12. These powers are per DQ pin.

To calculate the power for output or termination on the DRAM, the power per DQ must be multiplied by the number of DQ and strobes on the device (num_DQR). For write termination, data masks must also be included in the sum of the total number of write signals that must be terminated (num_DQW). This will vary, depending on mode register settings for differential strobe enable and RDQS enable.

Equation 15 calculates the DRAM power for the following four I/O buffer operations:

- Pds(DQ): DRAM output driver power when driving the bus
- Pds(termW): DRAM termination power when terminating a WRITE to the DRAM
- Pds(termRoth): DRAM termination power when terminating a READ from another DRAM
- Pds(termWoth): DRAM termination power when terminating write data to another DRAM

Table 3: Typical I/O and Termination Power Consumption

		DC Power	
		READ	WRITE
1 DIMM – 1 Rank/DIMM		Pd _{qRD} = 1.1mW	Pd _{qWR} = 8.2mW
2 DIMMs 2 Ranks/DIMM	Receiving/ Transmitting DIMM	Pd _{qRD} = 1.5mW	Pd _{qWR} = 0mW
	Terminating DIMM	Pd _{qRDoth} = 13.1mW	Pd _{qWRoth} = 14.6mW

$$\begin{aligned}
 Pds(DQ) &= Pdq(RD) \times \text{num_DQR} \\
 Pds(\text{term}W) &= Pdq(WR) \times \text{num_DQW} \\
 Pds(\text{termRoth}) &= Pdq(RD\text{oth}) \times \text{num_DQR} \\
 Pds(\text{termWoth}) &= Pdq(WRW\text{Roth}) \times \text{num_DQW}
 \end{aligned}
 \tag{Eq. 15}$$

To illustrate how the power is calculated, a 2-DIMM system is assumed, using a x8 device with differential strobes enabled and RDQS disabled. With the differential strobe enabled, num_DQR includes 8 DQ and 2 DQS signals for a total of 10, whereas num_DQW totals 11 to account for the addition of the data mask. The DC power values from Figure 3 are also used and the results are presented in Equation 16.

$$\begin{aligned}
 Pds(DQ) &= 1.5mW \times 10 = 15mW \\
 Pds(\text{term}W) &= 0mW \times 11 = 0mW \\
 Pds(\text{termRoth}) &= 13.1mW \times 10 = 131mW \\
 Pds(\text{termWoth}) &= 14.6mW \times 11 = 161mW
 \end{aligned}
 \tag{Eq. 16}$$

To complete the I/O and termination power calculation, the 100% use data sheet specification must be derated based on data bus utilization. The read and write utilization has already been provided as RDschd% and WRschd%. Two additional terms are required to cover the termination case for data to/from another DRAM. These are termRDsch% (terminating read data from another DRAM) and termWRsch% (terminating write data to another DRAM). The power based on command scheduling is then calculated as:

$$\begin{aligned}
 Psch(DQ) &= Pds(DQ) \times RDsch\% \\
 Psch(\text{term}W) &= Pds(\text{term}W) \times RWsch\% \\
 Psch(\text{termRoth}) &= Pds(\text{termRoth}) \times \text{termRDsch} \\
 Psch(\text{termWoth}) &= Pds(\text{termWoth}) \times \text{termWRsch}
 \end{aligned}
 \tag{Eq. 17}$$

Sample calculations showing how to determine the output and termination percentages are provided in “System Examples” on page 19. An I/O power calculator is provided on the Micron Web site, under Support > DRAM > System-Power Calculators.

Refresh Power

The final power component that must be calculated for the device to retain data integrity is refresh. DDR2 memory cells store data information in small capacitors that lose their charge over time and must be recharged. The process of recharging these cells is called refresh.

The specification for refresh in the DDR2 data sheet is I_{DD5} . I_{DD5} assumes the DRAM is operating continuously at minimum REFRESH-to-REFRESH command spacing, t_{RFC} (MIN). During this operation, the DRAM is also consuming I_{DD3N} standby current. Thus, to calculate only the power due to refresh, I_{DD3N} must be subtracted, as shown in Equation 18.

$$P_{ds}(REF) = (I_{DD5} - I_{DD3N}) \times V_{DD}$$

$$P_{ds}(REF) = (200mA - 45mA) \times 1.9V$$

$$P_{ds}(REF) = 295mW$$

(Eq. 18)

However, refresh operations are typically distributed evenly over time at a refresh interval of t_{REFI} . Thus, the scheduled refresh power, $P_{sch}(REF)$, is the ratio of t_{RFC} (MIN) to t_{REFI} , multiplied by $P_{ds}(REF)$, as shown in Equation 19.

$$P_{sch}(REF) = P_{ds}(REF) \times \frac{t_{RFC}(MIN)}{t_{REFI}}$$

$$P_{sch}(REF) = 295mW \times \frac{105ns}{7.85\mu s}$$

$$P_{sch}(REF) = P_{ds}(REF) = 4mW$$

(Eq. 19)

Power Derating

Thus far, the power calculations have assumed a system operating at worst-case V_{DD} . They have also assumed the clock frequency in the system is the same as the frequency defined in the data sheet. The resulting power is denoted as $P_{sch}(XXX)$. However, most systems operate at different clock frequencies or operating voltages than the ones defined in the data sheet. Each of the power components must be derated to the actual system conditions, with the resulting power denoted as $P_{sys}(XXX)$.

The following section explains how to derate each of the power components to an actual system.

Voltage Supply Scaling

All power calculations thus far have been calculated at the maximum specified V_{DD} . However, systems often operate closer to a nominal V_{DD} , with most power components scaling as V_{DD} changes. The only power parameters that do not scale with V_{DD} are the data I/O and termination power because the system V_{DD} is already assumed when the initial power is calculated.

On DRAM devices, power is typically related to the square of the voltage. This is because most of the power is dissipated by capacitance, with $P = cV^2f$ where c is the internal capacitance, V is the supply voltage, and f is the frequency of the clock or command (see next section). Thus, to scale power to a different supply voltage:

$$P_{sys}(XXX) = P_{sch}(XXX) \times \left[\frac{use V_{DD}}{Max spec V_{DD}} \right]^2$$

(Eq. 20)

Frequency Scaling

Many power components, such as $P_{sch}(ACT_STBY)$, $P_{sch}(IDLE_STBY)$, $P_{sch}(WR)$, and $P_{sch}(RD)$, are dependent on the clock frequency at which a device operates. Other powers, such as $P_{sch}(PRE_PDN)$ and $P_{sch}(ACT_PDN)$, are not because the clock is disabled during power-down mode.

Similarly, $P_{sch}(REF)$ does not scale with clock frequency, and $P_{sch}(ACT)$ is dependent on the interval between ACT commands, rather than clock frequency.

The power for components that are dependent on operating frequency can be scaled for actual operating frequency:

$$P_{sys}(XXX) = P_{sch}(XXX) \times \frac{use_freq}{spec_freq} \quad (Eq. 21)$$

The use_freq is the actual clock frequency at which a device operates in the system. The $spec_freq$ is the clock frequency at which the device was tested during the I_{DD} tests. This information is provided in the test condition notes in a data sheet. The test condition notes also describe tests at the minimum clock rate for a specific CAS latency, and that value is specified under the t_{CK} parameter.

The combination of all V_{DD} and clock frequency scaling is presented in Equation 22 on page 15.

$$\begin{aligned} P_{sys}(PRE_PDN) &= P_{sch}(PRE_PDN) \times \left[\frac{use\ VDD}{Max\ spec\ VDD} \right]^2 \\ P_{sys}(ACT_PDN) &= P_{sch}(ACT_PDN) \times \left[\frac{use\ VDD}{Max\ spec\ VDD} \right]^2 \\ P_{sys}(PRE_STBY) &= P_{sch}(PRE_STBY) \left[\frac{use_freq}{spec_freq} \right] \times \left[\frac{use\ VDD}{Max\ spec\ VDD} \right]^2 \\ P_{sys}(ACT_STBY) &= P_{sch}(ACT_STBY) \left[\frac{use_freq}{spec_freq} \right] \times \left[\frac{use\ VDD}{Max\ spec\ VDD} \right]^2 \\ P_{sys}(ACT) &= P_{sch}(ACT) \times \left[\frac{use\ VDD}{Max\ spec\ VDD} \right]^2 \\ P_{sys}(WR) &= P_{sch}(WR) \times \left[\frac{use_freq}{spec_freq} \right] \times \left[\frac{use\ VDD}{Max\ spec\ VDD} \right]^2 \\ P_{sys}(RD) &= P_{sch}(WRRD) \times \left[\frac{use_freq}{spec_freq} \right] \times \left[\frac{use\ VDD}{Max\ spec\ VDD} \right]^2 \\ P_{sys}(REF) &= P_{sch}(REF) \times \left[\frac{use\ VDD}{Max\ spec\ VDD} \right]^2 \end{aligned} \quad (Eq. 22)$$

Calculating Total System Power

The tools are now in place to calculate the system power for any use condition. The last task is to put them together. The various system power subcomponents are summed together, as shown in Equation 23:

$$\begin{aligned}
 P_{sys}(TOT) = & P_{sys}(PRE_PDN) + P_{sys}(PRE_STBY) \\
 & + P_{sys}(ACT_PDN) + P_{sys}(ACT_STBY) + P_{sys}(WR) \\
 & + P_{sys}(RD) + P_{sys}(REF) + P_{sys}(DQ) + P_{sys}(termW) \\
 & + P_{sys}(termRoth) + P_{sys}(termWoth)
 \end{aligned}$$

(Eq. 23)

Having compensated for all primary variables that can affect device power, the total power dissipation of a DDR2 device operating under specific system-use conditions has now been calculated.

DDR2 System-Power Calculator

Calculating all of these equations by hand can be tedious. For this reason, Micron has published an on-line workbook to simplify the process. Micron's DDR2 SDRAM System-Power Calculator, as well as detailed instructions for its use, are available on the Micron Web site. Examples of system-power calculations are provided in "System Examples" on page 19.

To utilize the on-line spreadsheet, enter the device data sheet conditions on the "DDR2 Spec" tab. Starting values are provided, but it is important to verify all data sheet parameters prior to using the spreadsheet. Note that multiple speed bins and DRAM densities are included, and correct inputs are required for each column.

After the data sheet values are entered, the actual DRAM configuration to be used for the power calculations is selected on the workbook "DDR2 Config" tab, as shown in Figure 8. The density, I/O configuration, and speed grade are selected with pull-down menus. In addition, the mode register configuration is selected for the differential strobe, RDQS, and PD exit mode. These inputs correctly configure the calculator for a specific DRAM based on the data input on the "DDR2 Spec" worksheet.

Figure 8: Spreadsheet – DRAM Configuration Tab

DRAM density	512Mb	▲▼
Number of DQs per DRAM	x8	▲▼
Speed grade	-37E	▲▼
Extended mode register bit 10: Differential strobe enable	1: Enable	▲▼
Extended mode register bit 11: RDQS enable	0: Disable	▲▼
Mode register bit 12: PD exit mode	0: Fast	▲▼

After the DRAM configuration has been selected, the system operating conditions are input on the "System Config" tab, as shown in Figure 9. The actual system operating V_{DD} and clock frequency are entered. Output power consumption and bus utilization are also entered, along with CKE conditions.

Two new parameters are also entered, which were not discussed previously: burst length and PageHit% rate. They are used to calculate t_{RRDsch} , as shown in Equation 23 on page 16.

After all the inputs are entered, the actual DRAM device power derated to the system conditions can be found on the “Summary” tab. Note that the interim power calculations for data sheet power and scheduled power can also be found in the system-power calculator worksheet.

See “System Examples” on page 19 for specific system examples.

Figure 9: Spreadsheet – System Configuration Tab

	System V _{DD}	1.8	V	
	System CK frequency	200	MHz	
	Burst length	4		Must be either 4 or 8.
PdqRD	DDR2 SDRAM output power per individual DQ on this DRAM	1.5	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
PdqWR	DDR2 SDRAM termination power per individual DQ during WRITES to this DRAM	0	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
PdqRDoth	DDR2 SDRAM termination power per individual DQ during READs from other DRAM	13.1	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
PdqWRoth	DDR2 SDRAM termination power per individual DQ during WRITES to other DRAM	14.6	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
BNK_PRE%	The percentage of time that all banks on the DRAM are in a precharged state	20%		
CKE_LO_PRE%	Percentage of the all bank precharge time for which CKE is held LOW	0%		
CKE_LO_ACT%	Percentage of at least one bank-active time for which CKE is held LOW	0%		
PH%	Page hit rate	0%		
RDsch%	The percentage of clock cycles outputting read data from the DRAM	15%		
WRsch%	The percentage of clock cycles inputting write data to the DRAM	5%		
termRDsch%	The percentage of clock cycles terminating read data to another DRAM	15%		Must be 0% for a 1-rank system.
termWRsch%	The percentage of clock cycles terminating write data to another DRAM	5%		Must be 0% for a 1-rank system.
tRRDsch	The average time between ACT commands to this DRAM (includes ACT to same or different banks in the same DRAM device)	50.0	ns	This is calculated from page hit rate read/write bus utilization. No entry is necessary.

Sample I_{DD} Specifications

Table 4: Data Sheet Assumptions for Micron's 512Mb DDR2-533 ^{1, 2}

$0^{\circ} \times C \leq T_{case} \leq +85^{\circ} C$; $V_{DDQ} = +1.8V \pm 0.1V$; $V_{DD} = +1.8V \pm 0.1V$

Parameter/Condition	Symbol	-37E		Units
		x8	x16	
Operating current: One-bank active precharge; $t_{RC} = 60ns$; $t_{CK} = 3.75ns$; $t_{RAS} = 45ns$	I_{DD0}	80	110	mA
Precharge power-down current: All banks idle; $t_{CK} = 3.75ns$ MIN; CKE = LOW	I_{DD2P}	5	5	mA
Precharge standby current: All Banks Idle; $CS_{-} = HIGH$; $t_{CK} = 5ns$; CKE = HIGH	I_{DD2N}	45	50	mA
Active power-down current: All banks open, $t_{CK} = 5ns$; CKE = LOW	I_{DD3P}	25	25	mA
		5	5	
Active standby current: All banks open; $CS_{-} = HIGH$; $t_{CK} = 5ns$; CKE = HIGH	I_{DD3N}	45	55	mA
Operating burst READ current: All banks open; BL = 4; $t_{CK} = 3.75ns$ $I_{OUT} = 0mA$	I_{DD4R}	145	195	mA
Operating burst WRITE current: All banks open; BL = 4; $t_{CK} = 3.75ns$	I_{DD4W}	130	190	mA
Burst REFRESH current CKE = HIGH; $t_{RFC} = 75ns$	I_{DD5}	200	210	mA

- Notes: 1. I_{DD} is dependent on output loading, cycle rates, $I_{OUT} = 0mA$, and on-die termination disabled.
2. Refer to data sheet for the most current information.

System Examples

Three examples are provided to show how to use the Micron System-Power Calculator at www.micron.com. The first is for a single-module PC system with a 266 MHz clock under a moderate workload. The second is for a two-module (two ranks per module) system with a 200 MHz clock under a high-stress workload. The final example is a lower-power system, similar to the first but operating with a lower-stress workload and aggressive power management.

Example 1: DDR2-533 Moderate Use

The first example for calculating DDR2 power in a system environment is based on a PC2-4300 system using one module comprised of x8, 512Mb devices operating at a clock rate of 266 MHz. Differential strobes and a normal PD exit mode are assumed. The “DDR2 Config” tab is shown in Figure 10, and the system-use conditions are shown in Figure 11 on page 20.

Note: The power calculator will estimate power for a single DRAM device. In this example, a 64-bit SRx8 UDIMM is used, which incorporates eight (8) DRAM. After calculating the power for one DRAM, multiply this value times the number of DRAM on the module, which is eight, to determine total module power.

Read bus utilization of 45% and write bus utilization of 15% are assumed. With only one rank of memory in the system, all of the bandwidth must come from a single rank, so all DRAM will be in the same condition. DRAM in this rank will never terminates data to another DRAM.

To support this bandwidth a burst length of four is assumed with a page hit rate of 50%. Based on the high bus utilization, no CKE power management is assumed, and there is always at least one bank active on the DRAM. Note that t_{RRDsch} is calculated at an average of 25ns over all accesses.

After these assumptions are entered into the spreadsheet, the spreadsheet calculates each subcomponent of power and derates it to the system-use condition. A summary of the results is shown in Figure 5 on page 21. Under these system conditions, a total of 80mW is used for the background operations, including all power-down, standby, and refresh powers. An average of 143mW is consumed activating banks, while 117mW is consumed actually reading and writing data to the DDR2 SDRAM. The sum of these powers shows the total device draws $\approx 340\text{mW}$ of power during a moderate workload.

Figure 10: DRAM Configuration for Example 1

DRAM density	512Mb	▲▼
Number of DQs per DRAM	x8	▲▼
Speed grade	-37E	▲▼
Extended mode register bit 10: Differential strobe enable	1: Enable	▲▼
Extended mode register bit 11: RDQS enable	0: Disable	▲▼
Mode register bit 12: PD exit mode	0: Fast	▲▼

Figure 11: System Configuration for Example 1

System V_{DD}	1.8	V	Inputs: Device operating conditions
System CK frequency	266	MHz	
Burst length	4		
PdqRD	1.1	mW	Inputs: Estimated termination power per device pin
PdqWR	8.2	mW	
PdqRDoth	0	mW	
PdqWRoth	0	mW	
BNK_PRE%	0%		Inputs: Type and amount of time device is in power-down
CKE_LO_PRE%	0%		
CKE_LO_ACT%	0%		
PH%	50%		Inputs: System usage conditions
RDsch%	45%		
WRsch%	15%		
termRDsch%	0%		Inputs: Amount of time device is terminating
termWRsch%	0%		
t_{RRDsch}	25.0	ns	Result: Average ACT-to-ACT time

Table 5: Power Consumption Summary for Example 1

Reference	Power per DRAM	Power per 64-Bit SRx8 UDIMM ¹
Psys(PRE_PDN)	0.0mW	0
Psys(PRE_STBY)	0.0mW	0
Psys(ACT_PDN)	0.0mW	0
Psys(ACT_STBY)	76.5mW	612mW
Psys(REF)	3.6mW	28.8mW
Total Background Power	80.1mW	640.8mW
Psys(ACT)	143.2mW	1.146mW
Total ACTIVATE Power	143.2mW	1.146mW
Psys(WR)	21.7mW	173.6mW
Psys(RD)	76.5mW	612mW
Psys(DQ)	5.0mW	40mW
Psys(TERM)	13.5mW	108mW
Total READ/WRITE/Term Power	116.7mW	933.6mW
Total DDR2 SDRAM Power	340.1mW¹	2.72W

Notes: 1. The total 340mW power shown is for a single DRAM. The module is 64 bits wide and a total of eight DRAM are on the module; the total module (assuming unbuffered DIMMs) is 340mW times 8 DRAM, or 2.7W.

Figure 12: Power Consumption per Device for Example 1

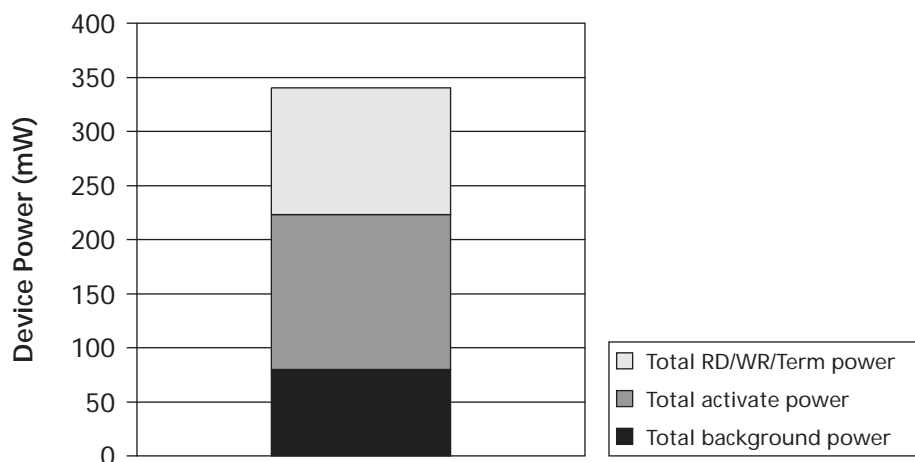
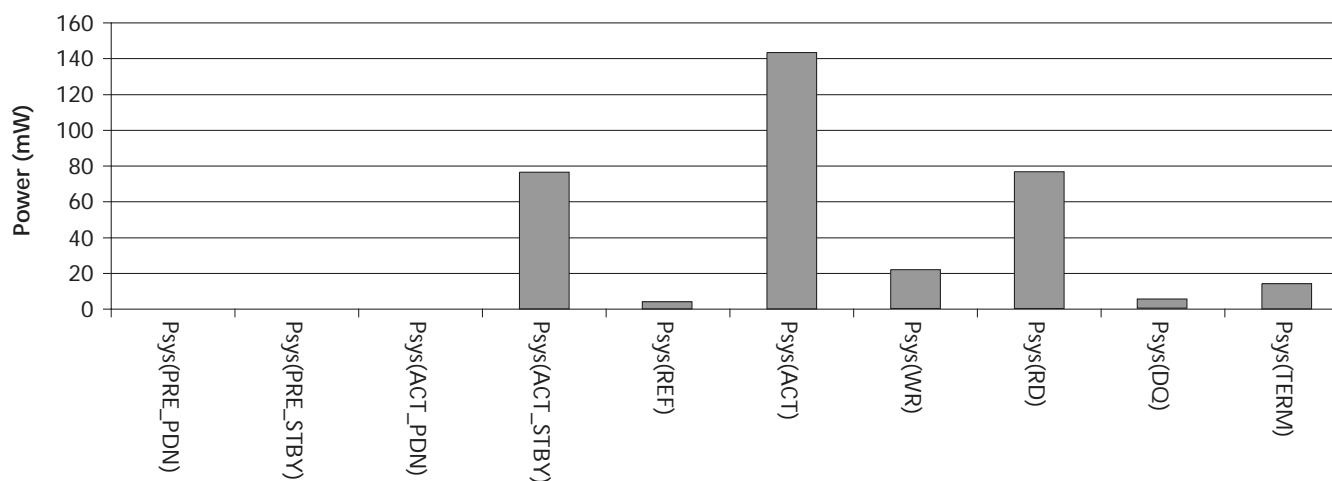


Figure 13: Power Consumption Breakout for Example 1



Example 2: DDR2-400 High Use

The second example is for a high-stress workload in a four-rank system. The system contains two modules with two ranks of memory on each, operating at a 200 MHz clock.

A high read bus utilization of 60% and write bus utilization of 20% are assumed. However, with four ranks of memory, each DRAM only averages 15% read bus utilization (60%/4 ranks) and 5% write bus utilization (20%/4 ranks). Additionally, each DRAM will terminate READs from other DRAM devices 15% of the time, and will terminate WRITES to other DRAM 5% of the time.

To support this bandwidth, a burst length of four is assumed, with a page hit rate of zero. No CKE use is assumed (CKE = HIGH), and because the bus utilization is not as large, it is assumed that all the pages are closed 20% of the time.

The system-use conditions from the system-power calculator worksheet are shown in Figure 16 on page 25. Note that the t_{RRDsch} is calculated to be an average of 50ns over all accesses. Even though the total bus utilization is high and there are no page hits, the actual average t_{RRDsch} is longer because the ACT commands are spread among four ranks of DRAM.

Figure 14: System Configuration for Example 2

System V_{DD}	1.8	V	Inputs: Device operating conditions
System CK frequency	200	MHz	
Burst length	4		
PdqRD	1.1	mW	Inputs: Estimated termination power per device pin
PdqWR	8.2	mW	
PdqRDoth	0	mW	
PdqWRoth	0	mW	
BNK_PRE%	20%		Inputs: Type and amount of time device is in power-down
CKE_LO_PRE%	0%		
CKE_LO_ACT%	0%		
PH%	0%		Inputs: System usage conditions
RDsch%	15%		
WRsch%	2%		
termRDsch%	15%		Inputs: Amount of time device is terminating
termWRsch%	5%		
t_{RRDsch}	50	ns	Result: Average ACT-to-ACT time

After these assumptions are entered into the spreadsheet, it calculates each subcomponent of power and derates it to the system use condition. A summary of the results is shown in Table 6. Under these system conditions, a total of 61mW of power is used for the background operations, including power-down, standby, and refresh. An average of 72mW is consumed activating banks, while 54mW is consumed actually reading and writing data to the DDR2 SDRAM. The sum of these powers shows that each device draws $\approx 190\text{mW}$ of power during a high workload.

Table 6: Power Consumption Summary for Example 2

Reference	Power per DRAM	Power per Module ¹
Psys(PRE_PDN)	0.0mW	0
Psys(PRE_STBY)	11.5mW	184mW
Psys(ACT_PDN)	0.0mW	0
Psys(ACT_STBY)	46.0mW	736mW
Psys(REF)	3.6mW	57.6mW
Total Background Power	61.1mW	977.6mW
Psys(ACT)	71.6mW	1.146mW
Total Activate Power	71.6mW	1.146mW
Psys(WR)	5.4mW	86.4mW
Psys(RD)	19.2mW	307.2mW
Psys(DQ)	2.1mW	33.6mW
Psys(TERM)	27.7mW	443.2mW
Total Read/Write/Term Power	54.4mW	870.4mW
Total DDR1 SDRAM Power	187.1mW	2.99W

Note that 190mW is for a single DRAM. If a module is 64 bits wide and a total of 16 DRAM are on each module, with 8 DRAM per rank and 2 ranks per module, the total module power consumption (assuming unbuffered DIMMs) is 190mW times 16 DRAM, or $\approx 3\text{W}$.

Example 3: DDR2-533 Low Use

The third example for calculating DDR2 SDRAM power in a system environment is for a PC2-4300 system that operates with a 266 MHz clock, 45% READs, 15% WRITEs, 50% hit rate, without termination for 10% of the time, and in power-down the remaining 90% of the time. Also, a single module of x16 components is used, along with a slow PD exit time. The “DDR2 Config” tab is shown in Figure 15. The system-use conditions are shown in Figure 16.

Figure 15: DRAM Configuration for Example 3

DRAM density	512Mb	⬆️⬆️
Number of DQs per DRAM	x16	⬆️⬆️
Speed grade	-37E	⬆️⬆️
Extended mode register bit 10: Differential strobe enable	1: Enable	⬆️⬆️
Extended mode register bit 11: RDQS enable	0: Disable	⬆️⬆️
Mode register bit 12: PD exit mode	1: Slow	⬆️⬆️

Figure 16: System Configuration for Example 3

System V_{DD}	1.8	V	Inputs: Device operating conditions
System CK frequency	266	MHz	
Burst length	4		
PdqRD	1.1	mW	Inputs: Estimated termination power per device pin
PdqWR	8.2	mW	
PdqRDoth	0	mW	
PdqWRoth	0	mW	
BNK_PRE%	60%		Inputs: Type and amount of time device is in power-down
CKE_LO_PRE%	90%		
CKE_LO_ACT%	80%		
PH%	50%		Inputs: System usage conditions
RDsch%	5%		
WRsch%	2%		
termRDsch%	0%		Inputs: Amount of time device is terminating
termWRsch%	0%		
t_{RRDsch}	214.8	ns	Result: Average ACT-to-ACT time

With a 45% READ, and WRITES occurring only 10% of the time (device is in power-down 90% of the time), actual read bus utilization is $\approx 5\%$, and write bus utilization is $\approx 2\%$.

It is assumed that the DRAM will have all banks in the precharge state 60% of the time, and CKE LOW 80% of the time if one or more banks are active. Under these conditions, t_{RRDsch} has an average of 215ns over all accesses.

After these assumptions are entered into the spreadsheet, it calculates each subcomponent of power and derates it to the system-use condition. A summary of the results is shown in Table 7. Under these system conditions, a total of 22mW of power is used for the background operations, including power-down, standby, and refresh. An average of 31mW is consumed activating banks, while 16mW is consumed actually reading and writing data to the DDR2 SDRAM. The sum of these powers shows that the total device draws $\approx 70\text{mW}$ of power during a moderate workload.

Table 7: Power Consumption Summary for Example 3

Reference	Power per DRAM	Power per Module ¹
Psys(PRE_PDN)	4.6mW	18.4mW
Psys(PRE_STBY)	4.6mW	18.4mW
Psys(ACT_PDN)	2.7mW	10.8mW
Psys(ACT_STBY)	6.1mW	24.4mW
Psys(REF)	3.6mW	14.4mW
Total Background Power	21.1mW	84.4mW
Psys(ACT)	31.0mW	124mW
Total Activate Power	31.0mW	124mW
Psys(WR)	2.9mW	11.6mW
Psys(RD)	8.5mW	34mW
Psys(DQ)	1.1mW	4.4mW
Psys(TERM)	3.6mW	14.4mW
Total Read/Write/Term Power	16.1mW	64.4mW
Total DDR1 SDRAM Power	68.7mW	274.8W

Notes: 1. If a module is 64 bits wide and a total of four DRAM are on the module, the total module power consumption (assuming an unbuffered DIMM) is 70mW times 4 DRAM, or $\approx 0.3W$.

Summary

Relying on a data sheet alone, it can be difficult to determine how much power a DDR2 device will consume in a system environment. However, by understanding the data sheet and how a DDR2 device consumes power, it is possible to create a power model based on system-use conditions. Such a model can enable system designers to experiment with various memory access schemes to determine the impact on power consumption, i.e., more aggressive use of power-down (CKE = LOW) or changes to data access patterns (page hit percentages). In short, system designers can use this tool to estimate realistic power requirements for DDR2 devices and adjust a system's power delivery and thermal budget accordingly, optimizing system performance versus cost.

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Revision History

Rev. B	3/11
<ul style="list-style-type: none">• Updated values for current product capabilities• Updated formats	
Rev. A	4/04
<ul style="list-style-type: none">• Initial release	