First, We Will Complete Combinational Logic
We Covered Combinational Logic Blocks

- Basic logic gates (AND, OR, NOT, NAND, NOR, XOR)
- Decoder
- Multiplexer
- Full Adder
- Programmable Logic Array (PLA)
- Comparator
- Arithmetic Logic Unit (ALU)
- Tri-State Buffer

- Standard form representations: SOP & POS
- Logical completeness
- Logic simplification via Boolean Algebra
Logic Simplification using Boolean Algebra Rules
Recall: Full Adder in SOP Form Logic

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<thead>
<tr>
<th>$a_i$</th>
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Goal: Simplified Full Adder

How do we simplify Boolean logic?

How do we automate simplification?

\[
S = A \oplus B \oplus C_{in} \\
C_{out} = AB + AC_{in} + BC_{in}
\]

<table>
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<tr>
<th>(C_{in})</th>
<th>A</th>
<th>B</th>
<th>(C_{out})</th>
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Quick Recap on Logic Simplification

- The original Boolean expression (i.e., logic circuit) may not be optimal
  
  \[ F = \neg A(A + B) + (B + AA)(A + \neg B) \]

- Can we reduce a given Boolean expression to an equivalent expression with fewer terms?
  
  \[ F = A + B \]

- The goal of logic simplification:
  - Reduce the number of gates/inputs
  - Reduce implementation cost

A basis for what the automated design tools are doing today
Logic Simplification

- Systematic techniques for simplifications
  - amenable to automation

**Key Tool: The Uniting Theorem** — \( F = A\overline{B} + AB \)

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<thead>
<tr>
<th>A</th>
<th>B</th>
<th>F</th>
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\[
F = A\overline{B} + AB = A(\overline{B} + B) = A(1) = A
\]

**Essence of Simplification:**
Find two element subsets of the ON-set where only one variable changes its value. This single varying variable can be eliminated!

\( \rightarrow B \) is eliminated, \( A \) remains

\[
G = \overline{A}\overline{B} + AB = (\overline{A} + A)\overline{B} = \overline{B}
\]

- B's value stays the same within the ON-set rows
- A's value changes within the ON-set rows

\( \rightarrow A \) is eliminated, \( B \) remains
Logic Simplification Example: Priority Circuit

- **Priority Circuit**
  - **Inputs:** “Requestors” with priority levels
  - **Outputs:** “Grant” signal for each requestor
  - **Example 4-bit priority circuit**

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<table>
<thead>
<tr>
<th>A_3</th>
<th>A_2</th>
<th>A_1</th>
<th>A_0</th>
<th>Y_3</th>
<th>Y_2</th>
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Simplified Priority Circuit

- **Priority Circuit**
  - Inputs: “Requestors” with priority levels
  - Outputs: “Grant” signal for each requestor
  - Example 4-bit priority circuit

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<th>$A_3$</th>
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**Figure 2.29** Priority circuit truth table with don’t cares (X’s)

$X$ (Don’t Care) means *I don’t care what the value of this input is*
Logic Simplification:
Karnaugh Maps (K-Maps)
Karnaugh Maps are Fun…

- A pictorial way of minimizing circuits by visualizing opportunities for simplification
- They are for you to **study on your own**…

- See backup slides
- Read H&H Section 2.7
- Watch videos of Lectures 5 and 6 from 2019 DDCA course:
  - [https://youtu.be/0ks0PeaOUjE?list=PL5Q2soXY2Zi8J58xLKBGFQFHRO3GrXxA9&t=4570](https://youtu.be/0ks0PeaOUjE?list=PL5Q2soXY2Zi8J58xLKBGFQFHRO3GrXxA9&t=4570)
  - [https://youtu.be/ozs18ARN6s?list=PL5Q2soXY2Zi8J58xLKBFQFHRO3GrXxA9&t=220](https://youtu.be/ozs18ARN6s?list=PL5Q2soXY2Zi8J58xLKBFQFHRO3GrXxA9&t=220)
We Are Done with This

- Building blocks of modern computers
  - Transistors
  - Logic gates

- Combinational circuits

- Boolean algebra

- How to use Boolean algebra to represent combinational circuits

- Minimizing logic circuits
Agenda for Today and Next Week

**Today**
- Start (and finish) Sequential Logic

**Next week**
- Hardware Description Languages and Verilog
  - Combinational Logic
  - Sequential Logic
- Timing and Verification
Extra Credit Assignment: Due March 15

- **Attend and watch Sean Lie’s talk on Feb 28**
  - Either on Zoom or Youtube
  - [https://www.youtube.com/watch?v=x2-qB0J7KHw](https://www.youtube.com/watch?v=x2-qB0J7KHw)

- **Optional Assignment – for 1% extra credit**
  - **Write and submit a 1-page summary** of the talk
    - What are the key ideas used in the Cerebras system?
    - What are your key takeaways from the talk?
    - What did you learn?
    - What did you like or dislike?
Assignment: Lecture Video (April 1)

- Why study computer architecture? Why is it important?
- Future Computing Platforms: Challenges & Opportunities

Required Assignment
- Watch one of Prof. Mutlu’s lectures and analyze either (or both)
  - https://www.youtube.com/watch?v=kgiZlSOcGFM (May 2017)
  - https://www.youtube.com/watch?v=mskTeNnf-i0 (Feb 2021)

Optional Assignment – for 1% extra credit
- Write a 1-page summary of one of the lectures and email us
  - What are your key takeaways?
  - What did you learn?
  - What did you like or dislike?
- Submit your summary to Moodle by April 1
Extra Assignment: Moore’s Law (I)

- **Paper review**

**Optional Assignment – for 1% extra credit**
- Write a 1-page review
- Upload PDF file to Moodle – Deadline: April 7

I strongly recommend that you follow my guidelines for (paper) review (see next slide)
Extra Assignment 2: Moore’s Law (II)

- **Guidelines on how to review papers critically**

  - **Guideline slides:** pdf ppt
  - **Video:** [https://www.youtube.com/watch?v=tOL6FANAJ8c](https://www.youtube.com/watch?v=tOL6FANAJ8c)

  - Example reviews on “Main Memory Scaling: Challenges and Solution Directions” ([link to the paper](https://example.com))
    - Review 1
    - Review 2

  - Example review on “Staged memory scheduling: Achieving high performance and scalability in heterogeneous systems” ([link to the paper](https://example.com))
    - Review 1
A 5-Minute Video on Transistor Innovation

https://www.youtube.com/watch?v=Z7M8etXUEUU
Enabling Manufacturing Tech: EUV

https://www.youtube.com/watch?v=Jv40Viz-KTc
Assignment: Required Readings

- Combinational Logic
  - P&P Chapter 3 until 3.3  +  H&H Chapter 2

- Sequential Logic
  - P&P Chapter 3.4 until end  +  H&H Chapter 3 in full

- Hardware Description Languages and Verilog
  - H&H Chapter 4 in full

- Timing and Verification
  - H&H Chapters 2.9 and 3.5 + (start Chapter 5)

By the end of next week, make sure you are done with
  - P&P Chapters 1-3  +  H&H Chapters 1-4
Required Readings (for Next Week)

- Hardware Description Languages and Verilog
  - H&H Chapter 4 in full

- Timing and Verification
  - H&H Chapters 2.9 and 3.5 + (start Chapter 5)

- By tomorrow, make sure you are done with
  - P&P Chapters 1-3 + H&H Chapters 1-4
Required Readings (for Next Next Week)

- Von Neumann Model, LC-3, and MIPS
  - P&P, Chapters 4, 5
  - H&H, Chapter 6
  - P&P, Appendices A and C (ISA and microarchitecture of LC-3)
  - H&H, Appendix B (MIPS instructions)

- Programming
  - P&P, Chapter 6

- Recommended: Digital Building Blocks
  - H&H, Chapter 5
Sequential Logic Circuits and Design
What We Will Learn Today

- Circuits that can store information
  - Cross-coupled inverter
  - R-S Latch
  - Gated D Latch
  - D Flip-Flop
  - Register

- Finite State Machines (FSM)
  - Moore Machine
  - Mealy Machine

- Verilog implementations of sequential circuits (next week)
Circuits that Can Store Information
Introduction

- Combinational circuit output depends **only** on current input
- We want circuits that produce output depending on **current** and **past** input values – circuits with **memory**
- How can we design a circuit that **stores information**?

![Diagram](image_url)
Capturing Data
Basic Element: Cross-Coupled Inverters

- Has two stable states: Q=1 or Q=0.
- Has a third possible "metastable" state with both outputs oscillating between 0 and 1 (we will see this later)
- Not useful without a control mechanism for setting Q

More Realistic Storage Elements

- **Have a control mechanism for setting Q**
  - We will see the R-S latch soon
  - Let’s look at an SRAM (static random access memory) cell first

![SRAM cell diagram]

- We will get back to SRAM (and DRAM) later
The Big Picture: Storage Elements

- **Latches and Flip-Flops**
  - Very fast, parallel access
  - Very expensive (one bit costs tens of transistors)

- **Static RAM (SRAM)**
  - Relatively fast, only one data word at a time
  - Expensive (one bit costs 6+ transistors)

- **Dynamic RAM (DRAM)**
  - Slower, one data word at a time, reading destroys content (refresh), needs special process for manufacturing
  - Cheap (one bit costs only one transistor plus one capacitor)

- **Other storage technology (flash memory, hard disk, tape)**
  - Much slower, access takes a long time, non-volatile
  - Very cheap
Basic Storage Element:
The R-S Latch
The R-S (Reset-Set) Latch

- Cross-coupled **NAND gates**
  - Data is stored at Q (inverse at Q’)
  - S and R are control inputs
    - In *quiescent (idle) state*, both S and R are held at 1
    - S (set): drive S to 0 (keeping R at 1) to change Q to 1
    - R (reset): drive R to 0 (keeping S at 1) to change Q to 0
- S and R should never both be 0 at the same time

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<th>Input</th>
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1. If \( R=S=0 \), \( Q \) and \( Q' \) will both settle to 1, which breaks our invariant that \( Q = !Q' \).

2. If \( S \) and \( R \) transition back to 1 at the same time, \( Q \) and \( Q' \) begin to oscillate between 1 and 0 because their final values depend on each other (metastability).

- This eventually settles depending on variation in the circuits (more metastability to come in Lecture 8).
How do we guarantee correct operation of an R-S Latch?
The Gated D Latch

- How do we guarantee correct operation of an R-S Latch?
  - Add two more NAND gates!

- Q takes the value of D, when write enable (WE) is set to 1
- S and R can never be 0 at the same time!
The Gated D Latch

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
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<td>WE</td>
<td>D</td>
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The Register
How can we use D latches to store more data?
- Use more D latches!
- A single WE signal for all latches for simultaneous writes

Here we have a register, or a structure that stores more than one bit and can be read from and written to

This register holds 4 bits, and its data is referenced as Q[3:0]
How can we use D latches to store more data?
• Use more D latches!
• A single WE signal for all latches for simultaneous writes

Here we have a register, or a structure that stores more than one bit and can be read from and written to

This register holds 4 bits, and its data is referenced as Q[3:0]
Memory
Memory

- Memory is comprised of locations that can be written to or read from. An example memory array with 4 locations:

<table>
<thead>
<tr>
<th>Addr(00):</th>
<th>0100 1001</th>
<th>Addr(01):</th>
<th>0100 1011</th>
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<tbody>
<tr>
<td>Addr(10):</td>
<td>0010 0010</td>
<td>Addr(11):</td>
<td>1100 1001</td>
</tr>
</tbody>
</table>

- Every unique location in memory is indexed with a unique **address**. 4 locations require 2 address bits (log[#locations]).

- **Addressability**: the number of **bits** of information stored in each location. This example: addressability is 8 bits.

- The entire set of **unique locations** in memory is referred to as the **address space**.

- Typical memory is **MUCH** larger (e.g., billions of locations)
Let’s implement a simple memory array with:
- 3-bit addressability & address space size of 2 (total of 6 bits)

1 Bit

6-Bit Memory Array

<table>
<thead>
<tr>
<th>Addr(0)</th>
<th>Bit₂</th>
<th>Bit₁</th>
<th>Bit₀</th>
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<tr>
<td>Addr(1)</td>
<td>Bit₂</td>
<td>Bit₁</td>
<td>Bit₀</td>
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</table>
Reading from Memory

How can we select an address to read?

- Because there are 2 addresses, address size is $\log(2)=1$ bit
How can we select an address to read?
• Because there are 2 addresses, address size is log(2)=1 bit
Reading from Memory

**How can we select an address to read?**

- Because there are 2 addresses, address size is \( \log(2) = 1 \) bit.

![Address Decoder Diagram](image-url)

Addr[0]

Address Decoder

Wordline

D[2]

D[1]

D[0]
How can we select an address to read?

- Because there are 2 addresses, address size is $\log(2)=1$ bit
Recall: Multiplexer (MUX), or Selector

- **Selects** one of the $N$ inputs to connect it to the output
  - based on the value of a $\log_2 N$-bit control input called **select**
- Example: 2-to-1 MUX
Writing to Memory

How can we select an address and write to it?
How can we select an address and write to it?

- Input is indicated with $D_i$
Let’s enable reading and writing to a memory array
A Bigger Memory Array (4 locations X 3 bits)
A Bigger Memory Array (4 locations X 3 bits)

Address Decoder

(together w/ decoder)
Example: Reading Location 3

![Diagram of memory chip reading location 3](image)

Figure 3.21  Reading location 3 in our $2^2$-by-3-bit memory.

The decoder is useful in determining how to interpret a bit pattern

- It could be the address of a location in memory, that the processor intends to read from
- It could be an instruction in the program and the processor needs to decide what action to take (based on instruction opcode)
Recall: A 4-to-1 Multiplexer
Aside: Implementing Logic Functions Using Memory
Recall: A Bigger Memory Array (4 locations X 3 bits)
Memory-Based Lookup Table Example

- Memory arrays can also perform Boolean Logic functions
  - $2^N$-location $M$-bit memory can perform any $N$-input, $M$-output function
  - Lookup Table (LUT): Memory array used to perform logic functions
  - Each address: row in truth table; each data bit: corresponding output value

![Truth Table and 4-word x 1-bit Array Diagram](image)

**Figure 5.52** 4-word × 1-bit memory array used as a lookup table
Lookup Tables (LUTs)

- LUTs are commonly used in FPGAs
  - To enable programmable/reconfigurable logic functions
  - To enable easy integration of combinational and sequential logic

<table>
<thead>
<tr>
<th>(A)</th>
<th>(B)</th>
<th>(C)</th>
<th>data 4</th>
<th>LUT output</th>
</tr>
</thead>
<tbody>
<tr>
<td>data 1</td>
<td>data 2</td>
<td>data 3</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>1</td>
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<tr>
<td>0</td>
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<td>X</td>
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<tr>
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<td>1</td>
<td>X</td>
<td>0</td>
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<tr>
<td>1</td>
<td>0</td>
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<td>X</td>
<td>0</td>
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<tr>
<td>1</td>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 5.59 LE configuration for two functions of up to four inputs each

Read H&H Chapter 5.6.2
Sequential Logic Circuits
Sequential Logic Circuits

- We have examined designs of circuit elements that can **store information**
- Now, we will use these elements to build circuits that **remember** past inputs

**Combinational**
Only depends on current inputs

**Sequential**
Opens depending on past inputs

https://www.easykeys.com/228_ESP_Combination_Lock.aspx
https://www.fosmon.com/product/tsa-approved-lock-4-dial-combo
State

- In order for this lock to work, it has to keep track (remember) of the past events!
- If passcode is **R13-L22-R3**, sequence of **states** to unlock:
  A. The lock is not open (locked), and no relevant operations have been performed
  B. Locked but user has completed R13
  C. Locked but user has completed R13-L22
  D. Unlocked: user has completed R13-L22-R3

- The **state** of a system is a snapshot of all relevant elements of the system at the moment of the snapshot
  - To open the lock, **states A-D must be completed in order**
  - If anything else happens (e.g., L5), lock **returns** to state A
State Diagram of Our Sequential Lock

- Completely describes the operation of the sequential lock

- We will understand “state diagrams” fully later today
Asynchronous vs. Synchronous State Changes

- Sequential lock we saw is an asynchronous “machine”
  - State transitions occur when they occur
  - There is nothing that synchronizes when each state transition must occur

- Most modern computers are synchronous “machines”
  - State transitions take place after fixed units of time
  - Controlled in part by a clock, as we will see soon

- These are two different design paradigms, with tradeoffs
  - Synchronous control can be easier to get correct when the system consists of many components and many states
  - Asynchronous control can be more efficient (no clock overheads)
Another Simple Example of State

- A standard Swiss traffic light has 4 states
  A. Green
  B. Yellow
  C. Red
  D. Red and Yellow

- The sequence of these states are always as follows
When should the light change from one state to another?

We need a **clock** to dictate when to change state

- Clock signal alternates between 0 & 1

![Clock signal diagram]
Changing State: The Notion of Clock (I)

- When should the light change from one state to another?
- We need a **clock** to dictate when to change state
  - Clock signal alternates between 0 & 1
    
    \[
    \text{CLK: } 1 \quad 0 \quad 1 \quad 0 \quad 1 \quad 0 \quad 1 \quad 0 \quad 1 \quad 0
    \]

- At the start of a clock cycle (\[
\text{□□□□□□□□□□□□□□}
\]), system state changes
  - During a clock cycle, the state stays constant
  - In this traffic light example, we are assuming the traffic light stays in each state an equal amount of time
Clock is a general mechanism that triggers transition from one state to another in a (synchronous) sequential circuit.

Clock synchronizes state changes across many sequential circuit elements.

Combinational logic evaluates for the length of the clock cycle.

Clock cycle should be chosen to accommodate maximum combinational circuit delay.

More on this later, when we discuss timing (Lecture 8).
Asynchronous vs. Synchronous State Changes

- Sequential lock we saw is an asynchronous “machine”
  - State transitions occur when they occur
  - There is nothing that synchronizes when each state transition must occur

- Most modern computers are synchronous “machines”
  - State transitions take place after fixed units of time
  - Controlled in part by a clock, as we will see soon

- These are two different design paradigms, with tradeoffs
  - Synchronous control can be easier to get correct when the system consists of many components and many states
  - Asynchronous control can be more efficient (no clock overheads)

We will assume synchronous systems in the rest of this course
Finite State Machines
What is a **Finite State Machine** (FSM)?

- A discrete-time model of a stateful system
- Each state represents a snapshot of the system at a given time

An FSM pictorially shows

1. the set of all possible **states** that a system can be in
2. how the system transitions from one state to another

An FSM can model

- A traffic light, an elevator, fan speed, a microprocessor, etc.

An FSM enables us to pictorially think of a stateful system using simple diagrams
Finite State Machines (FSMs) Consist of:

**Five elements:**

1. A *finite* number of states
   - *State*: snapshot of all relevant elements of the system at the time of the snapshot
2. A *finite* number of external inputs
3. A *finite* number of external outputs
4. An explicit specification of all state transitions
   - How to get from one state to another
5. An explicit specification of what determines each external output value
Finite State Machines (FSMs)

Each FSM consists of three separate parts:
- next state logic
- state register
- output logic

At the beginning of the clock cycle, next state is latched into the state register.
Finite State Machines (FSMs) Consist of:

- **Sequential Circuits**
  - State register(s)
    - Store the current state and
    - Load the next state at the clock edge

- **Combinational Circuits**
  - Next state logic
    - Determines what the next state will be
  - Output logic
    - Generates the outputs
Finite State Machines (FSMs) Consist of:

- **Sequential circuits**
  - State register(s)
    - Store the current state and
    - Load the next state at the clock edge

- **Combinational Circuits**
  - Next state logic
    - Determines what the next state will be
  - Output logic
    - Generates the outputs
State Register Implementation

- How can we implement a state register? Two properties:
  1. We need to store data at the beginning of every clock cycle
  2. The data must be available during the entire clock cycle
The Problem with Latches

Currently, we cannot simply wire a clock to WE of a latch
- Whenever the clock is high, the latch propagates D to Q
- The latch is transparent

Recall the Gated D Latch

CLK = WE

D ----> WE ----> Q

CLK: 1 0

Register Input:

Register Output:
Currently, we cannot simply wire a clock to WE of a latch

- Whenever the clock is high, the latch propagates D to Q
- The latch is transparent

Recall the Gated D Latch

CLK = WE

Undesirable!
Currently, we cannot simply wire a clock to WE of a latch. When the clock is high, Q will not take on D’s value AND when the clock is low, the latch will propagate D to Q.

The Problem with Latches

Recall the Gated D Latch

CLK = WE

D

Q

How can we change the latch, so that

1) D (input) is **observable** at Q (output) only at the **beginning of next** clock cycle?

2) Q is **available for the full clock cycle**
The Need for a New Storage Element

- To design viable FSMs
- We need storage elements that allow us
  - to read the current state throughout the current clock cycle
  - not write the next state values into the storage elements until the beginning of the next clock cycle.
The D Flip-Flop

- 1) state change on clock edge, 2) data available for full cycle

When the clock is low, master propagates D to the input of slave (Q unchanged)

Only when the clock is high, slave latches D (Q stores D)
- At the rising edge of clock (clock going from 0->1), Q gets assigned D
The D Flip-Flop

1) state change on clock edge, 2) data available for full cycle

- At the rising edge of clock (clock going from 0->1), \( Q \) gets assigned \( D \)
- At all other times, \( Q \) is unchanged
The D Flip-Flop

- 1) state change on clock edge, 2) data available for full cycle

- At the rising edge of clock (clock going from 0->1), Q gets assigned D
- At all other times, Q is unchanged

We can use the D Flip-Flop to implement the state register
Rising-Clock-Edge Triggered Flip-Flop

- **Two inputs**: CLK, D

- **Function**
  - The flip-flop “samples” D on the rising edge of CLK (positive edge)
  - When CLK rises from 0 to 1, D passes through to Q
  - Otherwise, Q holds its previous value
  - Q changes **only** on the rising edge of CLK

- A flip-flop is called an **edge-triggered state element** because it captures data on the clock edge
  - A latch is a **level-triggered** state element
D Flip-Flop Based Register

- Multiple parallel D flip-flops, each of which storing 1 bit

This register stores 4 bits

This line represents 4 wires

Condensed
A 4-Bit D-Flip-Flop-Based Register (Internally)

Finite State Machines (FSMs)

- Next state is determined by the current state and the inputs
- Two types of finite state machines differ in the output logic:
  - **Moore FSM**: outputs depend only on the current state
Finite State Machines (FSMs)

- Next state is determined by the current state and the inputs.
- Two types of finite state machines differ in the output logic:
  - **Moore FSM**: outputs depend only on the current state.
  - **Mealy FSM**: outputs depend on the current state and the inputs.
Finite State Machine Example

- “Smart” traffic light controller
  - **2 inputs:**
    - Traffic sensors: $T_A$, $T_B$ (TRUE when there’s traffic)
  - **2 outputs:**
    - Lights: $L_A$, $L_B$ (Red, Yellow, Green)
  - State can change every 5 seconds
    - Except if green and traffic, stay green

From H&H Section 3.4.1
**Finite State Machine Black Box**

- **Inputs:** CLK, Reset, $T_A$, $T_B$
- **Outputs:** $L_A$, $L_B$
**Moore FSM**: outputs labeled in each state

- **States**: Circles
- **Transitions**: Arcs
**Moore FSM:** outputs labeled in each state
- **States:** Circles
- **Transitions:** Arcs

- **S0**
  - $L_A$: green
  - $L_B$: red
  - Transitions:
    - $T_A$
  - Paths:
    - Academc -> Labs
    - Bravado -> Blvd.
    - Dinner Hall

- **S1**
  - $L_A$: yellow
  - $L_B$: red
  - Transitions:
    - $T_A$
  - Paths:
    - Academc -> Labs
    - Bravado -> Blvd.
    - Dinner Hall
Finite State Machine Transition Diagram

- **Moore FSM**: outputs labeled in each state
  - **States**: Circles
  - **Transitions**: Arcs

![Diagram of a Moore FSM](image-url)

- **States**: Circles
- **Transitions**: Arcs
- **Academic Ave.**
- **Bravado Blvd.**
- **Dining Hall**
- **Labs**
- **Dorms**
- **Fields**

- **States S0**: $L_A$: green, $L_B$: red
- **States S1**: $L_A$: yellow, $L_B$: red
- **States S2**: $L_A$: red, $L_B$: green

- **Transitions**: $T_A$, $T_B$, Reset

- **Labels**: $L_A$, $L_B$
Finite State Machine Transition Diagram

- **Moore FSM**: outputs labeled in each state
  - **States**: Circles
  - **Transitions**: Arcs

```
<table>
<thead>
<tr>
<th>Location</th>
<th>States</th>
<th>Transitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>L_A</td>
<td>S0</td>
<td>T_A</td>
</tr>
<tr>
<td>L_B</td>
<td>S1</td>
<td>T_A</td>
</tr>
<tr>
<td>S2</td>
<td>L_A</td>
<td>T_B</td>
</tr>
<tr>
<td>S3</td>
<td>L_B</td>
<td>T_B</td>
</tr>
<tr>
<td>Bravado</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dining Hall</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Labs</td>
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<tr>
<td>Dorms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Academic</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ave.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Labs Blvd.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fields</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

- **S0**: L_A: green, L_B: red
- **S1**: L_A: yellow, L_B: red
- **S2**: L_A: red, L_B: green
- **S3**: L_A: red, L_B: yellow

**Reset**

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Finite State Machine Transition Diagram

- **Moore FSM**: outputs labeled in each state
  - **States**: Circles
  - **Transitions**: Arrows

The diagram shows the transitions between different states labeled with specific outputs. The states and transitions are labeled with arrows indicating the direction of movement.

- **S0**
  - $L_A$: green
  - $L_B$: red

- **S1**
  - $L_A$: yellow
  - $L_B$: red

- **S2**
  - $L_A$: red
  - $L_B$: green

- **S3**
  - $L_A$: red
  - $L_B$: yellow

The diagram includes labels for academic and dormitory areas, as well as streets like Academic Ave., Bravado Blvd., Labs, and Fields.
Finite State Machine:
State Transition Table
### FSM State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Inputs</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>S0</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>S1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>S2</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>S2</td>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>S3</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**Diagram:**
- **S0**
  - $L_A$: green
  - $L_B$: red
  - Transition on $T_A$ to $S1$
- **S1**
  - $L_A$: yellow
  - $L_B$: red
  - Transition on $T_A$ to $S2$
- **S2**
  - $L_A$: red
  - $L_B$: green
  - Transition on $T_B$ to $S3$
- **S3**
  - $L_A$: red
  - $L_B$: yellow
  - Transition on $T_B$ to $S0$

**Notes:**
- $L_A$: lights in $A$ are green, red, or yellow.
- $L_B$: lights in $B$ are red, or green.
## FSM State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Inputs</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>0</td>
<td>S1</td>
</tr>
<tr>
<td>S0</td>
<td>1</td>
<td>S0</td>
</tr>
<tr>
<td>S1</td>
<td>X</td>
<td>S2</td>
</tr>
<tr>
<td>S2</td>
<td>X</td>
<td>S3</td>
</tr>
<tr>
<td>S2</td>
<td>1</td>
<td>S2</td>
</tr>
<tr>
<td>S3</td>
<td>X</td>
<td>S0</td>
</tr>
</tbody>
</table>

**Diagram:**

- **S0**: \( L_A: \text{green} \), \( L_B: \text{red} \)
- **S1**: \( L_A: \text{yellow} \), \( L_B: \text{red} \)
- **S2**: \( L_A: \text{red} \), \( L_B: \text{green} \)
- **S3**: \( L_A: \text{red} \), \( L_B: \text{yellow} \)

**Inputs:**

- \( T_A \)
- \( T_B \)

**Legend:**

- \( T_A \): green
- \( T_B \): red
- \( \overline{T_A} \): yellow
- \( \overline{T_B} \): green

**Reset**

- From S0 to S0
- From S1 to S1
- From S2 to S2
- From S3 to S3
FSM State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Inputs</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>X</td>
<td>S1</td>
</tr>
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<td>S1</td>
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<td>S2</td>
</tr>
<tr>
<td>S3</td>
<td>X</td>
<td>S0</td>
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</table>

State Encoding

<table>
<thead>
<tr>
<th>State</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>00</td>
</tr>
<tr>
<td>S1</td>
<td>01</td>
</tr>
<tr>
<td>S2</td>
<td>10</td>
</tr>
<tr>
<td>S3</td>
<td>11</td>
</tr>
</tbody>
</table>
### FSM State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Inputs</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S_1 )</td>
<td>( S_0 )</td>
<td>( T_A )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>State</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>00</td>
</tr>
<tr>
<td>S1</td>
<td>01</td>
</tr>
<tr>
<td>S2</td>
<td>10</td>
</tr>
<tr>
<td>S3</td>
<td>11</td>
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</table>
## FSM State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Inputs</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$S_1$</td>
<td>$S_0$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>X</td>
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<tr>
<td>1</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>

### State Encoding

<table>
<thead>
<tr>
<th>State</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>00</td>
</tr>
<tr>
<td>S1</td>
<td>01</td>
</tr>
<tr>
<td>S2</td>
<td>10</td>
</tr>
<tr>
<td>S3</td>
<td>11</td>
</tr>
</tbody>
</table>

$S'_1 = ?$
## FSM State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Inputs</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>S0</td>
<td>T_A</td>
</tr>
<tr>
<td>0</td>
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<td>0</td>
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<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>

\[ S'_1 = (\overline{S}_1 \cdot S_0) + (S_1 \cdot \overline{S}_0 \cdot T_B) + (S_1 \cdot S_0 \cdot T_B) \]

### State Encoding

<table>
<thead>
<tr>
<th>State</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>00</td>
</tr>
<tr>
<td>S1</td>
<td>01</td>
</tr>
<tr>
<td>S2</td>
<td>10</td>
</tr>
<tr>
<td>S3</td>
<td>11</td>
</tr>
</tbody>
</table>
FSM State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Inputs</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$S_1$</td>
<td>$S_0$</td>
<td>$T_A$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>

$S'_1 = (\overline{S}_1 \cdot S_0) + (S_1 \cdot \overline{S}_0 \cdot T_B) + (S_1 \cdot S_0 \cdot T_B)$

$S'_0 = \ ?$
### FSM State Transition Table

#### Diagram

- **S0**
  - $L_A$: green
  - $L_B$: red
- **S1**
  - $L_A$: yellow
  - $L_B$: red
- **S2**
  - $L_A$: red
  - $L_B$: green
- **S3**
  - $L_A$: red
  - $L_B$: yellow

#### Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Inputs</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>$S_0$</td>
<td>$T_A$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>

#### Equations

\[
S'_1 = (\overline{S_1} \cdot S_0) + (S_1 \cdot \overline{S_0} \cdot T_B) + (S_1 \cdot S_0 \cdot T_B)
\]

\[
S'_0 = (\overline{S_1} \cdot \overline{S_0} \cdot \overline{T_A}) + (S_1 \cdot \overline{S_0} \cdot \overline{T_B})
\]

#### State Encoding

<table>
<thead>
<tr>
<th>State</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>00</td>
</tr>
<tr>
<td>S1</td>
<td>01</td>
</tr>
<tr>
<td>S2</td>
<td>10</td>
</tr>
<tr>
<td>S3</td>
<td>11</td>
</tr>
</tbody>
</table>
FSM State Transition Table

Current State | Inputs | Next State
---|---|---
S1 | S0 | TA | TB | S’1 | S’0
0 | 0 | 0 | X | 0 | 1
0 | 0 | 1 | X | 0 | 0
0 | 1 | X | X | 1 | 0
1 | 0 | X | 0 | 1 | 1
1 | 0 | X | 1 | 1 | 0
1 | 1 | X | X | 0 | 0

\[ S'1 = S1 \text{ xor } S0 \quad \text{(Simplified)} \]

\[ S'0 = (\overline{S1} \cdot \overline{S0} \cdot \overline{TA}) + (S1 \cdot \overline{S0} \cdot \overline{TB}) \]
Finite State Machine:
Output Table
**FSM Output Table**

<table>
<thead>
<tr>
<th>Current State</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>$S_0$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
**FSM Output Table**

Current State | Outputs
---|---
|  | $L_A$ | $L_B$
---|---|---
$S_1$ | 0 | green | red
$S_0$ | 0 | yellow | red
| 1 | red | green
---|---|---
| 1 | red | yellow

Output Encoding

<table>
<thead>
<tr>
<th>Output</th>
<th>Encoding</th>
</tr>
</thead>
</table>
green | 00 |
yellow | 01 |
red | 10 |
FSM Output Table

Current State | Outputs
--- | ---
| $S_1$ | $S_0$ | $L_{A1}$ | $L_{A0}$ | $L_{B1}$ | $L_{B0}$
--- | --- | --- | --- | --- | ---
0 | 0 | 0 | 0 | 1 | 0
0 | 1 | 0 | 1 | 1 | 0
1 | 0 | 1 | 0 | 0 | 0
1 | 1 | 1 | 0 | 0 | 1

Output Encoding

<table>
<thead>
<tr>
<th>Output</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>green</td>
<td>00</td>
</tr>
<tr>
<td>yellow</td>
<td>01</td>
</tr>
<tr>
<td>red</td>
<td>10</td>
</tr>
</tbody>
</table>
### FSM Output Table

**Current State**

<table>
<thead>
<tr>
<th>$S_1$</th>
<th>$S_0$</th>
<th>$L_{A1}$</th>
<th>$L_{A0}$</th>
<th>$L_{B1}$</th>
<th>$L_{B0}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

**Output Encoding**

<table>
<thead>
<tr>
<th>Output</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>green</td>
<td>00</td>
</tr>
<tr>
<td>yellow</td>
<td>01</td>
</tr>
<tr>
<td>red</td>
<td>10</td>
</tr>
</tbody>
</table>

$L_{A1} = S_1$

$L_{A0} = S_1 \cdot S_0$
## FSM Output Table

### Outputs

<table>
<thead>
<tr>
<th>Current State</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S_1 )</td>
<td>( S_0 )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

### Output Encoding

<table>
<thead>
<tr>
<th>Output</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>green</td>
<td>00</td>
</tr>
<tr>
<td>yellow</td>
<td>01</td>
</tr>
<tr>
<td>red</td>
<td>10</td>
</tr>
</tbody>
</table>
### FSM Output Table

**Diagram:**
- **State S0:** $L_A$: green, $L_B$: red
- **State S1:** $L_A$: yellow, $L_B$: red
- **State S2:** $L_A$: red, $L_B$: green
- **State S3:** $L_A$: red, $L_B$: yellow

**Current State Table:**

<table>
<thead>
<tr>
<th>Current State</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>$S_0$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Output Encoding:**

- **green:** 00
- **yellow:** 01
- **red:** 10

**Equations:**
- $L_{A1} = S_1$
- $L_{A0} = \overline{S_1} \cdot S_0$
- $L_{B1} = S_1$
- $L_{B0} = S_1 \cdot S_0$
Finite State Machine:
Schematic
FSM Schematic: State Register
FSM Schematic: State Register

 CLK

 S'₁ S₁

 S'₀ S₀

 reset

 state register
FSM Schematic: Next State Logic

\[ S'_1 = S_1 \text{ xor } S_0 \]

\[ S'_0 = (\overline{S_1} \cdot \overline{S_0} \cdot \overline{T_A}) + (S_1 \cdot \overline{S_0} \cdot \overline{T_B}) \]
FSM Schematic: Output Logic

\[ L_{A1} = S_1 \]
\[ L_{A0} = S_1 \cdot S_0 \]
\[ L_{B1} = \overline{S_1} \]
\[ L_{B0} = S_1 \cdot S_0 \]
FSM Timing Diagram

- CLK
- Reset
- $T_A$
- $T_B$
- $S_1:0$
- $S_0$
- $L_A:0$
- $L_B:0$
- $L_A:1$
- $L_B:1$

Diagram:

- States: S0, S1, S2, S3
- Transitions:
  - From S0 to S1: $T_A$
  - From S1 to S2: $T_B$
  - From S2 to S3: $T_B$
  - From S3 to S0: $T_A$
- Input Signals:
  - $L_A$: yellow
  - $L_B$: red
  - $L_A$: red
  - $L_B$: yellow
  - $L_A$: red
  - $L_B$: yellow
  - $L_A$: red
  - $L_B$: yellow
  - $L_A$: yellow
  - $L_B$: red
- Output Signals:
  - $S_0$ (00)
  - $S_1$ (01)
  - $S_2$ (10)
  - $S_3$ (11)
FSM Timing Diagram

- **S0**
  - $L_A$: yellow
  - $L_B$: red

- **S1**
  - $L_A$: yellow
  - $L_B$: red

- **S2**
  - $L_A$: red
  - $L_B$: green

- **S3**
  - $L_A$: red
  - $L_B$: yellow

**Cycle Diagram**

- **CLK**
- **Reset**
- **$T_A$**
- **$T_B$**
- **$S'_{1:0}$**
- **$S_{1:0}$**
- **$L_{A1:0}$**
- **$L_{B1:0}$**

**Time (sec):**

- 0 to 5

**Legend:**
- Green (00)
- Red (10)
- Yellow (01)
FSM Timing Diagram

CLK
Reset
T_A
T_B
S'_1:0
S_1:0
L_A1:0
L_B1:0

Cycle 1
0 5 10
Cycle 2

S0
L_A: yellow
L_B: red

S1
L_A: yellow
L_B: red

S2
L_A: red
L_B: green

S3
L_A: red
L_B: yellow

T_A
T_B

Reset

S0 (00)
S1 (01)
S2 (10)
S3 (11)

Green (00)
Red (10)
FSM Timing Diagram

- **Cycle 1**: Start at state S0, L_A: yellow, L_B: red. L_A: yellow, L_B: red.
- **Cycle 2**: Transition to state S1, L_A: yellow, L_B: red. L_A: yellow, L_B: red.
- **Cycle 3**: Transition to state S2, L_A: red, L_B: green. L_A: red, L_B: green.
- **Cycle 4**: Transition to state S3, L_A: red, L_B: yellow. L_A: red, L_B: yellow.
- **Cycle 5**: Loop back to state S0, L_A: yellow, L_B: red. L_A: yellow, L_B: red.

- **Clock (CLK)**: Input signal.
- **Reset**: Initial state.
- **T_A**: Transition time A.
- **T_B**: Transition time B.
- **S': 1:0**, **S 1:0**, **L_A1:0**, **L_B1:0**: State and output signals.

- **State Changes**:
  - S0 → S1 → S2 → S3 → S0
  - L_A: yellow → red, L_B: red → green → red.

- **Time Axis (t (sec))**:
  - 0, 5, 10, 15 seconds.

- **Outputs**:
  - L_A: yellow, L_B: red, green, and red.
  - L_B: yellow, red, and green.
FSM Timing Diagram

Cycle 1 | Cycle 2 | Cycle 3 | Cycle 4 | Cycle 5
---|---|---|---|---
CLK
Reset
\( T_A \)
\( T_B \)
\( S'_{1:0} \):
?? \( \rightarrow \) S0 (00) \( \rightarrow \) S1 (01) \( \rightarrow \) S2
\( S_{1:0} \):
?? \( \rightarrow \) S0 (00) \( \rightarrow \) S1 (01)
\( L_{A1:0} \):
?? \( \rightarrow \) Green (00) \( \rightarrow \) Yellow
\( L_{B1:0} \):
?? \( \rightarrow \) Red (10)

Switches:
- \( L_A \): yellow
- \( L_B \): red

States:
- S0: \( L_A \): yellow, \( L_B \): red
- S1: \( L_A \): yellow, \( L_B \): red
- S2: \( L_A \): red, \( L_B \): green
- S3: \( L_A \): red, \( L_B \): yellow

Reset
FSM Timing Diagram

![ FSM Timing Diagram ]

- **S0**: L\_A: yellow, L\_B: red
- **S1**: L\_A: yellow, L\_B: red
- **S2**: L\_A: red, L\_B: green
- **S3**: L\_A: red, L\_B: yellow

- **CLK**
- **Reset**
- **T\_A**
- **T\_B**

### Cycle 1
- S\_1:0 -> S0 (00)
- L\_A: yellow
- L\_B: red

### Cycle 2
- S\_1:0 -> S0 (00)
- L\_A: yellow
- L\_B: red

### Cycle 3
- S\_1:0 -> S0 (00)
- L\_A: yellow
- L\_B: red

### Cycle 4
- S\_1:0 -> S1 (01)
- L\_A: red
- L\_B: yellow

### Cycle 5
- S\_1:0 -> S1 (01)
- L\_A: red
- L\_B: yellow

### Cycle 6
- S\_1:0 -> S2 (10)
- L\_A: red
- L\_B: green

### Cycle 7
- S\_1:0 -> S3 (11)
- L\_A: red
- L\_B: yellow

**Timings**

- t (sec): 0, 5, 10, 15, 20, 25, 30, 35, 40, 45

- Green (00)
- Red (10)
- Yellow (01)
This is from H&H Section 3.4.1
FSM Timing Diagram

CLK

Reset

T_A

T_B

S0

L_A: yellow
L_B: red

S1

L_A: yellow
L_B: red

S2

L_A: red
L_B: green

S3

L_A: red
L_B: yellow

S0

S1

S2

S3

S'_{1:0}

??

S0 (00)

??

S0 (00)

??

S0 (00)

??

Green (00)

??

Red (10)

??

Green (00)

??

Red (10)

 Cycle 1 | Cycle 2 | Cycle 3 | Cycle 4 | Cycle 5 | Cycle 6 | Cycle 7 | Cycle 8 | Cycle 9

0 0 5 0 10 0 15 0 20 0 25 0 30 0 35 0 40 0 4

Green (00) Yellow (01) Red (10)

Green (00) Yellow (01) Red (10)

Green (00) Yellow (01) Red (10)
FSM Timing Diagram

See H&H Chapter 3.4

Cycle 1  Cycle 2  Cycle 3  Cycle 4  Cycle 5  Cycle 6  Cycle 7  Cycle 8  Cycle 9  Cycle 10

CLK

Reset

T_A

T_B

S'_{1:0} ?? S0 (00) S1 (01) S2 (10) S3 (11) S0 (00) S1 (01)

S_{1:0} ?? S0 (00) S1 (01) S2 (10) S3 (11) S0 (00)

L_{A1:0} ?? Green (00) Yellow (01) Red (10) Green (00)

L_{B1:0} ?? Red (10) Green (00) Yellow (01) Red (10)

t (sec) 0 5 10 15 20 25 30 35 40 45

Reset

T_A

T_B
Finite State Machine: State Encoding
FSM State Encoding

- How do we encode the state bits?
  - Three common state binary encodings with different tradeoffs
    1. Fully Encoded
    2. 1-Hot Encoded
    3. Output Encoded

- Let’s see an example Swiss traffic light with 4 states
  - Green, Yellow, Red, Yellow+Red
1. **Binary Encoding (Full Encoding):**
   - Use the minimum possible number of bits
     - Use $\log_2(\text{num\_states})$ bits to represent the states
   - *Example state encodings:* 00, 01, 10, 11
   - *Minimizes* # flip-flops, but not necessarily output logic or next state logic

2. **One-Hot Encoding:**
   - Each bit encodes a different state
     - Uses $\text{num\_states}$ bits to represent the states
     - Exactly 1 bit is “hot” for a given state
   - *Example state encodings:* 0001, 0010, 0100, 1000
   - *Simplest design process* – very automatable
   - *Maximizes* # flip-flops, *minimizes* next state logic
3. Output Encoding:
   - Outputs are **directly accessible** in the state encoding.
   - For example, since we have **3 outputs** (light color), encode state with **3 bits**, where each bit represents a color.
     - *Example states*: 001, 010, 100, 110
       - $\text{Bit}_0$ encodes **green** light output,
       - $\text{Bit}_1$ encodes **yellow** light output
       - $\text{Bit}_2$ encodes **red** light output
   - **Minimizes** output logic
   - Only works for Moore Machines (output function of state)
3. Output Encoding:

- Outputs are **directly accessible** in the state encoding.

The **designer** must **carefully** choose an encoding scheme to **optimize** the design under given constraints.

- Minimizes output logic
- Only works for Moore Machines (output function of state)
Moore vs. Mealy Machines
Recall: Moore vs. Mealy FSMs

- Next state is determined by the current state and the inputs
- Two types of FSMs differ in the **output logic**:
  - **Moore FSM**: outputs depend only on the current state
  - **Mealy FSM**: outputs depend on the current state and the inputs
Alyssa P. Hacker has a snail that crawls down a paper tape with 1’s and 0’s on it.

The snail smiles whenever the last four digits it has crawled over are 1101.

Design Moore and Mealy FSMs of the snail’s brain.
Moore vs. Mealy FSM Examples

- Alyssa P. Hacker has a snail that crawls down a paper tape with 1’s and 0’s on it.
- The snail smiles whenever the last four digits it has crawled over are 1101.
- Design Moore and Mealy FSMs of the snail’s brain.
State Transition Diagrams

Moore FSM

Mealy FSM

What are the tradeoffs?
**FSM Design Procedure**

- **Determine** all possible states of your machine
- **Develop** a *state transition diagram*
  - Generally this is done from a textual description
  - You need to 1) determine the *inputs* and *outputs* for each *state* and 2) figure out how to get from one state to another

- **Approach**
  - Start by defining the *reset state* and what happens from it – this is typically an easy point to start from
  - Then continue to add *transitions* and *states*
  - Picking *good state names* is very important
  - Building an FSM is *like* programming (but it *is not* programming!)
    - An FSM has a sequential “control-flow” like a program with conditionals and goto’s
    - The if-then-else construct is controlled by one or more inputs
    - The outputs are controlled by the state or the inputs
  - In hardware, we typically have many concurrent FSMs
What is to Come: LC-3 Processor

Figure 4.3 The LC-3 as an example of the von Neumann model
What is to Come: LC-3 Datapath
Digital Design & Computer Arch.

Lecture 6: Sequential Logic Design

Prof. Onur Mutlu

ETH Zürich
Spring 2022
11 March 2022
Backup Slides:
Different Types of Flip Flops
Enabled Flip-Flops

- **Inputs:** CLK, D, EN
  - The enable input (EN) controls when new data (D) is stored
- **Function:**
  - **EN = 1:** D passes through to Q on the clock edge
  - **EN = 0:** the flip-flop retains its previous state

![Internal Circuit Diagram]
Resettable Flip-Flop

- **Inputs**: CLK, D, Reset
  - The Reset is used to set the output to 0.

- **Function**:
  - **Reset = 1**: Q is forced to 0
  - **Reset = 0**: the flip-flop behaves like an ordinary D flip-flop

Symbols

```
  D  Q
  Reset

  r
```
Resettable Flip-Flops

- Two types:
  - **Synchronous**: resets at the clock edge only
  - **Asynchronous**: resets immediately when Reset = 1

- Asynchronously resettable flip-flop requires changing the internal circuitry of the flip-flop (see Exercise 3.10)

- Synchronously resettable flip-flop?
Settable Flip-Flop

- **Inputs:** CLK, D, Set
- **Function:**
  - **Set = 1:** Q is set to 1
  - **Set = 0:** the flip-flop behaves like an ordinary D flip-flop

Symbols

\[
\begin{align*}
\text{Symbols} \\
\begin{array}{c}
\text{D} \\
\text{Q} \\
\text{Set}
\end{array}
\end{align*}
\]
Backup Slides on Karnaugh Maps (K-Maps)
Complex Cases

- One example
  
  \[ Cout = \overline{A}BC + \overline{A}BC + ABC + ABC \]

- Problem
  - Easy to see how to apply Uniting Theorem...
  - Hard to know if you applied it in all the right places...
  - ...especially in a function of many more variables

- Question
  - Is there an easier way to find potential simplifications?
  - i.e., potential applications of Uniting Theorem...?

- Answer
  - Need an intrinsically geometric representation for Boolean \( f( ) \)
  - Something we can draw, see...
Karnaugh Map

- Karnaugh Map (K-map) method
  - K-map is an alternative method of representing the truth table that helps visualize adjacencies in up to 6 dimensions
  - Physical adjacency ↔ Logical adjacency

**Numbering Scheme:** 00, 01, 11, 10 is called a “Gray Code” — only a single bit (variable) changes from one code word and the next code word
Karnaugh Map Methods

K-map adjacencies go “around the edges”
Wrap around from first to last column
Wrap around from top row to bottom row
Strategy for “circling” rectangles on Kmap:

Biggest “oops!” that people forget:

\[ F(A, B, C, D) = \sum m(0, 2, 5, 8, 9, 10, 11, 12, 13, 14, 15) \]

\[ F = A + \overline{B}D + B\overline{C}D \]
Logic Minimization Using K-Maps

- Very simple guideline:
  - Circle all the rectangular blocks of 1’s in the map, using the fewest possible number of circles
    - Each circle should be as large as possible
  - Read off the implicants that were circled

- More formally:
  - A Boolean equation is minimized when it is written as a sum of the fewest number of prime implicants
  - Each circle on the K-map represents an implicant
  - The largest possible circles are prime implicants
K-map Rules

- **What can be legally combined (circled) in the K-map?**
  - Rectangular groups of size $2^k$ for any integer $k$
  - Each cell has the same value (1, for now)
  - All values must be adjacent
    - Wrap-around edge is okay

- **How does a group become a term in an expression?**
  - Determine which literals are constant, and which vary across group
  - Eliminate varying literals, then AND the constant literals
    - constant 1 $\rightarrow$ use $x$, constant 0 $\rightarrow$ use $\overline{x}$

- **What is a good solution?**
  - Biggest groupings $\rightarrow$ eliminate more variables (literals) in each term
  - Fewest groupings $\rightarrow$ fewer terms (gates) all together
  - OR together all AND terms you create from individual groups
K-map Example: Two-bit Comparator

Design Approach:
Write a 4-Variable K-map for each of the 3 output functions

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>F1</th>
<th>F2</th>
<th>F3</th>
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K-map Example: Two-bit Comparator (2)

K-map for $F_1$

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<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
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<tbody>
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</table>

$F_1 = A'B'C'D' + A'BC'D + ABCD + AB'CD'$
K-map Example: Two-bit Comparator (3)

\[ K\text{-map for } F_2 \]

\[
\begin{array}{c|cccc}
A & B & C & D & \text{F2} \\
\hline
0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 1 & 0 & 0 \\
0 & 0 & 1 & 1 & 0 \\
0 & 1 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 & 1 \\
0 & 1 & 1 & 0 & 0 \\
0 & 1 & 1 & 1 & 0 \\
1 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 1 & 0 \\
1 & 0 & 1 & 0 & 1 \\
1 & 0 & 1 & 1 & 0 \\
1 & 1 & 0 & 0 & 0 \\
1 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 \\
1 & 1 & 1 & 1 & 1 \\
\end{array}
\]

\[ F_2 = \] \[ F_3 = \text{? (Exercise for you)} \]
**K-maps with “Don’t Care”**

- **Don’t Care** really means *I don’t care what my circuit outputs if this appears as input*

- You have an engineering choice to use DON’T CARE patterns intelligently as 1 or 0 to better *simplify* the circuit

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>F</th>
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I can pick 00, 01, 10, 11 independently of below

I can pick 00, 01, 10, 11 independently of above
Example: BCD Increment Function

- **BCD (Binary Coded Decimal) digits**
  - Encode decimal digits 0 - 9 with bit patterns $0000_2$ — $1001_2$
  - When *incremented*, the decimal sequence is 0, 1, ..., 8, 9, 0, 1

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These input patterns should never be encountered in practice (hey -- it's a BCD number!)
So, associated output values are “Don’t Cares”
K-map for BCD Increment Function

Z (without don’t cares) =

Z (with don’t cares) =

\[ Z \text{ (without don’t cares)} = A'D' + B'C'D' \]

\[ Z \text{ (with don’t cares)} = D' \]
K-map Summary

- Karnaugh maps as a formal systematic approach for logic simplification

- 2-, 3-, 4-variable K-maps

- K-maps with “Don’t Care” outputs

- H&H Section 2.7