

# Reorder Buffer Example

CAM

RAM

Register File (RF)

R0	
R1	1
R2	2
R3	3
R4	4
R5	5
R6	6
R7	

Value

Tag

Initially: all registers are valid in RF & ROB is empty

Simulate:

MUL R1, R2 → R3

MUL R3, R4 → R11

ADD R5, R6 → R3

ADD R3, R8 → R12

60 cycles

ACB (3)

Reorder Buffer (ROB)

Entry 0	1	3	0	0
Entry 1	1	3	0	0
Entry 2	1	3	0	0
Entry 3	1	3	0	0
Entry 4	1	3	0	0
Entry 5	1	3	0	0
Entry 6	1	3	0	0
Entry 7	1	3	0	0
Entry 8				
Entry 9				
Entry 10				
Entry 11				
Entry 12				
Entry 13				
Entry 14				
Entry 15				

Entry Valid?

Dest reg ID

Dest reg value

Dest reg written?

Oldest instruction

Youngest

Youngest instruction

Register Renaming

- eliminates false dependences