P&S Modern SSDs

NAND Flash Read/Write Operations

Dr. Mohammad Sadrosadati
Prof. Onur Mutlu
ETH Zürich
Fall 2022
19 October 2022
Upcoming EFCL & SAFARI Live Seminar (Oct. 19)

https://www.youtube.com/watch?v=5BRLkCCL-hY
Today’s Agenda

- NAND Flash Page Read/Write
- Sensing Circuitry
Today’s Agenda

- NAND Flash Page Read/Write
- Sensing Circuitry
A Flash Cell

- Basically, it is a transistor
A Flash Cell

- Basically, it is a transistor
  - w/ a special material: Floating gate (2D) or Charge trap (3D)
A Flash Cell

- Basically, it is a transistor
  - w/ a special material: Floating gate (2D) or Charge trap (3D)
  - Can hold electrons in a non-volatile manner

\[
V_{PGM} = 20 \text{ V}
\]

\(G\)  
(Control Gate)

\(FG\)  
(Floating Gate)

\(S\)  
(Source)

\(GND\)  
(Substrate)

\(D\)  
(Home)

\(Tunneling\)

\(V_{TH}\)  
\(V_{GS}\)
A Flash Cell

- Basically, it is a transistor
  - w/ a special material: Floating gate (2D) or Charge trap (3D)
  - Can hold electrons in a non-volatile manner
  - Changes the cell’s threshold voltage ($V_{TH}$)

![Flash Cell Diagram]

- $G$ (Control Gate)
- $GND$
- $S$ (Source)
- $D$ (Drain)
- $FG$ (Floating Gate)
- $V_{TH}$
- $V_{REF}$
- $V_{GS}$
- $20\, V$
- Tunneling
Threshold Voltage Distribution

- $V_{TH}$ distribution of cells in a programmed page/block/chip

- Why distribution? Variations across the cells
  - Some cells are more easily programmed or erased

There are $y$ cells whose $V_{TH} = xV$

# of cells

Threshold voltage ($V_{TH}$)

Erased (E) 1

Programmed 0

$V_{REF}$
**$V_{TH}$ Distribution of MLC NAND Flash**

- Multi-level cell (MLC) technique
  - $2^m V_{TH}$ states required to store $m$ bits in a single flash cell

- Limited width of the $V_{TH}$ window: Need to
  - Make each $V_{TH}$ state narrow
  - Guarantee sufficient margins b/w adjacent $V_{TH}$ states
**$V_{TH}$ Distribution of MLC NAND Flash**

- **Multi-level cell (MLC) technique**
  - $2^m V_{TH}$ states required to store $m$ bits in a single flash cell

- **Limited width** of the $V_{TH}$ window: Need to
  - Make each $V_{TH}$ state narrow
  - Guarantee sufficient margins b/w adjacent $V_{TH}$ states
    - $V_{TH}$ changes over time after programmed
    - Narrower margins $\rightarrow$ Lower reliability
    - More bits per cell $\rightarrow$ higher density but lower reliability

---

![Diagram showing $V_{TH}$ distribution for MLC NAND flash memory with multiple $V_{TH}$ states and margins.](image)

- Error cells
- Shifted & widened after programmed
Basic Operation: Page Program

String Select Line
SSL

Wordline
WL\(_{k-1}\)

Target Page

WL\(_k\)

WL\(_{k+1}\)

Ground Select Line
GSL

Block

BL\(_0\)
BL\(_1\)
BL\(_2\)
BL\(_3\)
BL\(_{132,095}\)
Basic Operation: Page Program

- **WL control** – All other cells operate as a resistance

![Diagram showing WL control](image-url)

**WL control** - All other cells operate as a resistance.

- **String Select Line (SSL)**
- **Wordline (WL)**
- **Ground Select Line (GSL)**

Voltage levels indicated:
- **$V_{CC}$**
- **$V_{PASS}$**
- **$V_{PROG}$**
Basic Operation: Page Program

- **BL control** – **Inhibits cells** to not be programmed

```
/--------------------------
<p>| V_PROG    WL_k          |</p>
<table>
<thead>
<tr>
<th>0   1   0   1       0</th>
</tr>
</thead>
</table>
```

**Program** (0) **inhibit** (1)
Basic Operation: Page Program

- **BL control** – **Inhibits cells** to not be programmed

![Diagram of BL control](attachment:image.png)
Basic Operation: Page Program

Program

Inhibit

$V_{PRoG}$ $WL_k$

To GND

To $V_{CC}$

To GND

To $V_{CC}$

To GND

# of cells

$V_{REF}$

1 Erased (E)

Threshold voltage ($V_{TH}$)

132,095
**Basic Operation: Page Program**

The diagram illustrates the basic operation of a page program using the voltage levels and states of the BL (Bit Line) and WL (Word Line) segments.

- **V<sub>PROG</sub>** and **WL<sub>k</sub>** are the control signals for programming and selecting the word line, respectively.

- The **program** and **inhibit** states are shown on the BL segments:
  - **BL<sub>0</sub>** is in the program state (0), **BL<sub>1</sub>** is in the inhibit state (1), and the rest are in the program state (0).

- The **# of cells** graph shows the distribution of cells in the erased (E) and programmed states.
  - **Erased (E)**: One cell is in the erased state (1).
  - **Programmed**: The rest of the cells are in the programmed state (0).

- The **V<sub>REF</sub>** threshold voltage separates the erased and programmed cells.

- The cells are connected to the **GND** or **V<sub>CC</sub>** power supplies as indicated by the arrows.
Basic Operation: Page Program

To GND  To \( V_{CC} \)  To GND  To \( V_{CC} \)  To GND

# of cells

Threshold voltage (\( V_{TH} \))

<table>
<thead>
<tr>
<th>Erased (E)</th>
<th>Inhibited cells</th>
</tr>
</thead>
</table>

Hard-to-program cells  Easy-to-program cells
Basic Operation: Page Program

- Incremental Step-Pulse Programming (ISPP)

![Diagram of ISPP process]

- **Program** step:
  - WLₙ₀
  - BL₀
  - BL₁
  - BL₂
  - BL₃
  - BL₁₃₂,₀₉₅

- **Inhibit** step:
  - WLₙ₀
  - BL₀
  - BL₁
  - BL₂
  - BL₃
  - BL₁₃₂,₀₉₅

**Verifying program as programmed**

- **Erased (E)**
- **Inhibited cells**
- **Cells to program**

**Threshold voltage (V_{TH})**

**# of cells**

**V_{PROGO}**
Basic Operation: Page Program

- Incremental Step-Pulse Programming (ISPP)

![Diagram showing ISPP process]

- Program
- Inhibit

WL<sub>k</sub>  BL<sub>0</sub>  BL<sub>1</sub>  BL<sub>2</sub>  BL<sub>3</sub>  BL<sub>132,095</sub>

- To GND  To V<sub>CC</sub>  To V<sub>CC</sub>  To V<sub>CC</sub>  To GND

# of cells

Threshold voltage (V<sub>TH</sub>)

- Inhibited cells
- V<sub>REF</sub>
- Cells to program
- Erased (E)

- Inhibited cells

V<sub>REF</sub>

Cells to program

Inhibited cells

V<sub>REF</sub>

Cells to program

Inhibited cells
Basic Operation: Page Program

- Incremental Step-Pulse Programming (ISPP)

![Diagram showing basic operation of page program with labeled components and waveforms.](image)

- **Program**
  - WL<sub>k</sub>, V<sub>PROG</sub>, BL<sub>0</sub>, BL<sub>1</sub>, BL<sub>2</sub>, BL<sub>3</sub>, BL<sub>132,095</sub>

- **Inhibit**
  - To GND, To V<sub>CC</sub>, To V<sub>CC</sub>, To V<sub>CC</sub>

- **Threshold voltage (V<sub>TH</sub>)**
  - Cells to program
  - Erased (E)
  - Inhibited cells

- **Inhibit programmed cells**

- **V<sub>REF</sub>**
Basic Operation: Page Program

- Incremental Step-Pulse Programming (ISPP)

Program:
- $V_{PROG1}$ to $WL_k$

Inhibit:
- BL$^0$ to GND
- BL$^1$ to $V_{cc}$
- BL$^2$ to $V_{cc}$
- BL$^3$ to $V_{cc}$
- BL$^{132,095}$ to GND

- Inhibited cells
- Programmed cells

- Erased (E)
- Programmed

- $V_{REF}$
- Cells to program

Threshold voltage ($V_{TH}$)

# of cells
Basic Operation: Page Read

- WL control – All other cells operate as a resistance

```
<table>
<thead>
<tr>
<th>BL0</th>
<th>BL1</th>
<th>BL2</th>
<th>BL3</th>
<th>BL132,095</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
```

- # of cells
  - Erased (E)
  - Programmed

- Threshold voltage ($V_{TH}$)
- $V_{REF}$
Basic Operation: Page Read

- **BL control** – Charge all BLs

![Diagram showing BL control and voltage levels]

- **V<sub>REF</sub>**
- **WL<sub>k</sub>**
- **To V<sub>cc</sub>**

- **# of cells**
- **1 Erased (E)**
- **0 Programmed**

- **Threshold voltage (V<sub>TH</sub>)**
- **V<sub>REF</sub>**
Basic Operation: Page Read

- Sensing the current through BLs

![Diagram showing the sensing of current through BLs and the relationship between threshold voltage ($V_{TH}$), reference voltage ($V_{REF}$), and the charge state of cells.]

- $V_{REF}$ WL$_k$
- $V_{TH} < V_{REF}$ (Erased (E))
- $V_{TH} > V_{REF}$ (Programmed)

(No current) (Current)
Basic Operation: Page Read - MLC

- Sensing the current through BLs

![Diagram of sensing current through BLs]

- # of cells
- MSB
- LSB
- CSB
- V_{REF0}
- V_{REF1}
- V_{REF2}
- V_{REF3}
- V_{REF4}
- V_{REF5}
- V_{REF6}

V_{TH
Basic Operation: Page Read - MLC

- Sensing the current through BLs

![Diagram showing sensing through BLs and MSB/LSB, with WLk, BL0 to BL132,095, and VREF0 to VREF6 markers.]
Basic Operation: Page Read - MLC

- Sensing the current through BLs

\[ WL_k \]

- BL\(_0\) 111
- BL\(_1\) 000
- BL\(_2\) 101
- BL\(_3\) 001
- BL\(_{132,095}\) 110

# of cells

E P1 P2 P3 P4 P5 P6 P7

V\(_{\text{REF0}}\) V\(_{\text{REF1}}\) V\(_{\text{REF2}}\) V\(_{\text{REF3}}\) V\(_{\text{REF4}}\) V\(_{\text{REF5}}\) V\(_{\text{REF6}}\)
Basic Operation: Page Read - MLC

- Sensing the current through BLs

![Diagram of BLs and WLk connections showing current sensing through BLs](image)

- VTH levels for reference:
  - VREF0
  - VREF1
  - VREF2
  - VREF3
  - VREF4
  - VREF5
  - VREF6

- MSB and LSB markers indicate cell status:
  - MSB 111
  - LSB 110

- Cells E, P1, P2, P3, P4, P5, P6, P7 with corresponding VTH values.
Basic Operation: Page Read - MLC

- Sensing the current through BLs

![Diagram showing the sensing of current through BLs for MLC operation](image-url)
Basic Operation: Page Read - MLC

- Sensing the current through BLs

![Diagram showing sensing the current through BLs](image-url)
Basic Operation: Page Read - MLC

- Sensing the current through BLs

![Diagram showing the sensing process through BLs with various voltage references and cell values.](image)
Basic Operation: Page Read – Takeaways

- Bit-encoding affects the read latency!
  - Compare # of sensing for LSB

<table>
<thead>
<tr>
<th># of cells</th>
<th>V_{REF0}</th>
<th>V_{REF1}</th>
<th>V_{REF2}</th>
<th>V_{REF3}</th>
<th>V_{REF4}</th>
<th>V_{REF5}</th>
<th>V_{REF6}</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>110</td>
<td>100</td>
<td>000</td>
<td>010</td>
<td>011</td>
<td>001</td>
<td>101</td>
</tr>
<tr>
<td>E</td>
<td>P1</td>
<td>P2</td>
<td>P3</td>
<td>P4</td>
<td>P5</td>
<td>P6</td>
<td>P7</td>
</tr>
</tbody>
</table>

![Diagram showing the relationship between bit encoding and read latency](image)

- MSB and LSB notations are illustrated along with the corresponding voltage references (V_{TH}, V_{REF}) for each cell.

33
Basic Operation: Page Read – Takeaways

- Bit-encoding affects the read latency!
  - Compare # of sensing for LSB
Basic Operation: Page Read – Takeaways

- Bit-encoding affects the read latency!
  - Compare # of sensing for LSB
Basic Operation: Page Read – Takeaways

- Bit-encoding affects the read latency!
  - Compare # of sensing for LSB
Today’s Agenda

- NAND Flash Page Read/Write
- Sensing Circuitry
Read Mechanism

- NAND flash read mechanism consists of three steps:
  - 1) Precharge
  - 2) Evaluation
  - 3) Discharge
Enable precharge transistor $M_{PRE}$ to charge all target BLs and their sense-out capacitors ($C_{SO}$) to $V_{PRE}$.
Read Mechanism: Evaluation

1. Precharge
2. Evaluation
3. Discharge
Read Mechanism: Evaluation

Disconnect the BLs from $V_{\text{PRE}}$ and enable the latching circuit.
If $V_{TH} \leq V_{REF}$, the charge in $C_{SO}$ quickly flows through the NAND string (Sensed as 1)
Read Mechanism: Evaluation

If $V_{TH} > V_{REF}$, the target cell blocks the BL discharge current (Sensed as 0)
Bitlines are discharged to return the NAND string to its initial state for future operations.
Before the evaluation step, the chip initializes the latching circuit

- Activating transistor $M_1$
- $V_{\text{OUT}} = 0$
- $V_{out} = 1$
Latching Circuit

- The evaluation step
  - Disables $M_{PRE}$ and $M_1$
  - Enables $M_2$

\[(a) \ V_{TH} \leq V_{REF} \]

\[(b) \ V_{TH} > V_{REF} \]
Inverse Read

- Performing an inverse read by simply changing the activation sequence of $M_1$ and $M_2$
  - The precharge step activates $M_2$
  - The evaluation step disables $M_2$ and activates $M_1$

(a) $V_{TH} \leq V_{REF}$

(b) $V_{TH} > V_{REF}$
Flash-Cosmos: In-Flash Bulk Bitwise Operations Using Inherent Computation Capability of NAND Flash Memory

Jisung Park$^\text{S V}$ Roknoddin Azizi$^\text{S}$ Geraldo F. Oliveira$^\text{S}$ Mohammad Sadrosadati$^\text{S}$
Rakesh Nadig$^\text{S}$ David Novo$^\dagger$ Juan Gómez-Luna$^\text{S}$ Myungsuk Kim$^\ddagger$ Onur Mutlu$^\text{S}$

$^\text{S}$ETH Zürich $^\text{V}$POSTECH $^\dagger$LIRMM, Univ. Montpellier, CNRS $^\ddagger$Kyungpook National University

Required Material

- Yu Cai, Saugata Ghose, Erich F. Haratsch, Yixin Luo, and Onur Mutlu,
  “Errors in Flash-Memory-Based Solid-State Drives: Analysis, Mitigation, and Recovery,” Invited Book Chapter in Inside Solid State Drives, 2018 - Introduction and Section 1

- Jisung Park, Myungsuk Kim, Myoungjun Chun, Lois Orosa, Jihong Kim, and Onur Mutlu,
  “Reducing Solid-State Drive Read Latency by Optimizing Read-Retry,” In ASPLOS, 2021
Recommended Material

- Arash Tavakkol, Mohammad Sadrosadati, Saugata Ghose, Jeremie Kim, Yixin Luo, Yaohua Wang, Nika Mansouri Ghiasi, Lois Orosa, Juan Gómez Luna, and Onur Mutlu, “FLIN: Enabling Fairness and Enhancing Performance in Modern NVMe Solid State Drives,” In ISCA, 2018
P&S Modern SSDs

NAND Flash Read/Write Operations

Dr. Mohammad Sadrosadati
Prof. Onur Mutlu

ETH Zürich
Fall 2022
19 October 2022