P&S DRAM Bender

FPGA-based Exploration of DRAM and RowHammer

Ataberk Olgun
Prof. Onur Mutlu
ETH Zürich
Fall 2023
3 October 2023
P&S DRAM Bender: Content

- We will learn in detail how modern DDR4 DRAM operates

- You will learn how to characterize DRAM using an FPGA-based DRAM characterization infrastructure (DRAM Bender)

- You will use DRAM Bender to develop your own DRAM experiments and gain hand-on experience in studying DRAM characteristics
This P&S is aimed at improving your

- **Knowledge** in Computer Architecture and Memory Systems
- **Technical skills** in running DRAM experiments using real devices
- **Critical thinking and analysis**
- **Familiarity with key research directions**
- **Technical presentation** of your project
- **Communication skills** (by interacting with a group of researchers)
P&S DRAM Bender: Key Goal

(Learn how to) study real memory chips using an FPGA-based DRAM infrastructure to gain new insights on DRAM behavior
Prerequisites of the Course

- Digital Design and Computer Architecture (or equivalent course)

- **Familiarity with a programming language (we will use C++/Python)**
  - You should have basic knowledge of version control (git), remote access (SSH), and be comfortable with Linux command line to make tangible progress in your projects

- Comfortable with discovering why things do or do not work and solving problems

- Interest in low-level hacking and memory

- (Optional) Familiarity with FPGA programming
Course Info: Who Are We? (I)

- **Onur Mutlu**
  - Full Professor @ ETH Zurich ITET (INFK), since September 2015
  - Strecker Professor @ Carnegie Mellon University ECE/CS, 2009-2016, 2016-...
  - PhD from UT-Austin, worked at Google, VMware, Microsoft Research, Intel, AMD
  - [https://people.inf.ethz.ch/omutlu/](https://people.inf.ethz.ch/omutlu/)
  - omutlu@gmail.com (Best way to reach me)
  - [https://people.inf.ethz.ch/omutlu/projects.htm](https://people.inf.ethz.ch/omutlu/projects.htm)

- **Research and Teaching in:**
  - Computer architecture, computer systems, hardware security, bioinformatics
  - Memory and storage systems
  - Hardware security, safety, predictability
  - Fault tolerance
  - Hardware/software cooperation
  - Architectures for bioinformatics, health, medicine
  - ...
Course Info: Who Are We? (II)

- **Lead Supervisor:**
  - Ataberk Olgun

- **Supervisors:**
  - Giray Yaglikci
  - Haocong Luo
  - Yahya Tugrul
  - Banu Cavlak
  - Ismail Yuksel

- **Get to know us and our research**
  - [https://safari.ethz.ch/group-members](https://safari.ethz.ch/group-members)
Onur Mutlu’s SAFARI Research Group

Computer architecture, HW/SW, systems, bioinformatics, security, memory

https://safari.ethz.ch/safari-newsletter-april-2020/

38+ Researchers

Think BIG, Aim HIGH!

https://safari.ethz.ch
Current Research Focus Areas

**Research Focus:** Computer architecture, HW/SW, bioinformatics
- Memory and storage (DRAM, flash, emerging), interconnects
- Heterogeneous & parallel systems, GPUs, systems for data analytics
- System/architecture interaction, new execution models, new interfaces
- Energy efficiency, fault tolerance, hardware security, performance
- Genome sequence analysis & assembly algorithms and architectures
- Biologically inspired systems & system design for bio/medicine

**Broad research spanning apps, systems, logic with architecture at the center**
Course Info: How About You?

- Let us know your background, interests
- Why did you join this P&S?
- Please submit HW0
  - Moodle link in the homework handout
Course Requirements and Expectations

- Attendance required for all (future) meetings
  - Meeting 2 (next week)
  - 1-1 weekly update meetings

- Study the learning materials

- Each student will carry out a hands-on project
  - Build, implement, code, and design with engagement from the supervisors

- Participation
  - Ask questions (to your peers/supervisors), contribute thoughts/ideas
  - Read relevant papers

We will help in all projects!
Course Website

- https://safari.ethz.ch/projects_and_seminars/doku.php?id=softmc

- Useful information about the course

- Check your email frequently for announcements
Meeting 1

- **Required Materials**
  - DRAM Bender Tutorial Video: [https://www.youtube.com/watch?v=FkIvEsfdZCI](https://www.youtube.com/watch?v=FkIvEsfdZCI)
  - DRAM Bender public repository: [https://github.com/CMU-SAFARI/DRAM-Bender](https://github.com/CMU-SAFARI/DRAM-Bender)

- **Recommended Materials**
  - SoftMC lecture: [https://www.youtube.com/watch?v=tnSPEP3t-Ys](https://www.youtube.com/watch?v=tnSPEP3t-Ys)
Meeting 2 (TBD)

- We will announce the projects and will give you some description about them.
- You will have a week to submit your project preferences.
- The supervisors would like to help you with selecting a project that matches your interests, skills, and background.
- It is important that you study the learning materials before our next meeting!
Tentative Weekly Schedule

- Week 0 – DRAM Bender Tutorial
- Week 1 – Logistics & Intro to DRAM and an Overview of DRAM Bender [TCAD’23]
  - Make sure to watch Week 0’s tutorial!
- Week 2 – Available Projects
- Week 3 – Experimental Analysis of RH in HBM2 [DSN’23] | Weekly updates start
- Week 4 – Uncovering in DRAM TRR [MICRO’21] | Weekly update meeting
- Week 5 – RowPress [ISCA’23] | Weekly update meeting
- Week 6 – RH Under Reduced Voltage [DSN’22] | Weekly update meeting
- Week 7 – Hidden Row Activation [MICRO’22] | Weekly update meeting
- Week 8+ Weekly update meetings

Weekly update meeting: All students and supervisor meet together
- Students give an update on their project
Every week: 1-1 meeting(s) with supervisor(s) + weekly update meetings
Performance Assessment

We expect you to:

- **Learn** how DRAM operates and **perform** DRAM characterization using FPGAs
- **Achieve the goals** of your project
- **Deliver** your **code and results** with sufficient documentation
- Prepare a **final presentation** and present your work to SAFARI
An Introduction to
DRAM and DRAM Bender
DRAM Bender
An Extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM Chips

Ataberk Olgun
Yahya Can Tugrul
Minesh Patel
Hasan Hassan
Lois Orosa
Oguz Ergin
A. Giray Yaglikci
Haocong Luo
Onur Mutlu
Accessing a DRAM Cell

wordline

capacitor

access transistor

enable

Sense Amp

bitline

[Seshadri+ MICRO’17]
Accessing a DRAM Cell

1. Enable wordline

2. Connects cell to bitline

3. Cell loses charge to bitline

4. Deviation in bitline voltage

5. Enable sense amp

6. Sense Amp

[Figure showing DRAM cell access process with labels for each step]
DRAM Operation

Wordline Drivers

Cache line

Sense Amplifiers

READ

READ

READ

DRAM Command Sequence

\( t_{RAS} \) (Activation Latency)

\( t_{RP} \) (Precharge Latency)

DRAM Operation

[Kim+ HPCA'19]
Factors Affecting DRAM Reliability and Latency

- DRAM timing violation
- Inter-cell interference
- Manufacturing process
- Temperature
- Voltage

Factors affecting DRAM reliability and latency cannot be properly modeled in simulation or analytically.

We need to perform experimental studies of real DRAM chips.
DRAM Testing Infrastructure

Allow experimental studies of real DRAM chips

Open-source FPGA-based testing infrastructure
• Publicly-available: Start using today
• Relatively low cost: An FPGA board + DRAM modules

SoftMC

Litex Tester
Limitations of Existing Infrastructure

<table>
<thead>
<tr>
<th>Testing Infrastructure</th>
<th>Interface (IF) Restrictions</th>
<th>Ease of Use</th>
<th>Extensibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>SoftMC [134]</td>
<td>Data IF</td>
<td>✗</td>
<td>✗</td>
</tr>
<tr>
<td>LiteX RowHammer Tester (LRT) [17]</td>
<td>Command &amp; Data IF</td>
<td>✗</td>
<td>✓</td>
</tr>
<tr>
<td>DRAM Bender (this work)</td>
<td>No Restrictions</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

Impose restrictions on the DDR4 interface. Restrictions limit various characterization experiments.

Difficult to set up (based on discontinued HW/SW) and use (require developing HW)

Monolithic hardware design makes extensions (new standards, prototypes) relatively difficult.
DRAM Bender: Design Goals

• **Flexibility**
  - Ability to test *any DRAM operation*
  - Ability to test *any combination* of DRAM operations and *custom timing* parameters

• **Ease of use**
  - Simple programming interface (C++)
  - Minimal programming effort and time
  - Accessible to a wide range of users
    • *who may lack experience in hardware design*

• **Extensibility**
  - Modular design
  - Well-defined interfaces between hardware modules
DRAM Bender: Overview

Publicly-available FPGA-based DDR4/3 (and HBM2) characterization infrastructure

Easily programmable using the DRAM Bender C++ API
## DRAM Bender: Prototypes

<table>
<thead>
<tr>
<th>Testing Infrastructure</th>
<th>Protocol Support</th>
<th>FPGA Support</th>
</tr>
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<tbody>
<tr>
<td>SoftMC [134]</td>
<td>DDR3</td>
<td>One Prototype</td>
</tr>
<tr>
<td>LiteX RowHammer Tester (LRT) [17]</td>
<td>DDR3/4, LPDDR4</td>
<td>Two Prototypes</td>
</tr>
<tr>
<td>DRAM Bender (this work)</td>
<td>DDR3/DDR4</td>
<td>Five Prototypes</td>
</tr>
</tbody>
</table>

### Five out of the box FPGA-based prototypes
1. RowHammer: Interleaving Pattern of Activations
   - Interleaving pattern significantly affects the number of RowHammer bitflips

2. RowHammer: Random Data Patterns
   - Use 512-bit random data patterns
   - Uncover more bitflips than 8-bit SoftMC random patterns

3. In-DRAM Bitwise Operations
   - Demonstrate in-DRAM bitwise AND/OR capability in real DDR4 chips

DRAM Bender is flexible: supports many different types of experiments
1. RowHammer: Interleaving Pattern of Activations

```c++
1  p.appendLI(hammerCount, 0);
2  p.appendLabel("HAMMER1");
3  p.appendACT(bank, false, A1, false, tRAS);
4  p.appendPRE(bank, false, false, tRP);
5  p.appendADDI(hammerCount, hammerCount, 1);
6  p.appendBL(hammerCount, T, "HAMMER1");
7  p.appendLI(hammerCount, 0);
8  p.appendLabel("HAMMER2");
9  p.appendACT(bank, false, A2, false, tRAS);
10 p.appendPRE(bank, false, false, tRP);
11 p.appendADDI(hammerCount, hammerCount, 1);
12 p.appendBL(hammerCount, T, "HAMMER2");
```

one iteration of the RowHammer test

Easy to devise new experiments to uncover new insights.
More in the paper (II)

- DRAM Bender design details
  - DRAM Bender instruction set architecture
  - Hardware & software modules
  - Prototype design
  - Temperature controller setup

- DRAM Bender application programming interface

- Detailed results for three case studies

- Future work & improvements
More in the paper (II)

DRAM Bender: An Extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM Chips

Ataberk Olgun§  Hasan Hassan§  A. Giray Yaşlıkçı§  Yahya Can Tuğrul§†
Lois Orosa§○  Haocong Luo§  Minesh Patel§  Oğuz Ergin†  Onur Mutlu§

§ ETH Zürich  † TOBB ETÜ  ○ Galician Supercomputing Center

https://arxiv.org/abs/2211.05838
1) [ISCA’23] Luo+, “RowPress: Amplifying Read Disturbance in Modern DRAM Chips”

2) [DSN’23 Disrupt] Olgun+, "An Experimental Analysis of RowHammer on HBM2 DRAM Chips"


5) [DSN’22] Yaglikci+, "Understanding RowHammer Under Reduced Wordline Voltage: An Experimental Study Using Real DRAM Devices"

6) [MICRO’21] Orosa+, “A Deeper Look into RowHammer’s Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses”

7) [MICRO’21] Hassan+, “Uncovering In-DRAM RowHammer Protection Mechanisms: A New Methodology, Custom RowHammer Patterns, and Implications”


9) [ISCA’21] Orosa+, “CODIC: A Low-Cost Substrate for Enabling Custom In-DRAM Functionalities and Optimizations”

10) [ISCA’20] Kim+, “Revisiting RowHammer: An Experimental Analysis of Modern Devices and Mitigation Techniques”

11) [S&P’20] Frigo+, “TRRespass: Exploiting the Many Sides of Target Row Refresh”


16) [MICRO’17] Khan+, “Detecting and Mitigating Data-Dependent DRAM Failures by Exploiting Current Memory Content”

17) [SIGMETRICS’16] Chang+, “Understanding Latency Variation in Modern DRAM Chips: Experimental Characterization, Analysis, and Optimization”
A Highlight: RowPress

Keeping a DRAM row **open for a long time** causes bitflips in adjacent rows

These bitflips do **NOT** require many row activations

**Only one activation** is enough in some cases!

**RowHammer**
- **Aggressor Row**
  - **Open**
  - **Close**
  - 36ns, 47K activations to induce bitflips

**RowPress**
- **Aggressor Row**
  - **Open**
  - **Close**
  - 7.8µs, only 5K activations to induce bitflips
RowPress Results & Source Code

RowPress: Amplifying Read Disturbance in Modern DRAM Chips

Haocong Luo      Ataberk Olgun      A. Giray Yağlıkçı      Yahya Can Tuğrul      Steve Rhyner
Meryem Banu Cavlak  Joël Lindeger      Mohammad Sadrosadati      Onur Mutlu

ETH Zürich

Fully open source and artifact evaluated

RowPress [ISCA 2023]

- Haocong Luo, Ataberk Olgun, Giray Yaglikci, Yahya Can Tugrul, Steve Rhyner, M. Banu Cavlak, Joel Lindegger, Mohammad Sadrosadati, and Onur Mutlu,

"RowPress: Amplifying Read Disturbance in Modern DRAM Chips"


[Slides (pptx) (pdf)]
[Lightning Talk Slides (pptx) (pdf)]
[Lightning Talk Video (3 minutes)]
[RowPress Source Code and Datasets (Officially Artifact Evaluated with All Badges)]

Officially artifact evaluated as available, reusable and reproducible.
Best artifact award at ISCA 2023.

RowPress: Amplifying Read-Disturbance in Modern DRAM Chips

Haocong Luo  Ataberk Olgun  A. Giray Yağlıkçı  Yahya Can Tuğrul  Steve Rhyner
Meryem Banu Cavlak  Joël Lindegger  Mohammad Sadrosadati  Onur Mutlu

ETH Zürich
More Research DRAM Bender Enabled

18) [DRAMSec’23] Lang+, “BLASTER: Characterizing the Blast Radius of Rowhammer”


20) [ETS’21] Farmani+, “RHAT: Efficient RowHammer-Aware Test for Modern DRAM Modules”

21) [HOST’20] Talukder+, “Towards the Avoidance of Counterfeit Memory: Identifying the DRAM Origin”

22) [MICRO’19] Gao+, “ComputeDRAM: In-Memory Compute Using Off-the-Shelf DRAMs”


DRAM Bender

The first publicly-available DDR4 characterization infrastructure

- **Flexible and Easy to Use**
- **Source code** available:

  [github.com/CMU-SAFARI/DRAMBender](https://github.com/CMU-SAFARI/DRAMBender)

DRAM Bender enables many studies, ideas, and methodologies in the design of future memory systems
DRAM Bender

- Ataberk Olgun, Hasan Hassan, A Giray Yaşlıkçı, Yahya Can Tuğrul, Lois Orosa, Haocong Luo, Minesh Patel, Oğuz Ergin, and Onur Mutlu,

*"DRAM Bender: An Extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM Chips"*


[Extended arXiv version]

[DRAM Bender Source Code]

[DRAM Bender Tutorial Video (43 minutes)]

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**DRAM Bender: An Extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM Chips**

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SAFARI  

https://github.com/CMU-SAFA/DRAM-Bender
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