SoftMC Tutorial

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Summary

- **SoftMC**: an FPGA-based DRAM testing infrastructure
- **Characterize, analyze, and understand** DRAM cell behavior
- **Flexible and Easy to Use** (C++ API)
- Open-source ([github.com/CMU-SAFARI/SoftMC](https://github.com/CMU-SAFARI/SoftMC))
- **SoftMC enables a wide range of studies**
DRAM Organization

Memory Bus

Memory Controller

CPU
Accessing DRAM

- Precharge
- Activate
- Read

DRAM Subarray

- DRAM Cell
- DRAM Row
- Sense Amplifier
Retention Time: The interval during which the data is retained correctly in the DRAM cell without accessing it.
Latency vs. Reliability

Violating latencies negatively affects DRAM reliability
Other Factors Affecting Reliability and Latency

• Temperature
• Voltage
• Inter-cell Interference
• Manufacturing Process
• Retention Time

To develop new mechanisms improving **reliability** and **latency**, we need to better understand the effects of these factors.
Characterizing DRAM

Many of the factors affecting DRAM reliability and latency cannot be properly modeled.

We need to perform experimental studies of real DRAM chips.
SoftMC

- FPGA-based DRAM characterization infrastructure
- Ability to test *any* DRAM operation
- Ability to test *any combination* of DRAM operations and *custom timing* parameters
- Simple programming interface (C++)
Current SoftMC Setups

DDR3

DDR4
SoftMC Programming DEMO