P&S Modern SSDs

Understanding and Designing Modern NAND Flash-Based Solid-State Drives

Dr. Jisung Park
Prof. Onur Mutlu
ETH Zürich

Spring 2021

31 March 2021

Today's Agenda

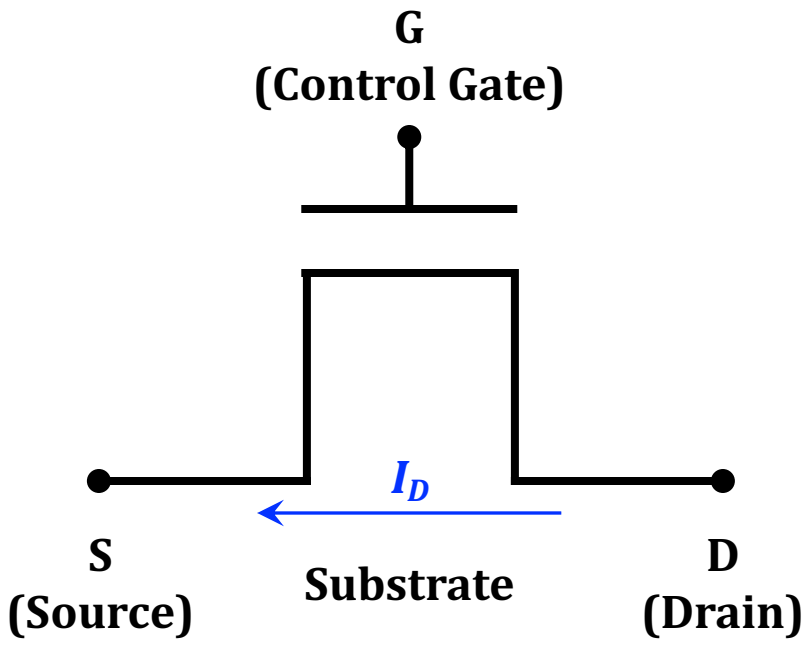
- Progress Review
- NAND Flash Organization

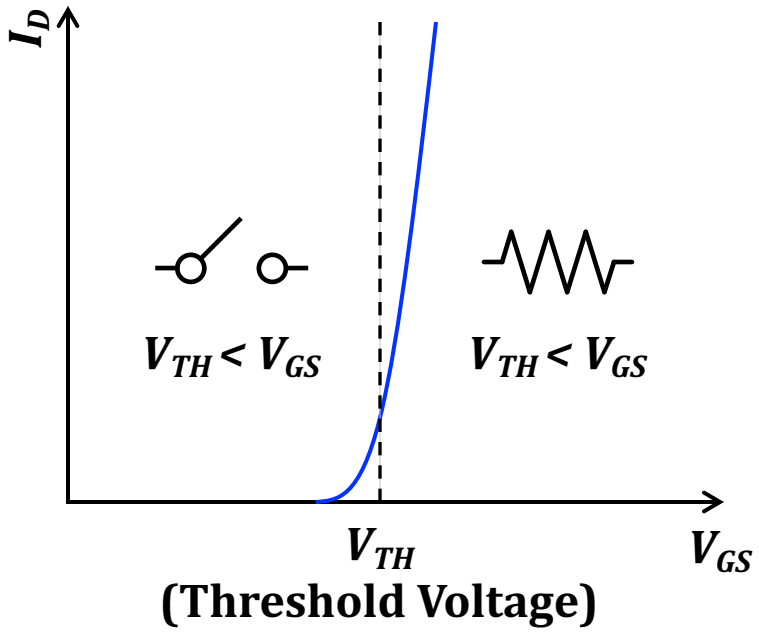
Progress Review

- Refactoring the simulation engine
  - Push your modifications into the repository when ready
- How does the simulation engine work?
- How did you improved?
- How did you validated your modifications?
- Any Questions?

A Flash Cell

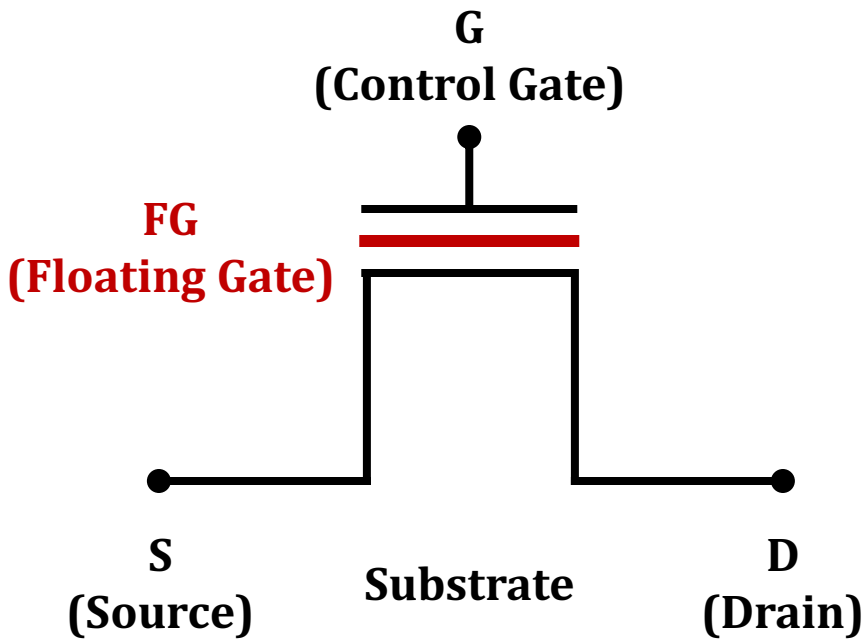
- Basically, it is a transistor

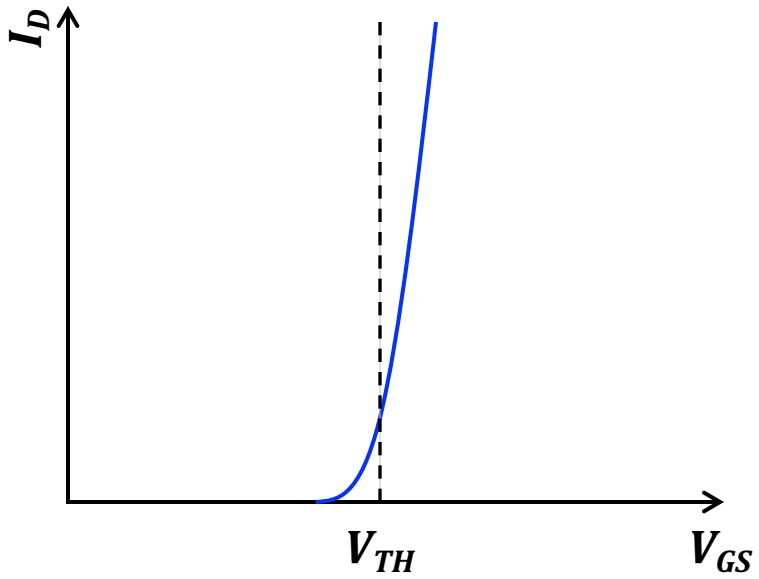




A Flash Cell

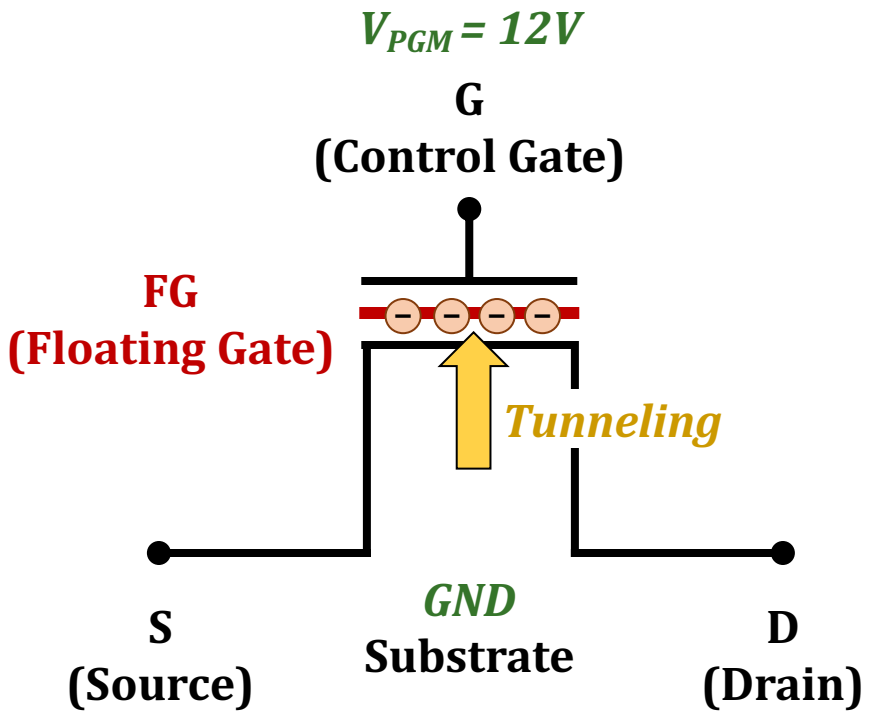
- Basically, it is a transistor
  - w/ a special material: Floating gate (2D) or Charge trap (3D)

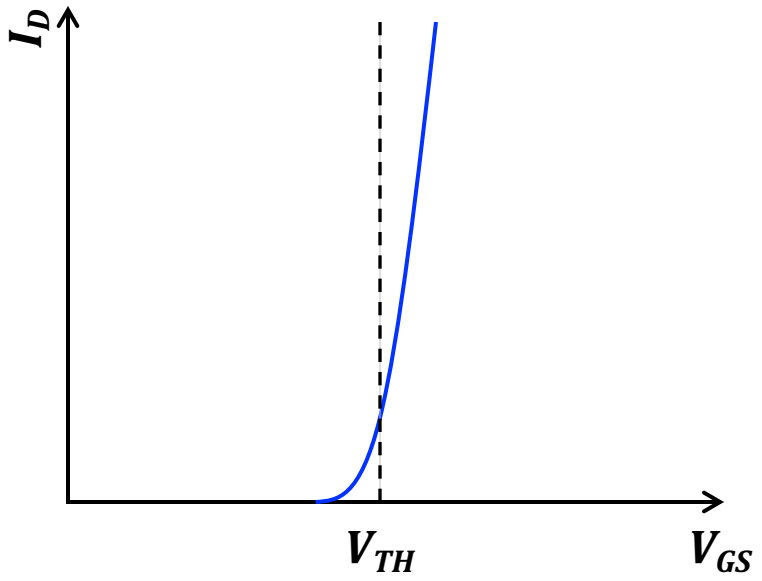




A Flash Cell

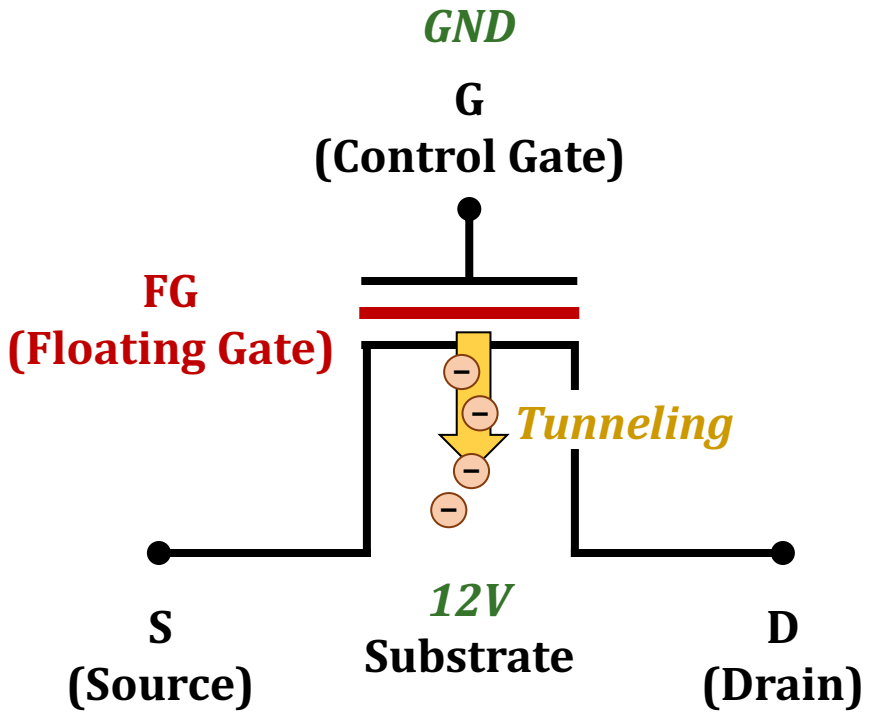
- Basically, it is a transistor
  - w/ a special material: Floating gate (2D) or Charge trap (3D)
  - Can hold electrons in a non-volatile manner

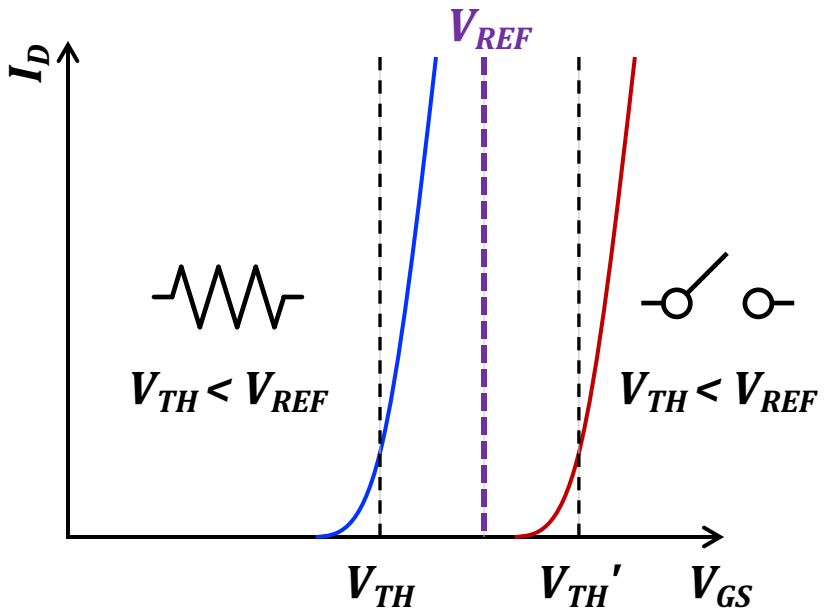




A Flash Cell

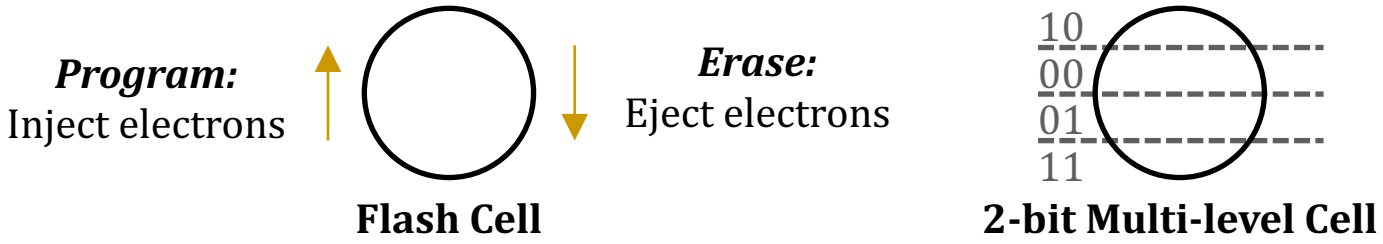
- Basically, it is a transistor
  - w/ a special material: Floating gate (2D) or Charge trap (3D)
  - Can hold electrons in a non-volatile manner
  - Changes the cell's threshold voltage (V_{TH})



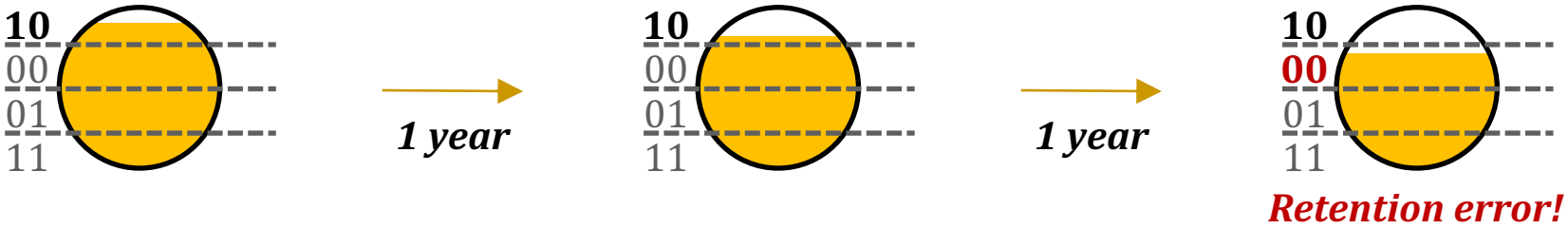


Flash Cell Characteristics

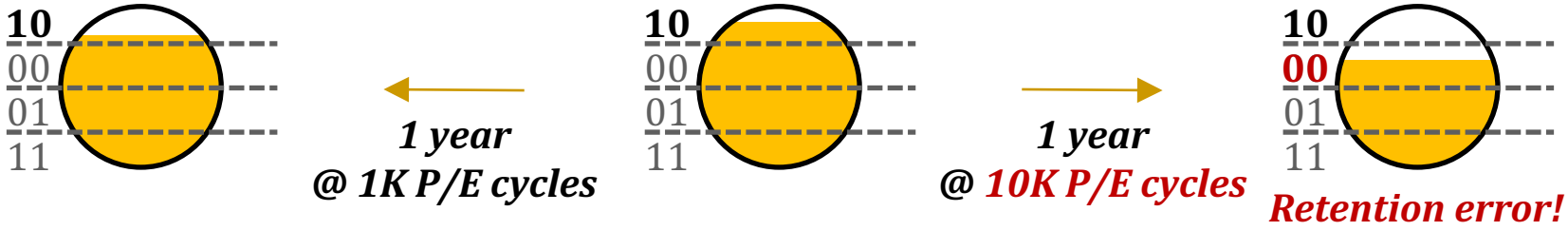
- Multi-leveling: A cell can store multiple bits



- Retention loss: A cell leaks electrons over time

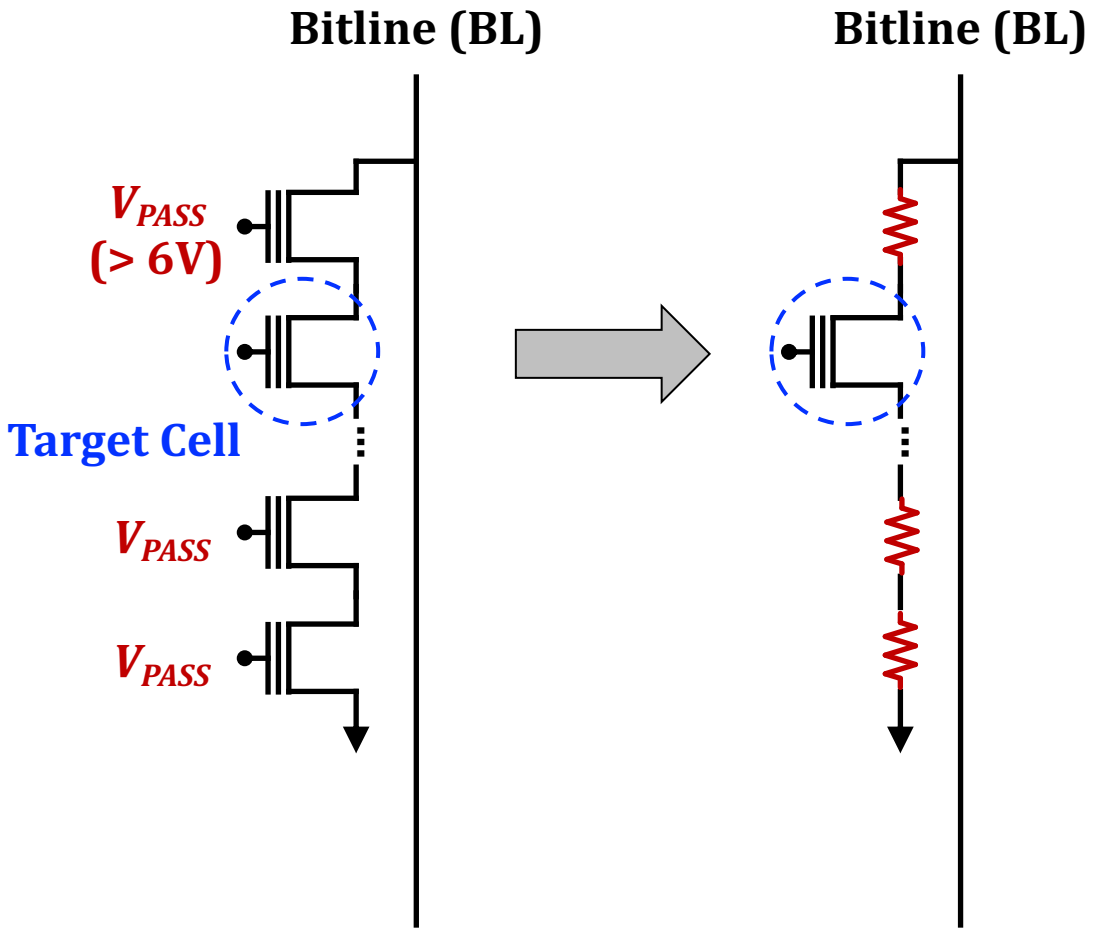


- Limited lifetime: A cell wears out after P/E cycling



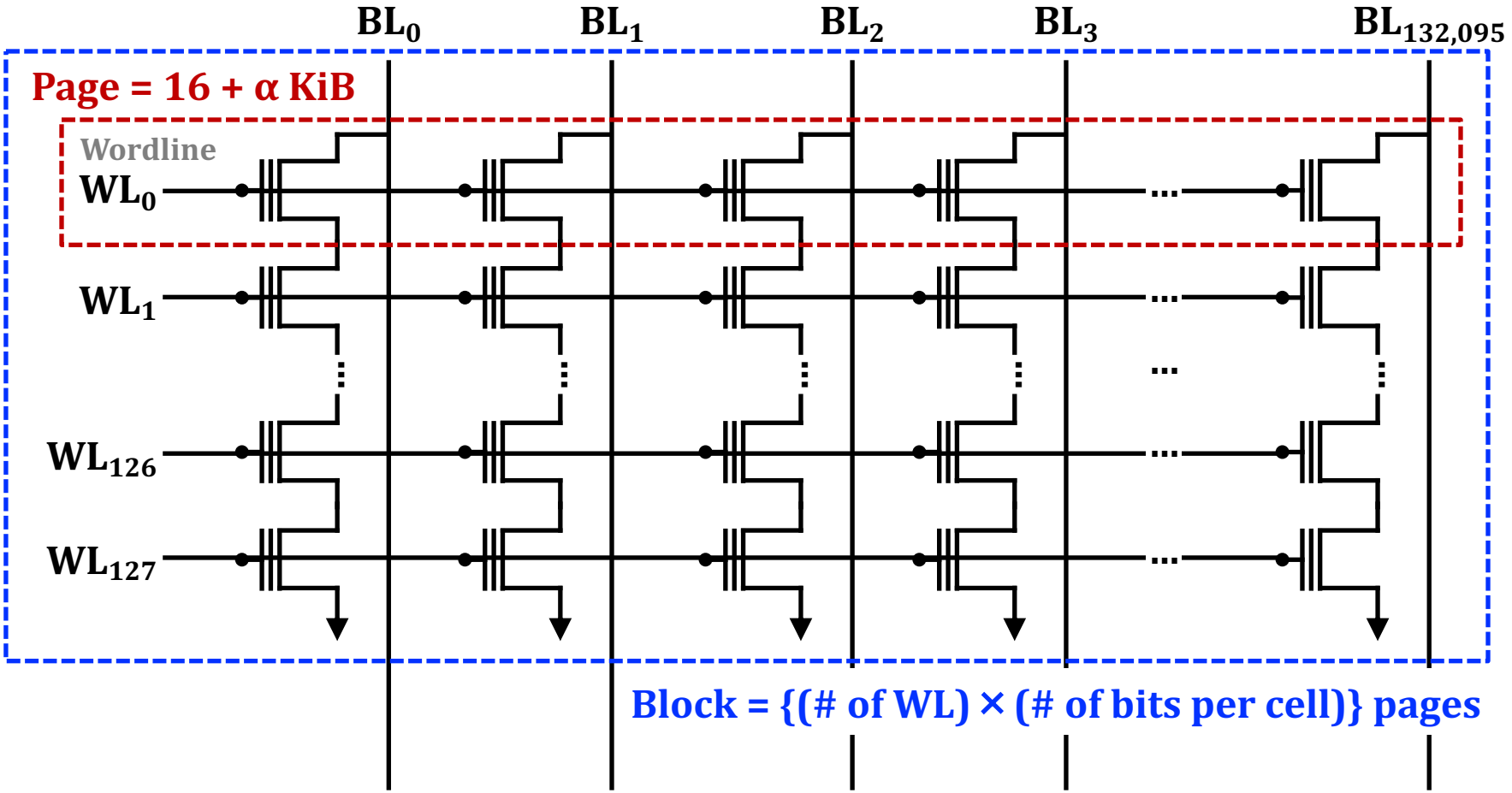
A NAND String

- Multiple (e.g., 128) flash cells are serially connected



Pages and Blocks

- A large number (> 100,000) of cells operate concurrently

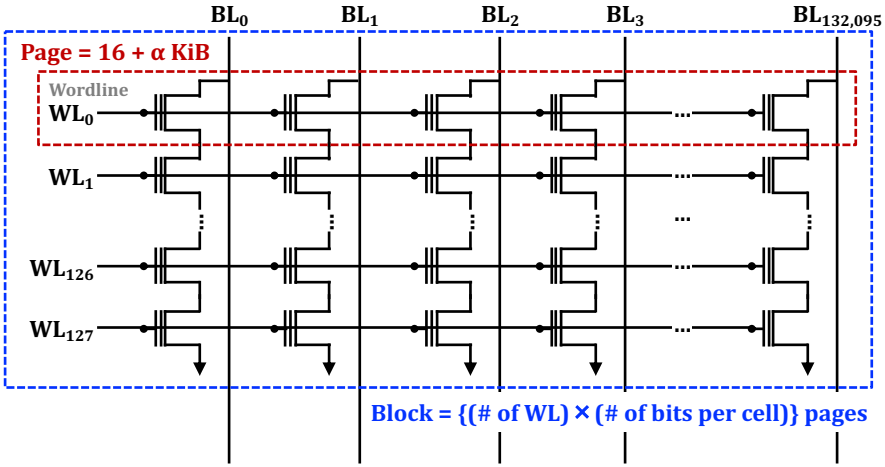


Pages and Blocks (Continued)

- Program and erase: Unidirectional
  - Programming a cell → Increasing the cell's VTH
  - Eraseing a cell → Decreasing the cell's VTH

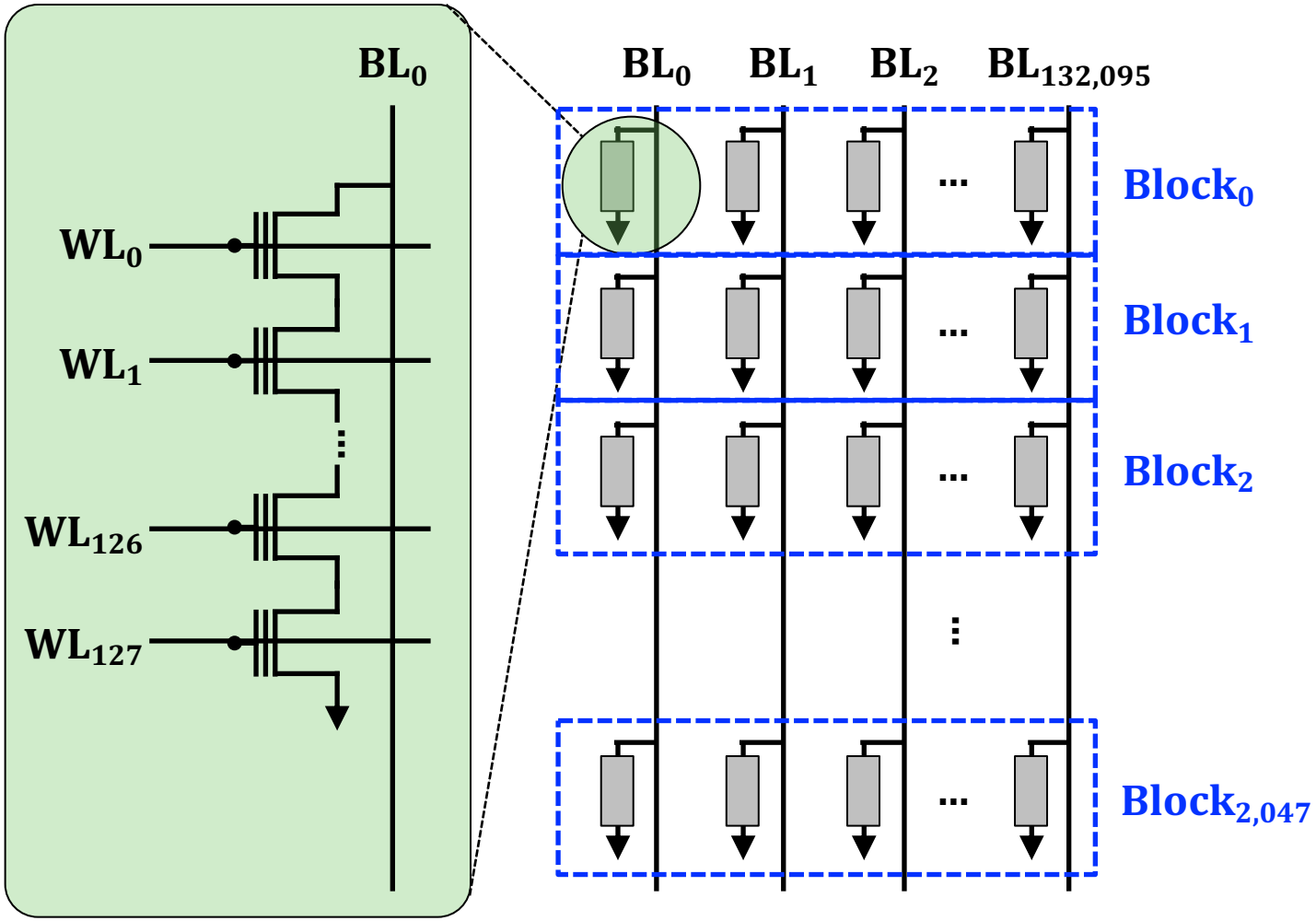
- Programming a page cannot change '0' cells to '1' cells
  → Erase-before-write property

- Erase unit: Block
  - Increase erase bandwidth
  - Makes in-place write on a page very inefficient
    → Out-of-place write & GC



Planes

- A large number (> 1,000) of blocks share bitlines in a plane



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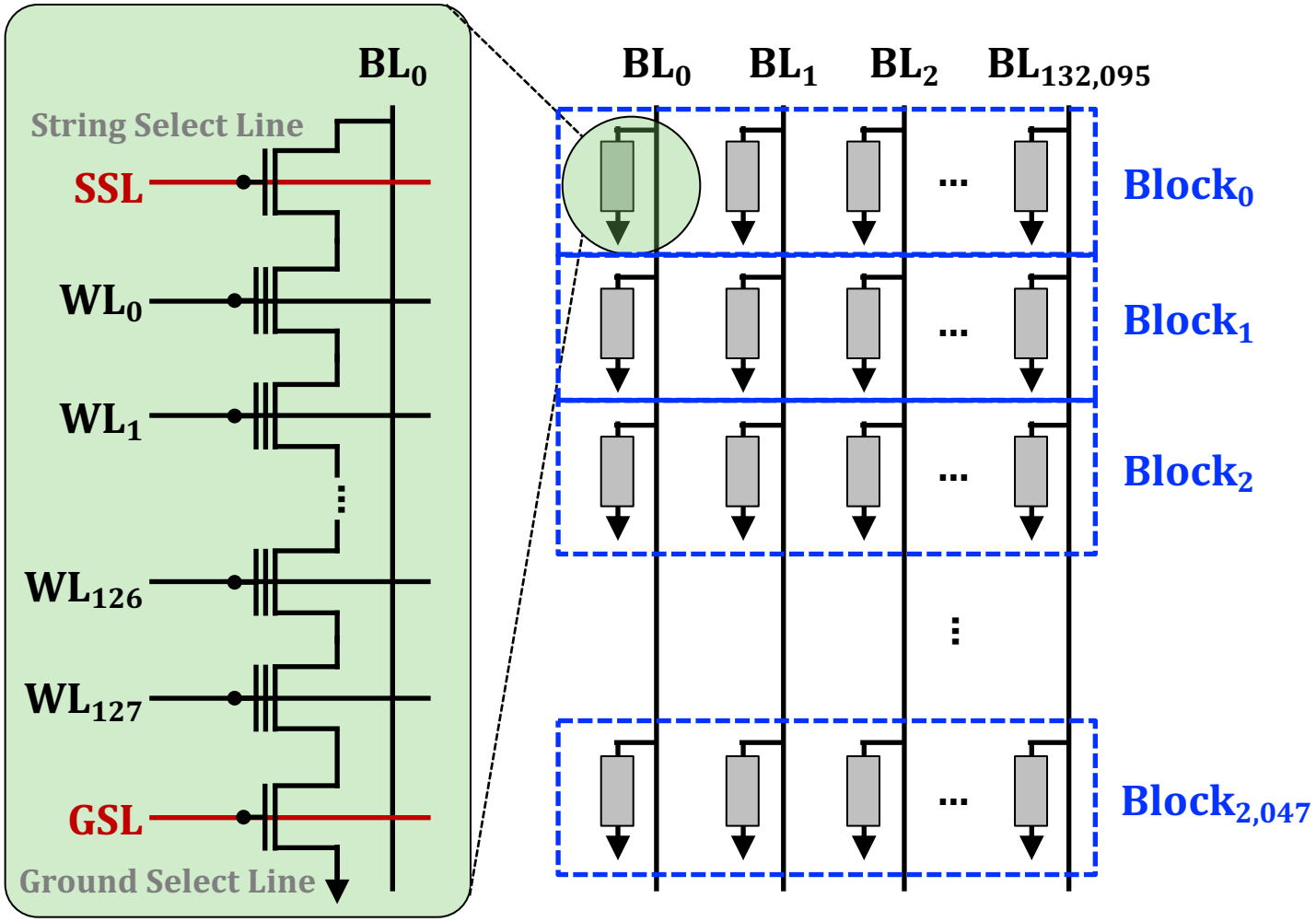
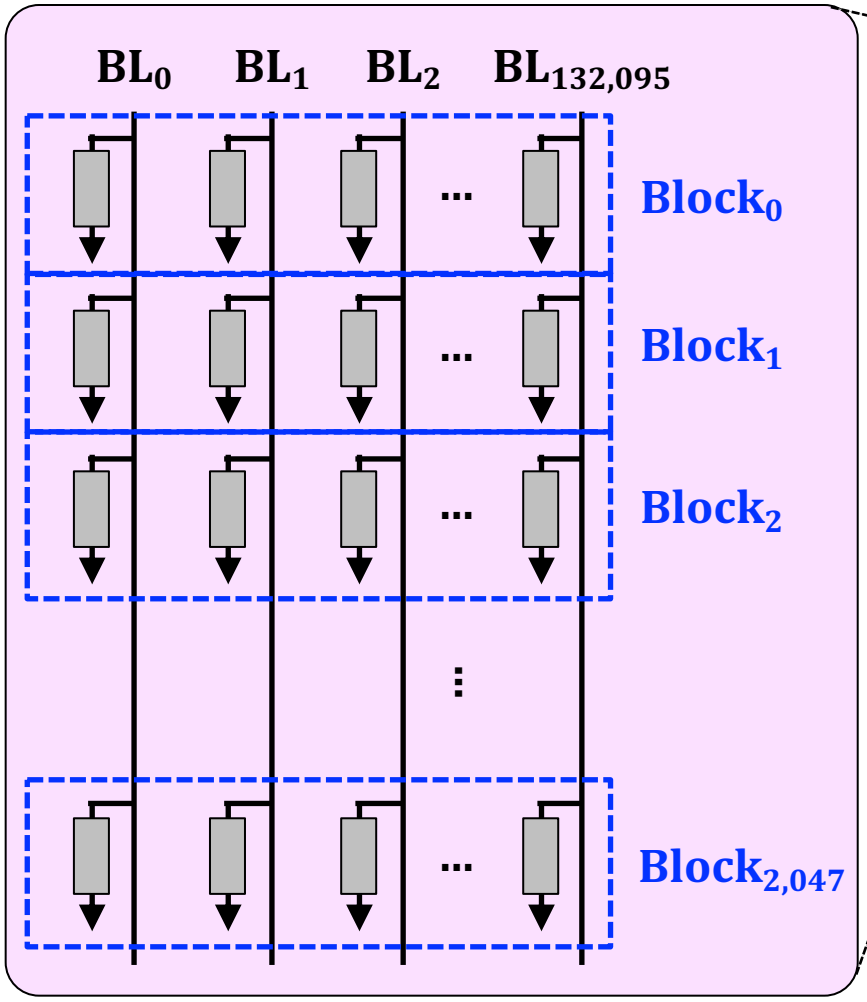
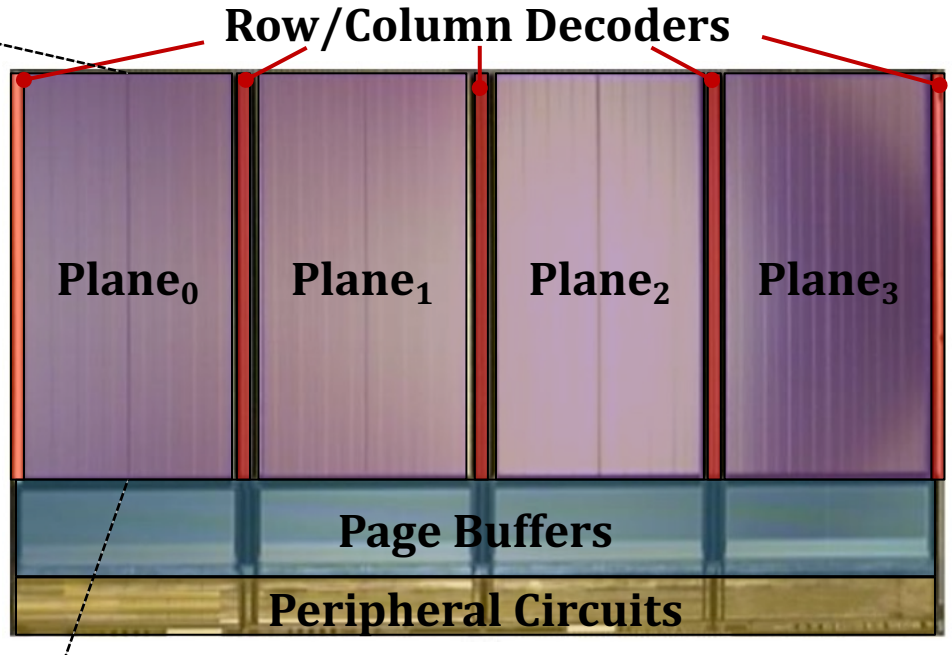


Planes and Dies

- A die (or chip) contains multiple (e.g., 2 – 4) planes





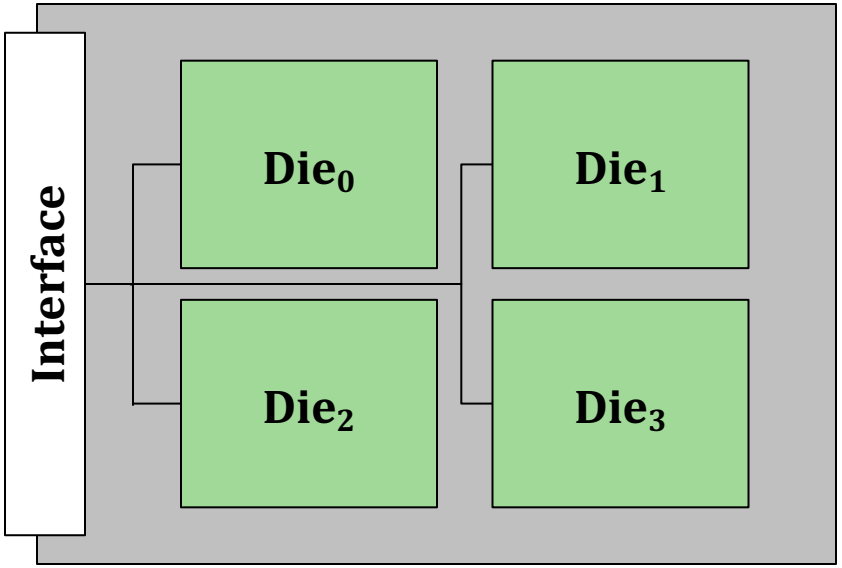
A 21-nm 2D NAND Flash Die

- Planes share decoders: limit internal parallelism (only operations @ the same WL offset)

Dies

- A package contains multiple (e.g., 4 – 8) dies
  - Dies share a channel (or a bus)
  - To communicate with the flash controller

- Dies can operate independently of each other
  - w/ channel interleaving



Next Meetings

- We will provide more background on NAND flash memory
- We will discuss your progress in last week
  - Please contact us whenever you have any questions

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