P&S Modern SSDs

Understanding and Designing Modern NAND Flash-Based Solid-State Drives

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Today’s Agenda

■ Progress Review

■ Basic NAND Flash Operation
Progress Review

- Refactoring the simulation engine
  - Push your modifications into the repository when ready

- How does the simulation engine work?

- How did you improved?

- How did you validated your modifications?

- Any Questions?
Recap: Program/Erase/Read a Flash Cell

- Basically, a flash cell is a transistor
  - w/ a special material: Floating gate (2D) or Charge trap (3D)
  - Can hold electrons in a non-volatile manner

\[ V_{PGM} = 12V \]

- G (Control Gate)
- FG (Floating Gate)
- S (Source)
- D (Drain)
- GND (Substrate)

\[ V_{TH} \]
Recap: Program/Erase/Read a Flash Cell

- Basically, it is a transistor
  - w/ a special material: Floating gate (2D) or Charge trap (3D)
  - Can hold electrons in a non-volatile manner
  - Changes the cell’s threshold voltage ($V_{TH}$)

![Diagram of Flash Cell](image-url)

- **GND**
- **G** (Control Gate)
- **S** (Source)
- **D** (Drain)
- **Substrate**
- **FG** (Floating Gate)
- **12V**
- **Tunneling**

- $V_{TH} < V_{REF}$
- $V_{TH} < V_{REF}$
Recap: Pages and Blocks

- A large number (> 100,000) of cells operate concurrently

Page = 16 + α KiB

Block = \{ (# of WL) × (# of bits per cell) \} pages
Threshold Voltage Distribution

- $V_{TH}$ distribution of cells in a programmed page/block/chip

Why distribution? Variations across the cells
- Some cells are more easily programmed or erased

Why (almost) the same shape?
- Every data is stored after randomized for better reliability
- In reality, $V_{TH}$ states’ shapes can be different, but there areas are almost the same
**V\textsubscript{TH} Distribution of MLC NAND Flash**

- **Multi-level cell (MLC) technique**
  - $2^m \text{V}_{TH}$ states required to store $m$ bits in a single flash cell

- **Limited width** of the $V_{TH}$ window: Need to
  - Make each $V_{TH}$ state narrow
  - Guarantee **sufficient margins** b/w adjacent $V_{TH}$ states
**$V_{TH}$ Distribution of MLC NAND Flash**

- **Multi-level cell (MLC) technique**
  - $2^n V_{TH}$ states required to store $m$ bits in a single flash cell

- **Limited width of the $V_{TH}$ window:** Need to
  - Make each $V_{TH}$ state narrow
  - Guarantee sufficient margins b/w adjacent $V_{TH}$ states
    - $V_{TH}$ changes over time after programmed
    - Narrower margins $\Rightarrow$ Lower reliability
    - More bits per cell $\Rightarrow$ higher density but lower reliability

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![Diagram showing $V_{TH}$ distribution with $V_{REF}$ levels and error cells.](image-url)
Basic Operation: Page Program

![Diagram showing basic operation of page program with BL0, BL1, BL2, BL3, and BL132,095 blocks and WLk, WLk+1, SSL, and GSL select lines. The diagram highlights a target page with WLk.]
Basic Operation: Page Program

- **WL control** – **All other cells operate as a resistance**

```
<table>
<thead>
<tr>
<th></th>
<th>BL0</th>
<th>BL1</th>
<th>BL2</th>
<th>BL3</th>
<th>BL132,095</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{CC} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{PASS} )</td>
<td>( WL_{k-1} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{PROG} )</td>
<td>( WL_k )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{PASS} )</td>
<td>( WL_{k+1} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{CC} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Ground Select Line</td>
</tr>
<tr>
<td>SSL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Ground Select Line</td>
</tr>
</tbody>
</table>

\( V_{CC} \), \( V_{PASS} \), and \( V_{PROG} \) are applied to control the operation of the memory cells.
Basic Operation: Page Program

- BL control – **Inhibits cells** to not be programmed

![Diagram](image-url)

- **Program**
- **Inhibit**

$$V_{PROG} \quad WL_k$$
Basic Operation: Page Program

- BL control – **Inhibits cells** to not be programmed

![Diagram showing BL control](image)
Basic Operation: Page Program

Program

Inhibit

\[ V_{PROG} \]

\[ WL_k \]

\[ \begin{array}{c}
\text{To GND} \\
\text{To } V_{CC} \\
\text{To GND} \\
\text{To } V_{CC} \\
\text{To GND}
\end{array} \]

# of cells

Threshold voltage (\( V_{TH} \))

Erased (E)

\[ V_{REF} \]
Basic Operation: Page Program

Program:

1. Apply a voltage $V_{PROG}$ to WL subscripts
2. Apply a voltage to BL subscripts
   - BL0: 0
   - BL1: 1
   - BL2: 0
   - BL3: 1
   - BL132,095: 0

Inhibit:

1. Apply a voltage $V_{CC}$ to BL subscripts

# of cells

- **Inhibited cells**
  - Erased (E)
  - Programmed

Threshold voltage ($V_{TH}$)

- $V_{REF}$
- Programmed cells
- Erased (E)
Basic Operation: Page Program

Program

Inhibit

0 1 0 1

To GND To Vcc To GND To Vcc

# of cells

Threshold voltage ($V_{TH}$)

Inhibited cells

1 Erased (E)

Cells to program

$V_{REF}$

Hard-to-program cells

Easy-to-program cells
Basic Operation: Page Program

- Incremental Step-Pulse Programming (ISPP)

![Diagram showing program and inhibit steps for BL0 to BL132,095](image)

- Program: WLk to Vprog, BL0 to GND, BL1 to Vcc, BL2 to GND, BL3 to Vcc, BL132,095 to GND
- Inhibit: BL0 to 1, BL1 to 0, BL2 to 1, BL3 to 0, BL132,095 to 0

- # of cells
- Erased (E)
- Inhibited cells
- Cells to program
- VREF

Verified as programmed:

Threshold voltage (V_{TH})
Basic Operation: Page Program

- Incremental Step-Pulse Programming (ISPP)

- **WL**: Word Line
- **BL**: Bit Line
- **Vcc**: Voltage Source
- **GND**: Ground

Diagram:
- WL: Write Line
- BL: Bit Line
- Program: Write to memory
- Inhibit: Prevent writing

Graph:
- X-axis: Threshold voltage ($V_{TH}$)
- Y-axis: Number of cells
- Inhibited cells
- Erased (E)
- Cells to program
- VREF

**Key Points**:
- Program cells
- Inhibit programed cells
- WL and BL connections to GND and Vcc
Basic Operation: Page Program

- Incremental Step-Pulse Programming (ISPP)

![Diagram showing Basic Operation: Page Program]

- **Program**: $V_{PROG1}$ and $WL_k$
- **Inhibit**: $BL_0$, $BL_1$, $BL_2$, $BL_3$, $BL_{132,095}$

**Inhibit**

- Programmed Cells
- Erased Cells ($E$)

**Threshold voltage ($V_{TH}$)**

- **Inhibited cells**
- **Cells to program**

$V_{REF}$
Basic Operation: Page Program

- Incremental Step-Pulse Programming (ISPP)

**Diagram:**
- **V_{PROG1}** and **WL_k**
- **BL_0** with 0 (program)
- **BL_1** with 1 (inhibit)
- **BL_2** with 0
- **BL_3** with 1
- **BL_{132,095}** with 0

**Legend:**
- **# of cells**
- **Inhibited cells**
- **Inhibited programmed cells**
- **Erased (E)**
- **Threshold voltage (V_{TH})**
- **Cells to program**
- **Programmed**
- **V_{REF}**

- **To GND**: Connections to ground
- **To V_{CC}**: Connections to power supply

**IC Design:**
- BL0
- BL1
- BL2
- BL3
- BL_{132,095}

**Cells:**
- Programmed
- Erased (E)
Basic Operation: Page Read

- WL control – All other cells operate as a resistance

![Diagram showing WL control and resistance operation]

\( V_{REF} \) \( WL_k \)

\( BL_0 \) \( BL_1 \) \( BL_2 \) \( BL_3 \) \( BL_{132,095} \)

\( 0 \) \( 1 \) \( 0 \) \( 1 \) \( 0 \)

- Erased (E)
- Programmed

Threshold voltage (\( V_{TH} \))

\( # \text{ of cells} \)
Basic Operation: Page Read

- **BL control** – Charge all BLs

![Diagram showing BL control and charge for different cells](image)

- **VREF**
- **WLk**

<table>
<thead>
<tr>
<th>BL</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>BL0</td>
<td>0</td>
</tr>
<tr>
<td>BL1</td>
<td>1</td>
</tr>
<tr>
<td>BL2</td>
<td>0</td>
</tr>
<tr>
<td>BL3</td>
<td>1</td>
</tr>
<tr>
<td>BL132,095</td>
<td>0</td>
</tr>
</tbody>
</table>

**# of cells**

- **1 Erased (E)**
- **0 Programmed**

**Threshold voltage (V_{TH})**

**VREF**
Basic Operation: Page Read

- Sensing the current through BLs

![Diagram](image_url)

- **V_{TH} < V_{REF}**
  - Erased (E)
  - Threshold voltage (V_{TH})

- **V_{REF}**

- **V_{TH} < V_{REF}**
  - Programmed

- **(No current)**
  - **(Current)**

- # of cells

- WL_{k}

- BL_{0} 0

- BL_{1} 1

- BL_{2} 0

- BL_{3} 1

- BL_{132,095} 0
Basic Operation: Page Read - MLC

- Sensing the current through BLs

![Diagram](image-url)
Basic Operation: Page Read - MLC

- Sensing the current through BLs

![Diagram showing basic operation of MLC with sensing through BLs and voltage references.](image_url)
Basic Operation: Page Read - MLC

- Sensing the current through BLs

![Diagram showing the sensing process through BLs with voltage levels at different points along the word line (WLk) and bit lines (BL0 to BL132,095). The diagram also illustrates the reference voltages (V_{REF0} to V_{REF6}) and the voltage threshold (V_{TH}).]
Basic Operation: Page Read - MLC

- Sensing the current through BLs

![Diagram showing the sensing of the current through BLs and the corresponding voltage levels with reference voltages (V_{REF0} to V_{REF6}) and cell states (P1 to P7).]
Basic Operation: Page Read - MLC

- Sensing the current through BLs
Basic Operation: Page Read – Takeaways

- MLC NAND flash memory requires an in-chip XOR logic
- Bit-encoding affects the read latency!
  - Compare # of sensing for CSB

\[
\begin{align*}
\text{MSB} & \quad \text{LSB} \\
E & \quad 111 \\
P1 & \quad 110 \\
P2 & \quad 100 \\
P3 & \quad 000 \\
P4 & \quad 010 \\
P5 & \quad 011 \\
P6 & \quad 001 \\
P7 & \quad 101 \\
\end{align*}
\]
Next Meetings

- We will provide more background on NAND flash memory
- We will discuss your progress in last week
  - Please contact us whenever you have any questions
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