

Bachelor's / Master's / Semester Project

Securing Main Memory

DRAM-based main memory is used in most computers today. Manufacturers have been optimizing DRAM capacity and bandwidth for years, but little effort has been done for designing secure memories.

Our goal is to discover **new security vulnerabilities in DRAM** and propose new mechanisms that provide **security support in DRAM**. This requires characterizing DRAM under different working conditions and testing different data and address patterns. Our group has developed a DRAM **testing infrastructure** for memory characterization. To design new in-Memory security mechanisms, our group has developed a **DRAM simulator** that allows evaluating new hardware features in DRAM quickly.

You will be involved with designing and conducting experiments with other researchers. The goals are: 1) discover new security vulnerabilities and identify new attack vectors that might compromise the security of the system, and 2) designing new security mechanisms that protect from these and other vulnerabilities using our infrastructure.

Requirements

- Outstanding programming skills (C/C++/Python)
- Strong interest in computer architecture and hardware security
- An interest in developing and evaluating new ideas
- Strong work ethic

For **example studies** you may perform, please see:

- ["Flipping Bits in Memory Without Accessing Them: An Experimental Study of DRAM Disturbance Errors"](#), *ISCA* 2014.
- ["The DRAM Latency PUF: Quickly Evaluating Physical Unclonable Functions by Exploiting the Latency-Reliability Tradeoff in Modern DRAM Devices"](#), *HPCA* 2018.
- ["D-RaNGe: Using Commodity DRAM Devices to Generate True Random Numbers with Low Latency and High Throughput"](#), *HPCA* 2019.
- ["Dataplant: In-DRAM Security Mechanisms for Low-Cost Devices"](#), arXiv 2019

If you are interested, please email:

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