

Title:

An Addiction to Low Cost Per Memory Bit - How to Recognize it and What to Do About it

Abstract:

The phenomenal rise in the amounts of data has put great pressure on the semiconductor industry to provide low cost memory solutions. The result is a constant drive to lower the cost per bit of DRAM, SRAM and NAND Flash. In addition, AI requires intense store and recall between processor and memory. In the rush to provide low cost solutions, other attributes have been treated as expendable as an acceptable cost of doing business. Several examples come to mind: short product lifetimes because of limited NAND Flash endurance; data insecurity because of DRAM Rowhammer; poor energy efficiency because of the need to bring growing amounts of data from DRAM into the processor chip due to SRAM area inefficiencies. All such "negative externalities" have a cost that is not included in the product cost but affects society in terms of wasted energy and resources. This talk looks into their origins and consequences and is a call to action for a more comprehensive understanding of what cost per bit really means.

Biography

Andy Walker has been working in silicon technology since 1985. After a BSc in physics from Dundee University in Scotland he joined Philips Research Laboratory in Eindhoven, The Netherlands. His PhD from the Technical University of Eindhoven arose from his research work at Philips. In 1994 he came to Silicon Valley and worked at various companies including Cypress, Matrix and Spin Memory. He also founded Schiltron Corporation to develop new forms of monolithic memories. He has been fortunate in being able to work in many interesting areas of silicon devices and process technology including MOS device physics, nonvolatile memories, ESD and Latch-up, TFTs and MRAM. He is now active in the area of GaN high voltage devices.