

Bachelor's / Master's / Semester Project

Designing and Evaluating Energy-Efficient Main Memory

DRAM-based main memory is used in nearly all computers today, but its energy consumption is becoming a **growing concern**. **DRAM energy utilization** now accounts for as much as 40% of the total energy used by a computer.

Our goal is to design **new DRAM-based memory** architectures that reduce the energy consumption significantly. This requires a principled approach, where we must measure how existing DRAM devices consume energy. Our group has developed a sophisticated **energy measurement infrastructure** to collect detailed information on DRAM energy usage.

You will be involved with designing and conducting experiments to measure energy consumption using our infrastructure. Based on the data, you will work with other researchers to identify memory operations that consume large amounts of energy, and will design new DRAM architectures that improve the efficiency of these operations.

Requirements

- Outstanding programming skills (C/C++)
- Familiarity with FPGA programming and Verilog/RTL design
- Computer architecture background
- An interest in developing and evaluating new ideas
- Strong work ethic

For **example studies** you may perform please see:

- ["SoftMC: A Flexible and Practical Open-Source Infrastructure for Enabling Experimental DRAM Studies"](#), HPCA 2017.
- ["Understanding Reduced-Voltage Operation in Modern DRAM Devices: Experimental Characterization, Analysis, and Mechanisms"](#), SIGMETRICS 2017.
- ["Understanding Latency Variation in Modern DRAM Chips: Experimental Characterization, Analysis, and Optimization"](#), SIGMETRICS 2016.

If you are interested, please email:

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