SAFARI
SAFARI Research Group

Semester project (practical work) D-INFK students

Improving the Trustworthiness and Accuracy of DRAM Models in Ramulator 2

Background

Memory is the major performance, energy and reliability bottleneck of all data-intensive workloads, e.g., deep learning, graph processing, in-memory databases, genome analysis.

The landscape of main memory is quickly changing with many technologies appearing and being proposed. This includes many new DRAM standards (e.g., DDR5, LPDDR5, HBM3), new types of DRAM architectures, novel memory designs that are capable of processing in/near memory, new non-volatile memory technologies that are poised to replace DRAM, etc. The impact of such new designs and technologies on systems and applications need to be quickly evaluated and understood, with rigorous evaluation infrastructures.

Ramulator 2.0 is a modern, modular, and extensible DRAM simulator, developed as a successor to Ramulator (1.0). The public version of Ramulator 2.0 is available at https://github.com/CMU-SAFARI/ramulator2 Ramulator 2.0 models a wide range of DRAM standards, including DDR3, DDR4, DDR5, LPDDR5, HBM2/3, GDDR6, etc. The DRAM models of DDR3 and DDR4 are validated against publicly-available verification models provided by DRAM manufacturers. Unfortunately, for newer DRAM standards, there exist no publicly-available verification models.

Your Task

Phase I

Expected Completion Time: 1 week
You will learn the basics of DRAM. We will provide you with resources covering:

- Introduction to the DRAM-based main memory system
- Basic DRAM organization
- Key DRAM operations

We will also walk you through the JEDEC DDR4 standard so you are better prepared for the next phase of the project. If you are already familiar with DRAM basics, you can directly start with Phase II.

Phase II

Expected Completion Time: 2-3 weeks
You will choose a DRAM standard from the following:

- DDR5
- LPDDR5
- HBM2/3
- GDDR6

You will read and digest the JEDEC specification documents of the DRAM standard you chose to understand its key features. To proceed to the next phase, you will need to present to us and demonstrate that you have a good understanding of the key differences of the standard you chose (in terms of key organization, command, and timings) compared to DDR4.

Phase III

Expected Completion Time: 2 months
In this phase, first, we will give you a tutorial on Ramulator 2, focusing on the DRAM modeling methodology and implementation details.

Second, you will implement tests, using the test framework provided by us (based on gtest), that validates both the microarchitectural (e.g., DRAM commands and timing constraints) and high-level characteristics (e.g., bandwidth and latency) of the DRAM standard you chose in Phase II. You will also fix the bugs you find during the process.

Prerequisite

- Be interested in and have basic background knowledge in computer architecture, especially the memory system (e.g., has taken DDCA or any equivalent course)
- Be comfortable in coding with modern C++, preferably experience with C++20
- Willing to follow good coding practices and maintain proper documentation of the code you write
- Strong work ethic, attention to detail

Credits

This is mainly aimed as a semester project (practical work) for D-INFK students who would like to develop quality software. However, other course or project types are also potentially possible to satisfy with this work, depending on the experience level of the student and the requirements of the course.

If you are interested, please email:
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