Functionally-Complete Boolean Logic in Real DRAM Chips
Experimental Characterization and Analysis

Ismail Emir Yüksel
Yahya C. Tugrul  Ataberk Olgun  F. Nisa Bostancı
A. Giray Yağlıkçı  Geraldo F. Oliveira  Haocong Luo
Juan Gómez–Luna  Mohammad Sadr  Onur Mutlu

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Executive Summary

• **Motivation:** Processing-using-DRAM can alleviate the performance and energy bottlenecks caused by data movement
  – **Prior works** show that existing DRAM chips can perform three-input majority and two-input AND and OR operations

• **Problem:** Proof-of-concept demonstrations on commercial off-the-shelf (COTS) DRAM chips do not provide
  – functionally-complete operations (e.g., NAND or NOR)
  – NOT operation
  – AND and OR operations with more than two inputs

• **Experimental Study:** 256 DDR4 chips from two major manufacturers

• **Key Results:**
  – COTS DRAM chips can perform NOT and {2, 4, 8, 16}-input AND, NAND, OR, and NOR operations with very high reliability (>94% success rate)
  – Data pattern and temperature only slightly affect the reliability of these operations (<1.98% decrease in success rate)
Outline

Background

Goal & Overview

Experimental Methodology

Multiple-Row Activation in Neighboring Subarrays

NOT Operation

AND, NAND, OR, and NOR Operations

Conclusion

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Outline

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Conclusion
DRAM Organization

DRAM Module

DRAM Chip

Chip I/O

Bank

DRAM Chip

DRAM Bank

Sense Amplifiers

Subarray

DRAM Row

Sense Amps.

Wordline

Bitline
DRAM Open Bitline Architecture

DRAM Bank

Subarray

SA

SA

SA

SA

SA

Sense Amplifier

bitline
DRAM Open Bitline Architecture

- **Activated**
  - bitline
  - NOT Gate
  - Serves as the reference for the SA

- **Not Activated**

**DRAM Bank**

**Subarray**

- **SA**
- **SA**
DRAM Operation

1. **ACTIVATE (ACT):**
   Fetch the row’s content into the sense amplifiers

2. **Column Access (RD/WR):**
   Read/Write the target column and drive to I/O

3. **PRECHARGE (PRE):**
   Prepare the subarray for a new ACTIVATE
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Our Goal

Understand the **capability** of COTS DRAM chips beyond just storing data

Rigorously **characterize** the **reliability** of this capability
The Capability of COTS DRAM Chips

We demonstrate that COTS DRAM chips:

1. Can simultaneously activate up to 48 rows in two neighboring subarrays

2. Can perform NOT operation with up to 32 output operands

3. Can perform up to 16-input AND, NAND, OR, and NOR operations
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DRAM Testing Infrastructure

• Developed from DRAM Bender [Olgun+, TCAD’23]*
• Fine-grained control over DRAM commands, timings, and temperature

**DRAM Chips Tested**

- **256 DDR4 chips** from two major DRAM manufacturers
- Covers **different die revisions and chip densities**

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<td></td>
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<td>18-14</td>
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<td>8Gb</td>
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<td>Samsung</td>
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<td>F</td>
<td>21-02</td>
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<td>2 (16)</td>
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<td>x8</td>
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<td>22-12</td>
<td>8Gb</td>
<td>x8</td>
<td>3200MT/s</td>
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</table>
Testing Methodology

- Carefully sweep:
  - Row addresses: Row A and Row B
  - Timing parameters: Between ACT → PRE and PRE → ACT
The Capability of COTS DRAM Chips

We demonstrate that COTS DRAM chips:

1. Can simultaneously activate up to 48 rows in two neighboring subarrays

2. Can perform NOT operation with up to 32 output operands

3. Can perform up to 16-input AND, NAND, OR, and NOR operations
Key Observation

Activating two rows in quick succession can simultaneously activate multiple rows in neighboring subarrays.
Characterization Methodology

- To understand which and how many rows are simultaneously activated
  - **Sweep** Row A and Row B addresses

![Diagram of DRAM bank and subarrays](image)

- ACT Row A
- PRE
- ACT Row B

All rows in Subarray X
All rows in Subarray Y

- Subarray X
- Row A
- Shared Sense Amplifiers
- Subarray Y
- Row B

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COTS DRAM chips have **two distinct** sets of activation patterns in **neighboring subarrays** when two rows are activated with **violated timings**.

- **Exactly the same number** of rows in each subarray are activated.
- **Twice as many** rows in one subarray compared to its neighbor subarray are activated.

**Subarray X**
- Up to **16 rows**
- Shared Sense Amplifiers
- Up to **16 rows**

**Subarray Y**
- Up to **16 rows**

A total of **32 rows**

**Subarray X**
- Up to **16 rows**
- Shared Sense Amplifiers
- Up to **32 rows**

**Subarray Y**
- Up to **32 rows**

A total of **48 rows**.
COTS DRAM chips can simultaneously activate up to 48 rows in two neighboring subarrays.
The Capability of COTS DRAM Chips

We demonstrate that COTS DRAM chips:

1. Can simultaneously activate up to 48 rows in two neighboring subarrays.

2. Can perform **NOT operation** with up to **32** output operands.

3. Can perform up to 16-input **AND, NAND, OR, and NOR** operations.
Key Idea

Connect rows in neighboring subarrays through a NOT gate by simultaneously activating rows.
NOT Operation: A Walkthrough

ACT src

connects src to bitline
NOT Operation: A Walkthrough

ACT src
Nominal

drives bitline to GND

drives bitline to VDD

GND

src

GND

VDD
dst

GND

VDD

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NOT Operation: A Walkthrough

ACT src -> PRE -> ACT dst

Nominal

<3ns

dst's bitline is still VDD

dst's bitline is still VDD

connects dst to bitline

sense amplifier is still enabled

GND

src

dst

VDD

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NOT Operation: A Walkthrough

ACT src \rightarrow \text{Nominal} \rightarrow \text{PRE} \rightarrow \text{ACT dst}

Negated value of src (VDD) is written to dst

VDD

GND

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Characterization Methodology

- Sweep **Row A and Row B addresses**

- Sweep **DRAM chip temperature**

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**Diagram Explanation:**

- ACT Row A and all rows in Subarray X, followed by PRE to ACT Row B and all rows in Subarray Y in less than 3ns.

- Temperature sweep from 50°C to 95°C.
Reliability Metric

**Success Rate** (for a DRAM cell)

Percentage of trials where the correct output of a tested operation is stored in the cell

Success rate for this cell: 50%

Visual representation of the circuit and the success rate calculation.
# Key Takeaways from In-DRAM NOT Operation

<table>
<thead>
<tr>
<th>Key Takeaway 1</th>
<th>COTS DRAM chips can perform NOT operations with up to 32 destination rows</th>
</tr>
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<tbody>
<tr>
<td>Key Takeaway 2</td>
<td>Temperature has a small effect on the reliability of NOT operations</td>
</tr>
</tbody>
</table>
Performing NOT in COTS DRAM Chips

There is at least one DRAM cell that can perform the NOT operation with a 100% success rate.

COTS DRAM chips can perform NOT operations with up to 32 destination rows.
Impact of Temperature

- Used **destination cells** that can perform NOT operation with >90% success rate at 50°C

Temperature has a small effect on the reliability of NOT operations.

From 50°C to 95°C, only 0.2% variation in average success rate.
### The Capability of COTS DRAM Chips

We demonstrate that COTS DRAM chips:

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
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<tbody>
<tr>
<td>1</td>
<td>Can simultaneously activate up to 48 rows in two neighboring subarrays</td>
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<tr>
<td>2</td>
<td>Can perform NOT operation with up to 32 output operands</td>
</tr>
<tr>
<td>3</td>
<td>Can perform <strong>up to 16-input</strong> AND, NAND, OR, and NOR operations</td>
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</table>
Key Idea

Manipulate the bitline voltage to express a wide variety of functions using multiple-row activation in neighboring subarrays.

V_{REF} \quad A \quad B \quad V_{(A,B)}

V_{REF} \quad X \quad Y \quad V_{(X,Y)}

Multiple Row ACT

sense amp. compares $V_{(A,B)}$ and $V_{(X,Y)}$
Two-Input AND and NAND Operations

- **ACT** → **PRE** → **ACT**
- Time: <3ns

**AVG(V_{DD}, V_{DD}/2)**

Reference Subarray (REF)

Compute Subarray (COM)

AVG(X, Y)

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Two-Input AND and NAND Operations

$V_{DD} = 1 \& GND = 0$

- ACT
- PRE
- ACT

sense amp. compares the voltages on the bitlines

$3V_{DD}/4$

$sense amp.$
Two-Input AND and NAND Operations

$V_{DD} = 1$ & $GND = 0$

<table>
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<tr>
<th>X</th>
<th>Y</th>
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sense amp. compares the voltages on the bitlines

$sense amp.$

$V_{DD}/2$

$3V_{DD}/4$

$V_{DD}$

$GND$
Two-Input AND and NAND Operations

- $V_{DD} = 1 \& GND = 0$

- Components:
  - ACT
  - PRE
  - ACT

Diagram:
- Voltage levels:
  - $V_{DD}/4$
  - $3V_{DD}/4$
  - $V_{DD}/2$

- Sense amp. compares the voltages on the bitlines.

Table:

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Two-Input AND and NAND Operations

V_{DD} = 1 & GND = 0

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</table>
Two-Input AND and NAND Operations

V_{DD} = 1 & GND = 0

Average (V_{DD}, V_{DD}/2)

Reference Subarray (REF)

Compute Subarray (COM)

AVG(X, Y)

We can express **AND, NAND, OR, and NOR** operations by carefully manipulating the **reference voltage**

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**Functionally-Complete Boolean Logic in Real DRAM Chips:**

*Experimental Characterization and Analysis*

İsmail Emir Yüksel  Yahya Can Tuğrul  Ataberk Olgun  F. Nisa Bostancı  A. Giray Yağhkçı  
Geraldo F. Oliveira  Haocong Luo  Juan Gómez-Luna  Mohammad Sadrosadati  Onur Mutlu

ETH Zürich

(More details in the paper)

Characterization Methodology

- **Sweep** Row A and Row B addresses
| Key Takeaway 1 | COTS DRAM chips can perform \{2, 4, 8, 16\}-input AND, NAND, OR, and NOR operations |
| Key Takeaway 2 | COTS DRAM chips can perform AND, NAND, OR, and NOR operations with very high reliability |
| Key Takeaway 3 | Data pattern slightly affects the reliability of AND, NAND, OR, and NOR operations |
Performing AND, NAND, OR, and NOR

COTS DRAM chips can perform \{2, 4, 8, 16\}-input AND, NAND, OR, and NOR operations
Performing AND, NAND, OR, and NOR

COTS DRAM chips can perform 16-input AND, NAND, OR, and NOR operations with very high success rate (>94%)
Impact of Data Pattern

1.98% variation in average success rate across all number of input operands
Impact of data pattern is consistent across all tested operations.
Impact of Data Pattern

Data pattern slightly affects the reliability of AND, NAND, OR, and NOR operations.
More in the Paper

• Detailed hypotheses & key ideas to perform
  – NOT operation
  – Many-input AND, NAND, OR, and NOR operations

• How the reliability of bitwise operations are affected by
  – The location of activated rows
  – Temperature (for AND, NAND, OR, and NOR)
  – DRAM speed rate
  – Chip density and die revision

• Discussion on the limitations of COTS DRAM chips
Functionally-Complete Boolean Logic in Real DRAM Chips: Experimental Characterization and Analysis

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ETH Zürich

Processing-using-DRAM (PuD) is an emerging paradigm that leverages the analog operational properties of DRAM circuitry to enable massively parallel in-DRAM computation. PuD has the potential to significantly reduce or eliminate costly data movement between processing elements and main memory. A common approach for PuD architectures is to make use of bulk bitwise computation (e.g., AND, OR, NOT). Prior works experimentally demonstrate three-input MAJ (i.e., MAJ3) and two-input AND and OR operations in commercial off-the-shelf (COTS) DRAM chips. Yet, demonstrations on COTS DRAM chips do not provide a functionally complete set of operations (e.g., NAND or AND and NOT).

We experimentally demonstrate that COTS DRAM chips are capable of performing 1) functionally-complete Boolean operations: NOT, NAND, and NOR and 2) many-input (i.e., more than two-input) AND and OR operations. We present an extensive systems and applications [12, 13]. Processing-using-DRAM (PuD) [29–32] is a promising paradigm that can alleviate the data movement bottleneck. PuD uses the analog operational properties of the DRAM circuitry to enable massively parallel in-DRAM computation. Many prior works [29–53] demonstrate that PuD can greatly reduce or eliminate data movement.

A widely used approach for PuD is to perform bulk bitwise operations, i.e., bitwise operations on large bit vectors. To perform bulk bitwise operations using DRAM, prior works propose modifications to the DRAM circuitry [29–31, 33, 35, 36, 43, 44, 46, 48–58]. Recent works [38, 41, 42, 45] experimentally demonstrate the feasibility of executing data copy & initialization [42, 45], i.e., the RowClone operation [49], and a subset of bitwise operations, i.e., three-input bitwise majority (MAJ3) and two-input AND and OR operations in unmodified commercial off-the-shelf (COTS) DRAM chips by operating beyond
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<td>Multiple-Row Activation in Neighboring Subarrays</td>
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<td>AND, NAND, OR, and NOR Operations</td>
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<td>Conclusion</td>
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</table>
Conclusion

• We experimentally demonstrate that commercial off-the-shelf (COTS) DRAM chips can perform:
  – **Functionally-complete** Boolean operations: NOT, NAND, and NOR
  – **Up to 16-input** AND, NAND, OR, and NOR operations

• We characterize the success rate of these operations on 256 COTS DDR4 chips from two major manufacturers

• We highlight two key results:
  – We can perform NOT and \{2, 4, 8, 16\}-input AND, NAND, OR, and NOR operations on COTS DRAM chips with very high success rates (>94%)
  – Data pattern and temperature only slightly affect the reliability of these operations

We believe these empirical results demonstrate the promising potential of using DRAM as a computation substrate
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Functionally-Complete Boolean Logic in Real DRAM Chips
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Backup Slides

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Experimental Methodology

We test all banks in each DRAM chip.

We test three neighboring subarray pairs in each bank.

We test all possible combinations of activated rows.
Performing NOT in COTS DRAM Chips

The average success of the NOT operation with

four destination row: 98.37%

thirty-two destination rows: 7.95%

As the number of destination rows increases, more DRAM cells produce incorrect results.
The Coverage of Multiple-Row Activation

Figure 5: Coverage of each $N_{RF}:N_{RL}$ activation type across tested $R_F$ and $R_L$ row pairs.
Figure 8: Success rate of the NOT operation vs. $N_{RF} : N_{RL}$ activation type.
Impact of Location in NOT Op.

- Categorize the distance between activated rows (source and destination rows) and the sense amplifiers into three regions: Far, Middle, and Close.

The distance between activated rows and the sense amplifiers significantly affects the reliability.
The effect of DRAM Speed Rate on NOT

Figure 11: Success rate of the NOT operation for different DRAM speed rates.
Figure 12: Success rate of the NOT operation for different chip density and die revision combinations for two major manufacturers.
Performing AND, NAND, OR, and NOR

The reliability distributions are very similar between 1) AND-NAND and 2) OR – NOR operations.
Impact of Temperature

Temperature has a small effect on the reliability of AND, NAND, OR, and NOR operations.
Boolean Operations vs. Number of 1s

Figure 16: Success rates of AND and OR operations based on the number of logic-1s in the input operands.
The Effect of the Location

(a) AND

(b) NAND

(c) OR

(d) NOR
Figure 20: Success rates of AND, NAND, OR, and NOR operations for three DRAM speed rates.
Chip Density & Die Revision vs. Bitwise Ops.

Success Rate (%)

Number of Input operands

AND

NAND

OR

NOR

Die Revision
- 4Gb A-die
- 4Gb M-die
- 8Gb A-die
- 8Gb M-die
DRAM Cell Operation

1. ACTIVATE (ACT)
2. PRECHARGE (PRE)
DRAM Cell Operation - ACTIVATE

- Raise wordline
- Cell loses charge to bitline
- Enable sense amp
- Bitline connects cell to bitline
- Deviation in bitline voltage

1/2 V_{DD} + \delta

\[ \frac{1}{2} V_{DD} \]

\[ \frac{1}{2} V_{DD} \]
DRAM Cell Operation - PRECHARGE

Precharge bitline for next access

Disable Sense Amp

1/2 \( V_{DD} \)

1/2 \( V_{DD} \)

enable

lower wordline

wordline

capacitor

access transistor

bitline