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Spatial Variation-Aware Read Disturbance Defenses:
Experimental Analysis of Real DRAM Chips and Implications on Future Solutions

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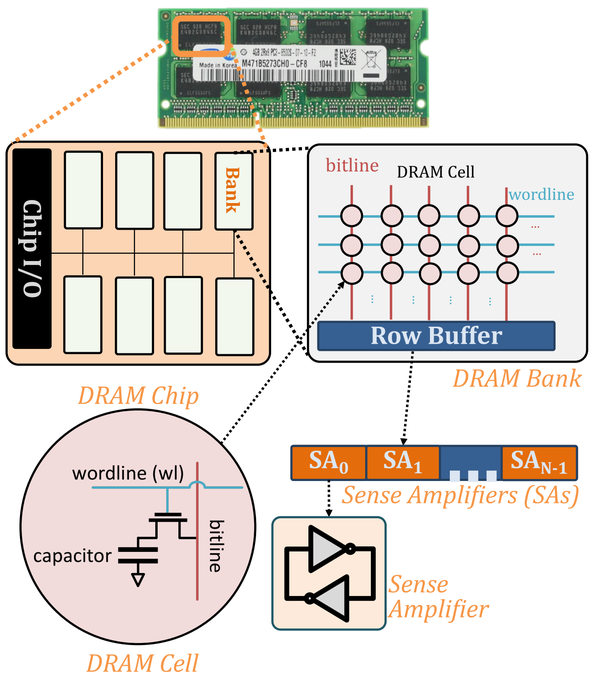
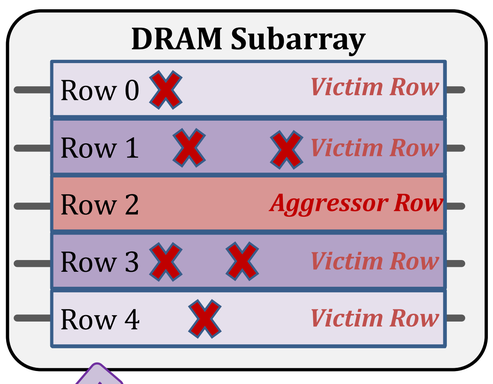
1: DRAM Background

DRAM Organization



DRAM Read Disturbance

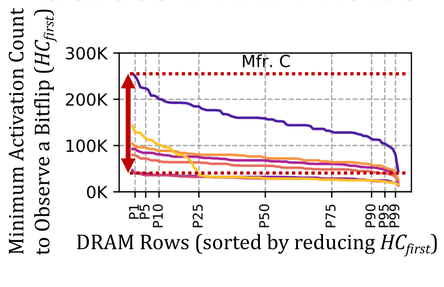


RowHammer

RowPress

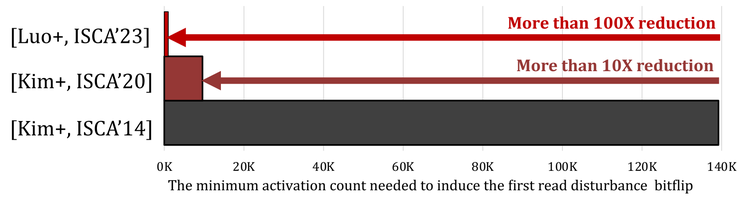
Repeatedly **opening** and **closing**
OR
keeping open
a DRAM row causes
bit flips in nearby cells

Spatial Variation in RowHammer across DRAM Rows



RowHammer vulnerability **significantly varies** across different **DRAM rows** within a DRAM bank
[Orosa, Yaglikci+ 2021]

2: Motivation and Goal



Modern DRAM chips are **more vulnerable to read disturbance**

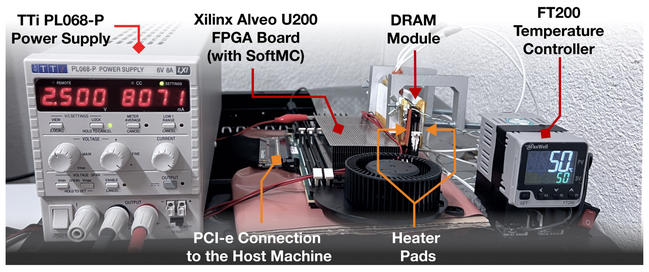
Defenses are becoming **prohibitively expensive**
[Kim+ 2020] [Luo+ 2023]

To gain **insights** into the **spatial variation** of **read disturbance** across DRAM rows

To prevent bitflips **efficiently, scalably** by leveraging the **heterogeneity** across rows

3: Understanding the Spatial Variation of Read Disturbance across DRAM Rows

Methodology



DRAMBender [Olgun+ 2023]

Full paper

GitHub

Fine-grained control over
- **DRAM commands**,
- **Timing parameters (±1.5ns)**,
- **Temperature (±0.5°C),**

Tested 144 DRAM Chips
- A Bank from each **Bank Group**
- **All Rows** in each Bank

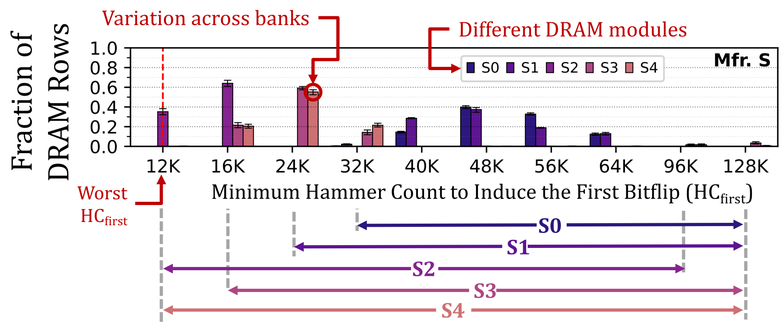
Key Takeaways

A **large variation** in the necessary *activation count* to induce the first bitflip and *bit error rate*

No strong correlation between a row's **spatial features** & read disturbance **vulnerability**

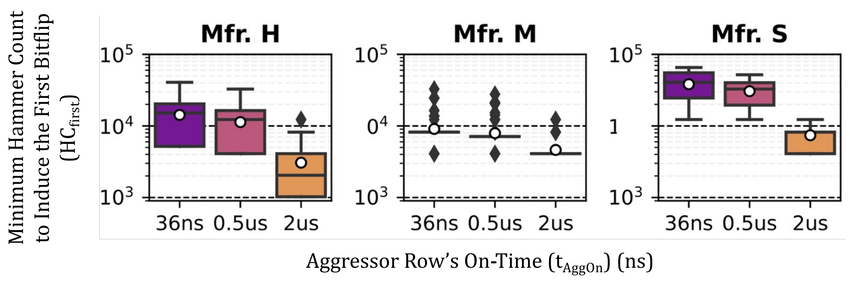
Experimental Observations on Real DRAM Chips

Distribution of HC_{first} across DRAM Rows



The minimum hammer count to induce the first bitflip **significantly varies across rows** in a DRAM bank

Effect of RowPress on the HCfirst Distribution



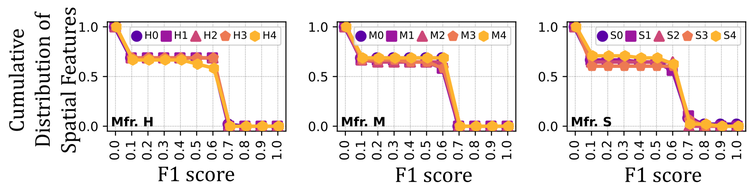
- RowPress **reduces the mean** of the distribution with increased t_{AggOn}
- There is a large variation in vulnerability to RowPress across DRAM rows

RowPress induces bitflips at **smaller hammer counts** on average and RowPress vulnerability also **significantly varies** across DRAM rows

Predictability of HC_{first} based on Spatial Features of a DRAM Row

A small fraction of DRAM chips (4/15) contain spatial features that predict HC_{first} with an F1 score larger than 0.7

The minimum hammer count to induce the first bitflip **irregularly varies across rows** in a DRAM bank

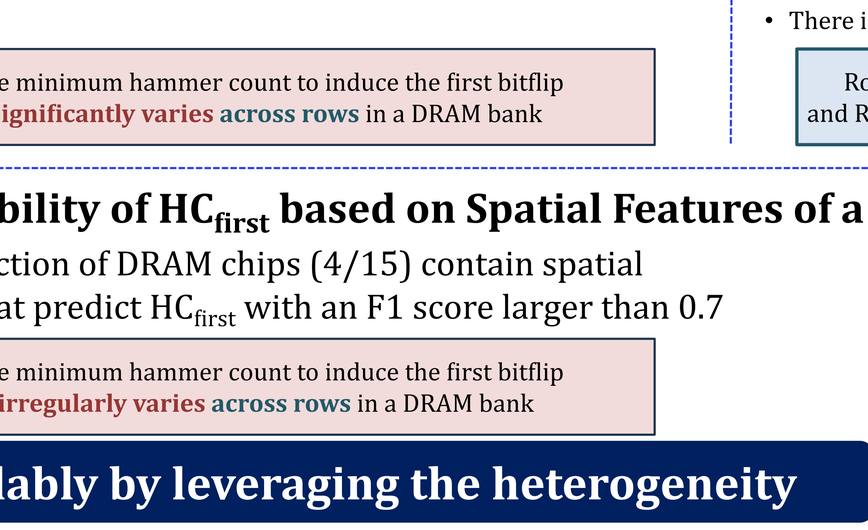


4: Preventing bitflips efficiently, scalably by leveraging the heterogeneity

Svärd: Spatial Variation-Aware Read Disturbance Defenses

- **Dynamically adapts** the aggressiveness of a defense **to the victim row's** vulnerability level
- Classifies DRAM rows into **several vulnerability-level bins**
- Maintains **a few bits** (e.g., four bits) for each DRAM row **within**
  - the memory controller in an SRAM array
  - the parity bits in DRAM
  - the DRAM row itself (e.g., 4 bits for each 8KB capacity)
- Svärd is implemented **nearby the defense** in either
  - the memory controller
  - or the DRAM chip

Svärd **significantly increases** system performance
for HC_{first} of 128 (**64**), by 1.23x (1.63x), 2.65x (4.88x),
1.03x (1.07x),1.57x (1.95x), and 2.76x (4.80x)
, over **AQUA, BlockHammer**, **Hydra**, **PARA**, and **RRS,** respectively.



5: Conclusion

The first rigorous experimental study on the spatial variation of DRAM read disturbance across DRAM rows

Read disturbance vulnerability varies **significantly** and **irregularly** across DRAM rows

Key Idea:
Dynamically tune a solution's aggressiveness (e.g., perform more/less refresh) to the **victim row's vulnerability** to DRAM read disturbance

Svärd:
Spatial Variation-Aware Read Disturbance Defenses
- Tunes **the solution's threshold** for performing a preventive action
- Implemented either in **the memory controller** or in **the DRAM chip**

Svärd significantly **reduces the performance overhead** of existing solutions